AVC Logic Family Technology and Applications

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Abstract

Texas Instruments (TI™) announces the industry's first logic family to achieve maximum propagation delays of less than 2 ns at 2.5 V. TI's next-generation logic is the Advanced Very-low-voltage CMOS (AVC) family. Although optimized for 2.5-V systems, AVC logic supports mixed-voltage systems because it is compatible with 3.3-V and 1.8-V devices. The AVC family features TI's Dynamic Output Control (DOC™) circuit (patent pending). The DOC circuit provides enough current to achieve high signaling speeds, but automatically lowers the output impedance of the circuit during a signal transition and subsequently increases the impedance to reduce the overshoot and undershoot noise that is often found in high-speed logic. This feature of AVC logic eliminates the need for series damping resistors. AVC logic also has a power-off feature that disables outputs from the device when no power is applied.

Introduction

Current trends in advanced digital electronics design continue to include lower power consumption, lower supply voltages, faster operating speeds, smaller timing budgets, and heavier loads. Many designs are making the transition from 3.3 V to 2.5 V, and bus speeds are increasing beyond 100 MHz. Encompassing all these goals makes the requirement of signal integrity more difficult to achieve. For designs that require very-low-voltage logic and bus-interface functions, TI produces a new logic family that designers of next-generation high-performance workstations, PCs, networking, and telecommunications equipment find particularly useful.

AVC Family

TI's next-generation logic family is AVC (see Figure 1). As part of TI's Widebus™ and Widebus+™ families, these devices give designers an easy migration path to higher performance and lower voltages. Also offered in the AVC family are a broad line of logic gates and octal bus-interface functions. The devices in TI's AVC family are available in multiple JEDEC-standard advanced packages to provide maximum flexibility in board layout and cost.

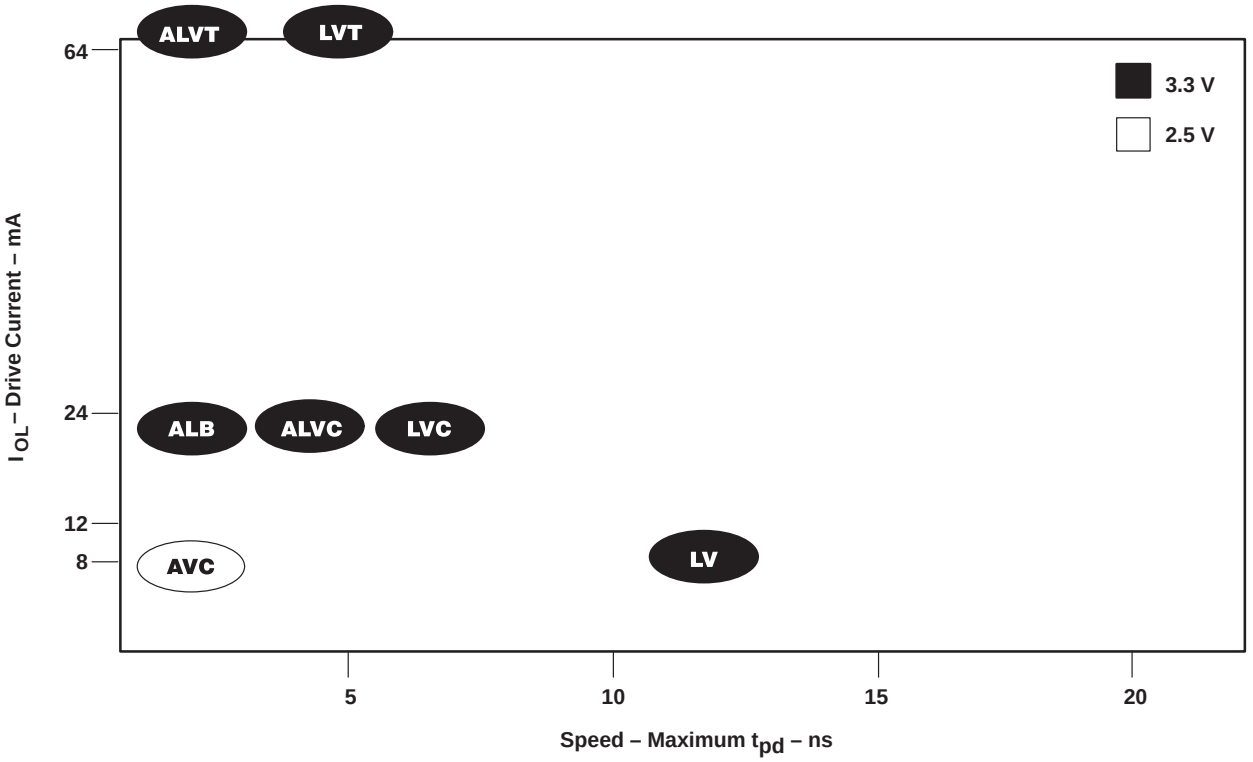

Figure 1. Low-Voltage Logic Family Performance Positioning

Unparalleled Performance

TI's AVC family is the industry's first logic family to achieve maximum propagation delays of less than 2 ns at 2.5 V. This premier performance is achieved through a combination of advances. The family was designed for high performance, incorporating several novel circuit structures and changes to conventional logic-circuit designs. TI's advanced 0.5-micron Enhanced-Performance Implanted CMOS (EPIC™) fabrication process is used to produce the new devices.

Novel Output Structure

The AVC family features TI's DOC circuit, which changes output impedance during switching (see Figure 2). The DOC circuit allows a single device to have the desirable characteristics of reduced noise, similar to damping-resistor outputs during static conditions, and high drive similar to a low-impedance output during dynamic conditions. The DOC circuit controls overshoots and undershoots and limits noise, which are inherent in high-speed, high-current devices.

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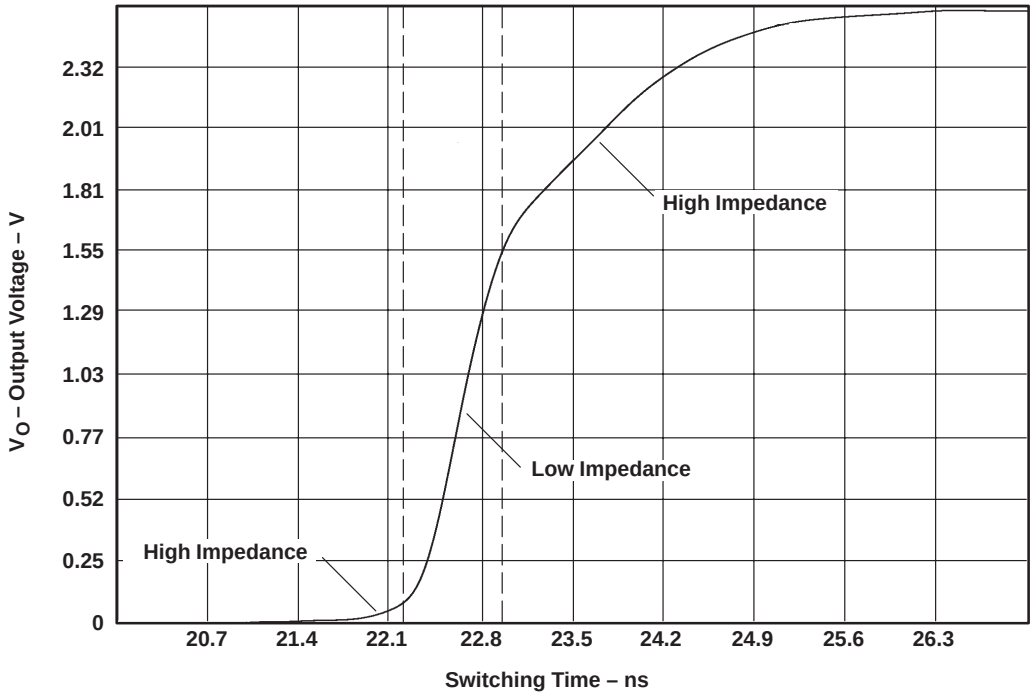


Figure 2. Impedance Changes Through Switching Transitions

Mixed-Voltage Mode and Power Off

The AVC family is optimized for low-power 2.5-V systems and effectively supports mixed-voltage systems because it is compatible with 3.3-V and 1.8-V devices. AVC device inputs and outputs are 3.6-V tolerant at 2.5-V and 1.8-V V_{CC}. This provides a bidirectional data path between 3.3-V LVTTL and 2.5-V CMOS, and a one-way data path from 3.3-V LVTTL or 2.5-V CMOS to 1.8-V CMOS. AVC logic also has a power-off isolation feature that disables outputs from the device during system partial power down.

Design Issues and AVC Family Solutions

Low Power (Optimized for 2.5 V)

Perhaps one of the most pervasive trends in advanced digital-electronics design is lower power consumption. Lower power consumption is especially important to extend battery life of portable equipment. Reduced heat dissipation from lower power consumption simplifies the measures necessary to remove heat and decrease the necessary packaging area, leading to production of smaller and less expensive products. One of the most effective ways to reduce power dissipation is to decrease integrated-circuit operating voltages. The AVC family, designed to operate at 2.5-V V_{CC}, enables high-performance, low-power, and advanced designs. Not simply a scaled-down 3.3-V family, AVC is the first logic family conceived and designed for optimized performance at 2.5 V.

Unused and Undriven Inputs (Bus Hold)

A circuit element that must be addressed when designing with a CMOS family, such as AVC, is circuit inputs. With the totem-pole structure (see Figure 3) that characterizes the inputs of CMOS devices, the input node must be held as close to the V_{CC} or GND rails as possible.

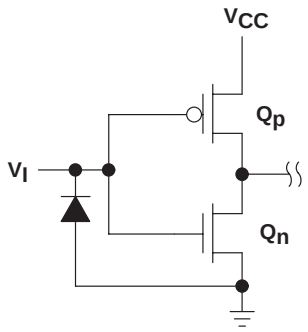


Figure 3. Totem-Pole Input Structure

Precautions should be taken to prevent the input voltage from floating near the threshold voltage because this biases both input transistors on and creates undesirably high I_{CC} currents at the V_{CC} pin of the device. Under certain conditions, this can damage the device. One way to address this concern is to place external pullup resistors at any input that might be in a high-impedance, undriven state. This is costly in terms of component count, reliability, and board area. An alternative solution is to employ the devices in the AVC family that utilize the optional bus-hold circuit at the inputs (see Figure 4). AVC devices with bus-hold circuitry are designated as AVCH.

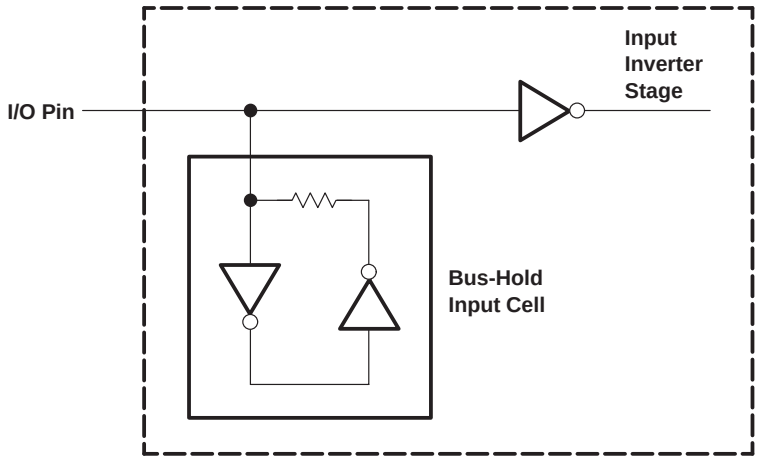


Figure 4. Typical Bus-Hold Cell

The bus-hold circuit consists of two series inverters with the output fed back to the input through a resistor. This provides a weak positive feedback by sinking or sourcing current to the input node. The bus-hold cell holds the input at its last-known valid logic state until forcibly changed by a driving circuit. Figure 5 shows the input characteristics of bus hold as the input voltage is swept from 0 V to 2.5 V. These characteristics are similar to a weak bistable latch. The bus-hold cell sinks current when the input is low, and sources current when the input is high. When the input voltage is near the threshold, the circuit sinks or sources maximum current to force the input node toward either the V_{CC} or GND rail.

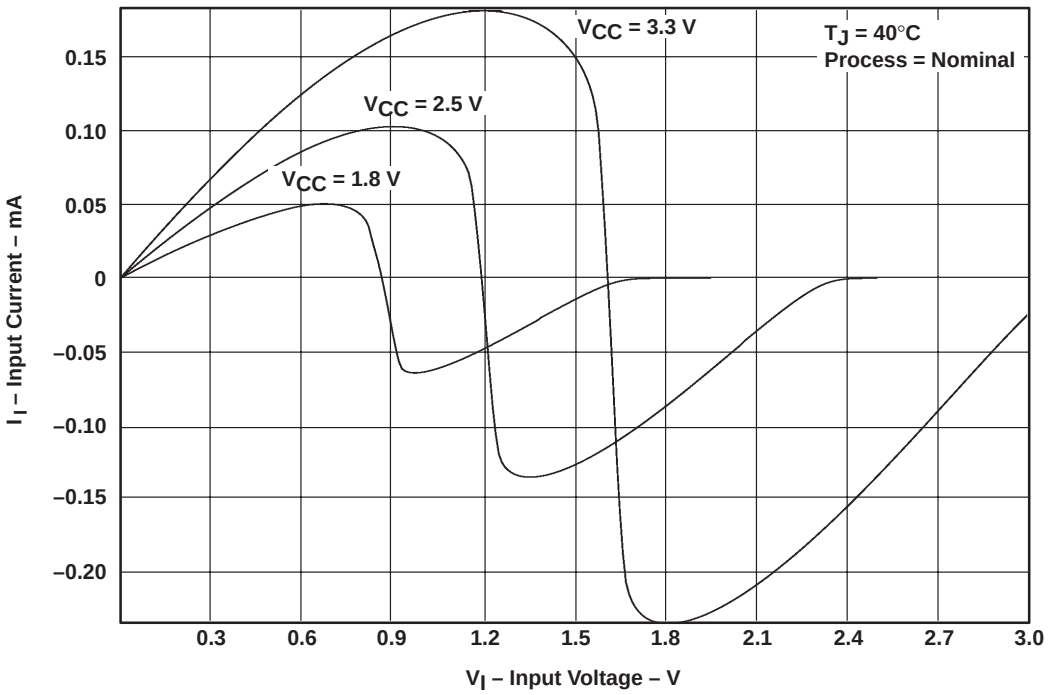


Figure 5. Bus Hold Across V_{CC}

Generally, pullup and pulldown resistors should not be used on the inputs of devices with bus hold. In applications that require pullup or pulldown resistors to hold the inputs at a specific logic level, the $I_{I(hold)}$ maximum specification should be considered. The resistor value should be chosen to overcome bus hold under worst-case conditions. The resistor must supply enough current so that the input is pulled through the threshold to the desired logic level. If the current supplied is too weak, the input node could be held near the threshold, causing a high I_{CC} that could damage the part.

Partial Power-Down and Mixed-Voltage-Mode Data Communication

The inputs and outputs of the AVC family have been designed with all reverse-current paths to V_{CC} blocked. This low I_{OFF} current feature allows the device to remain electrically connected to a bus during partial power down without loading the remaining live circuits. This feature also allows the use of this family in a mixed-voltage environment. If the inputs or outputs are at a voltage greater than the V_{CC} of the device, there is no current sourcing back through the device from the higher voltage node to the lower-voltage V_{CC} supply.

With a bidirectional AVC transceiver powered with 2.5-V V_{CC}, two-way data communication between 3.3-V LVTTL devices and 2.5-V CMOS devices can occur (see Figure 6). The inputs of the AVC part are 3.6-V tolerant and accept the LVTTL switching levels. The outputs of the AVC part, when powered at 2.5-V V_{CC} under worst-case conditions, are accepted as valid switching levels at the input of a 3.3-V LVTTL device.

With a unidirectional AVC driver powered with 1.8-V V_{CC}, data communication from 2.5-V or 3.3-V signal levels to 1.8-V devices can occur (see Figure 7). The inputs of the AVC part are tolerant of the higher voltages and accept the higher switching levels. The outputs of the AVC driver are valid 1.8-V signal levels.

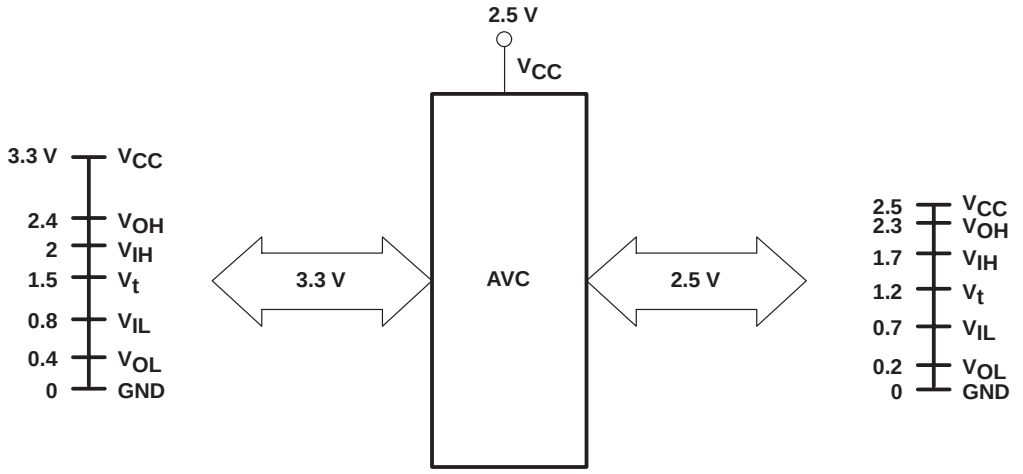


Figure 6. Device at 2.5-V V_{CC} With 3.3-V I/Os on One Side and 2.5-V I/Os on the Other, Showing Switching Levels

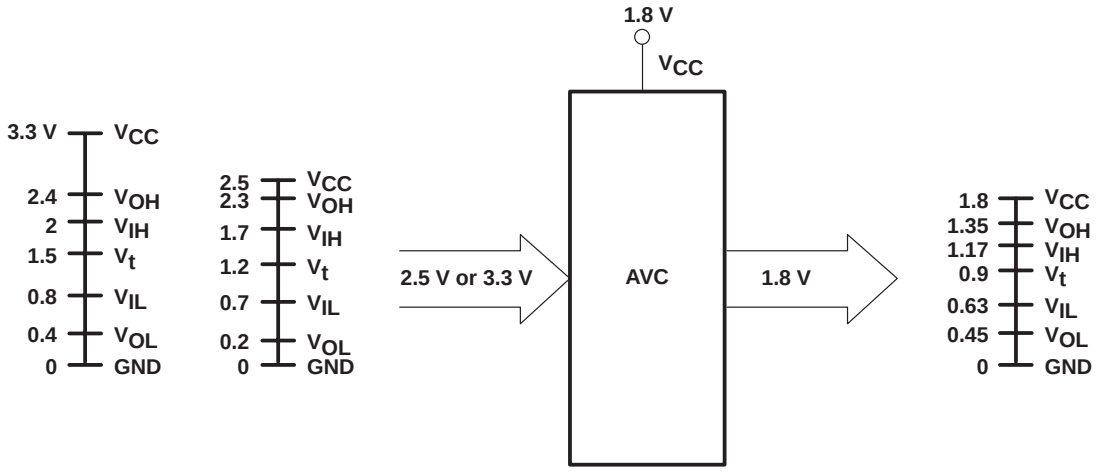


Figure 7. Device at 1.8-V V_{CC} With 2.5-V Inputs or 3.3-V Inputs, Showing Switching Levels

Device Characteristics

To facilitate a preliminary analysis of the characteristics of the AVC family, SPICE analysis graphs from TI's initial AVC-family device, the SN74AVC16245 16-bit bus transceiver with 3-state outputs are shown in Figures 8 through 22. These analyses are the outputs of SPICE simulations using standard loads specified in the parameter measurement information illustrations in Appendix A, unless otherwise noted.

Power Consumption

Figure 8 presents SPICE information about the device dynamic power consumption across the operating frequencies. Table 1 shows modeled values of power dissipation capacitance (C_{pd}). The C_{pd} data were obtained using an input edge rate of 1 ns (0%–100%), open-circuit load on the output, and one output switching with a 48-pin TSSOP (DGG) package.

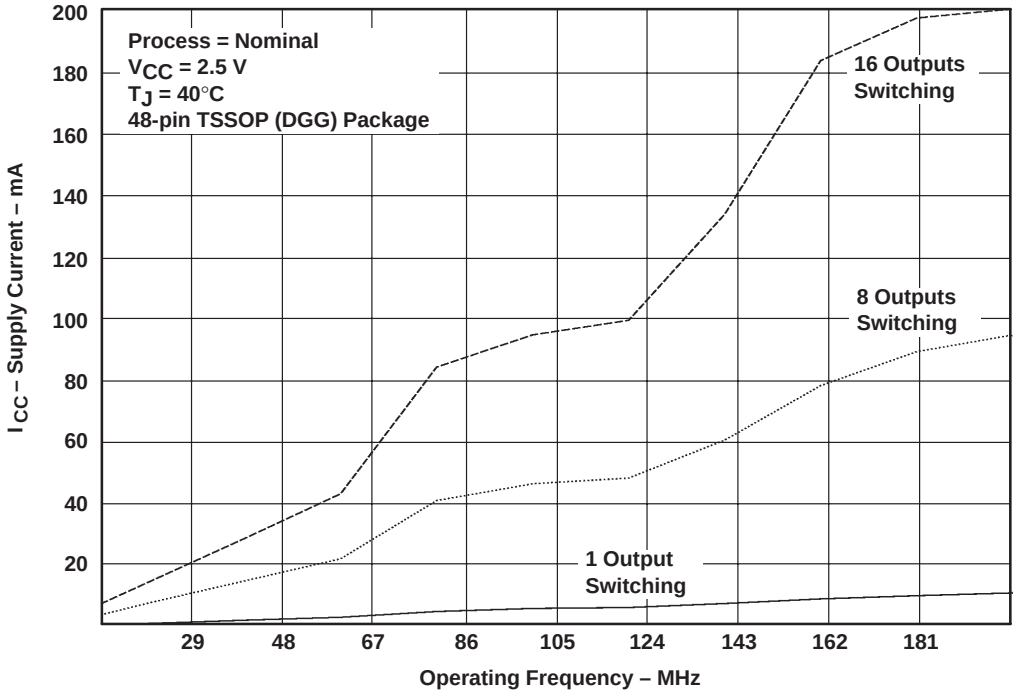


Figure 8. I_{CC} vs Frequency With 1, 8, or 16 Outputs Switching

Table 1. C_{pd} for Various Conditions, One Output Switching

PARAMETER	TEST CONDITIONS C_L = 0, f = 10 MHz	V_{CC} = 1.8 V ± 0.15 V TYP	V_{CC} = 2.5 V ± 0.2 V TYP	V_{CC} = 3.3 V ± 0.3 V TYP
C_{pd}	Outputs enabled	15.9 pF	18.1 pF	21.1 pF
C_{pd}	Outputs disabled	~1 pF	~1 pF	~1 pF

Input Characteristics

Figures 9 and 10 present SPICE information about the device static behavior. Figure 9 shows the device supply-current requirements across input voltage and Figure 10 shows the output-voltage versus input-voltage transfer curves.

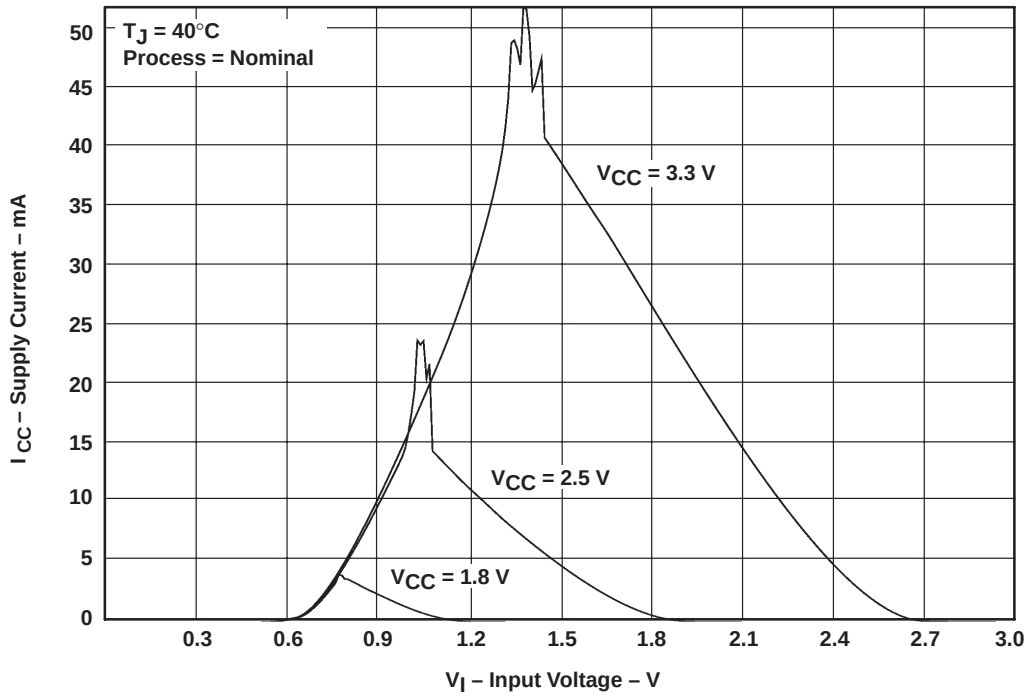


Figure 9. I_{CC} vs V_I

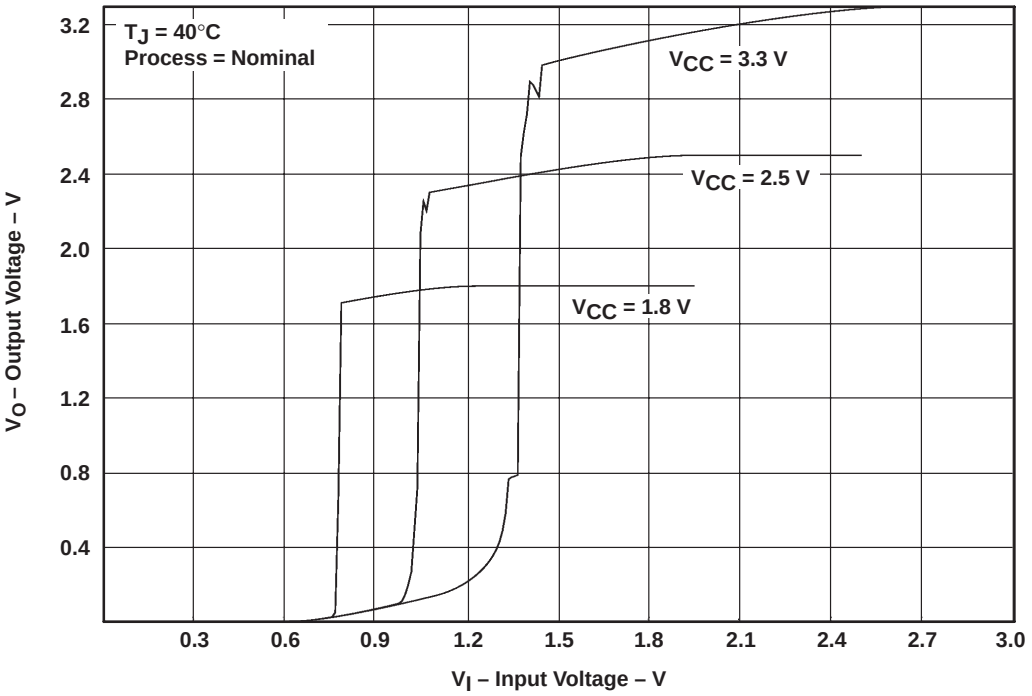


Figure 10. V_O vs V_I

Switching Performance

Figures 11 through 16 present SPICE models of the device dynamic behavior. Propagation delay times across various conditions of ambient temperature, load capacitance with one output switching, and load capacitance with 16 outputs switching are shown.

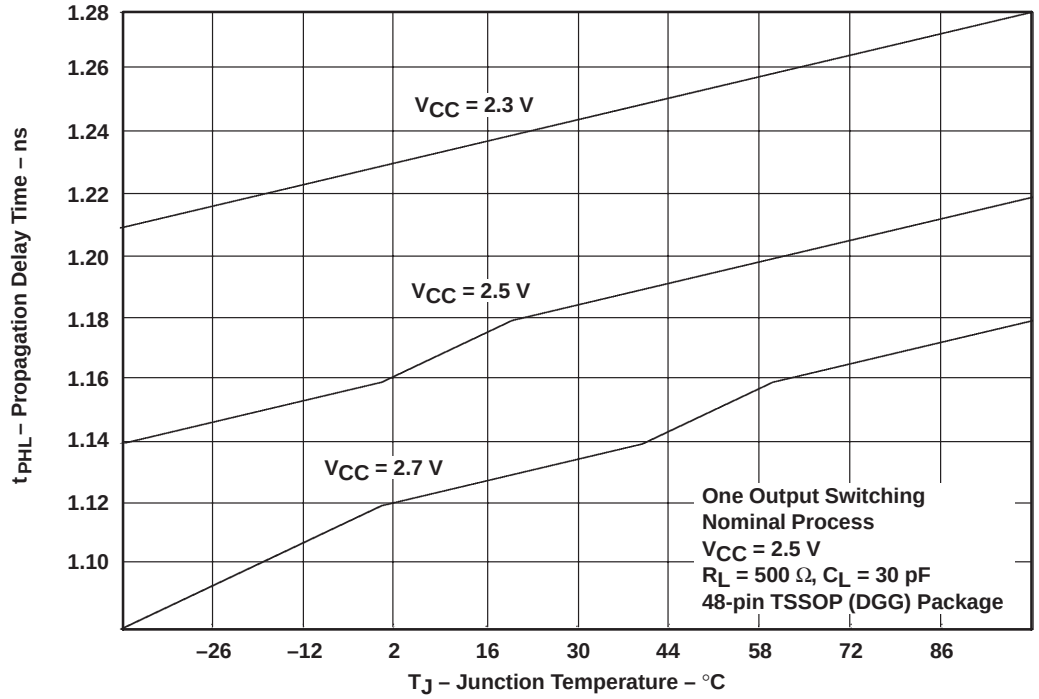


Figure 11. t_{PHL} vs T_J

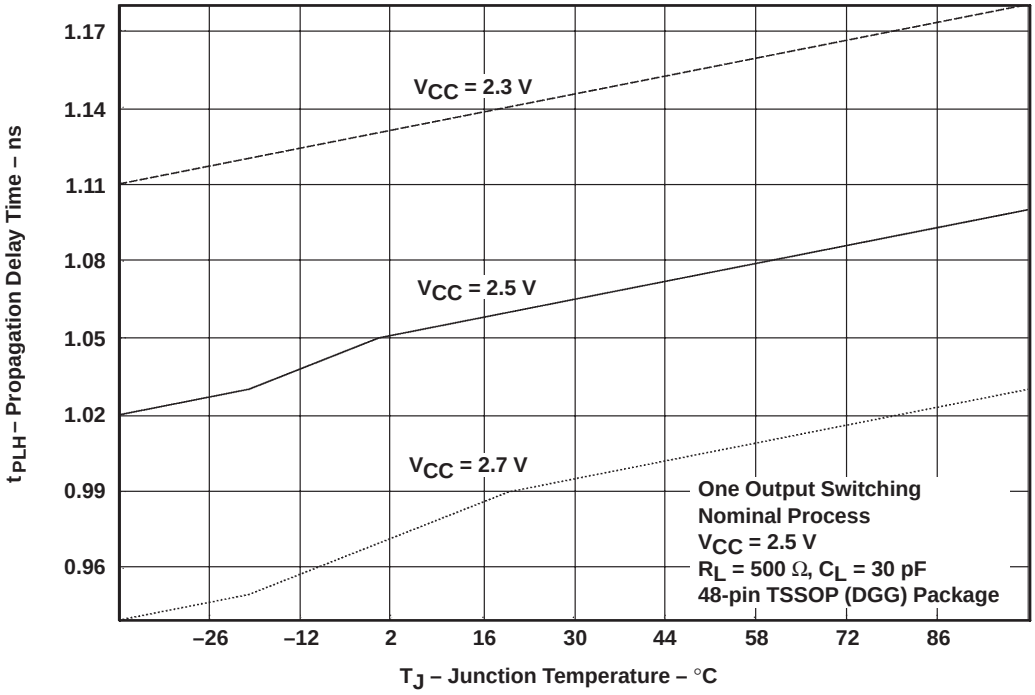


Figure 12. t_{PLH} vs T_J

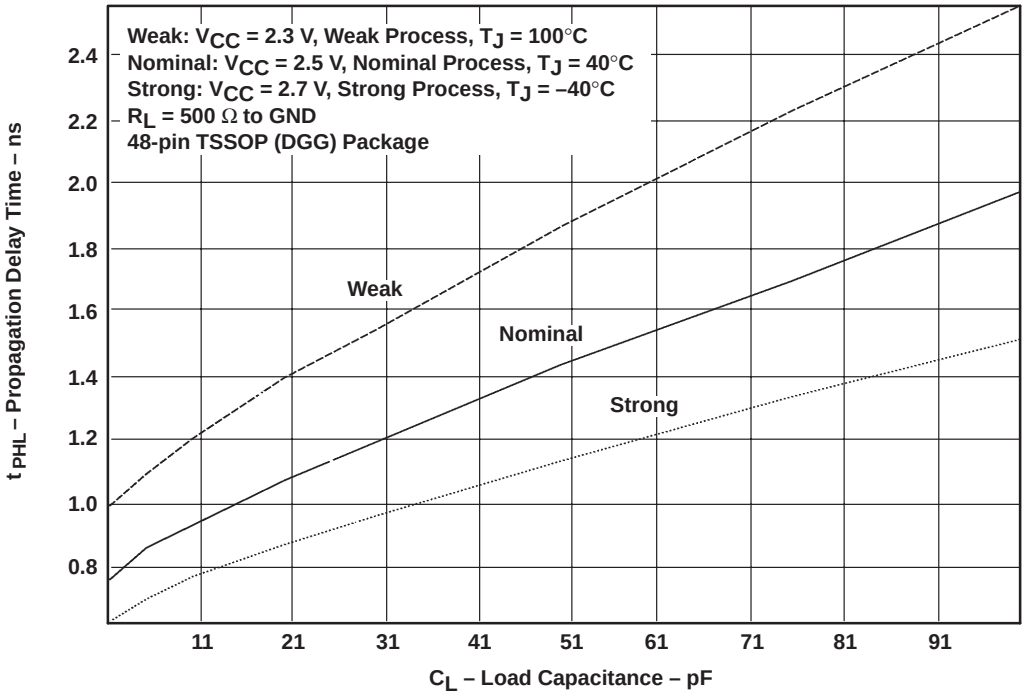


Figure 13. t_{PHL} vs Load Capacitance, One Output Switching

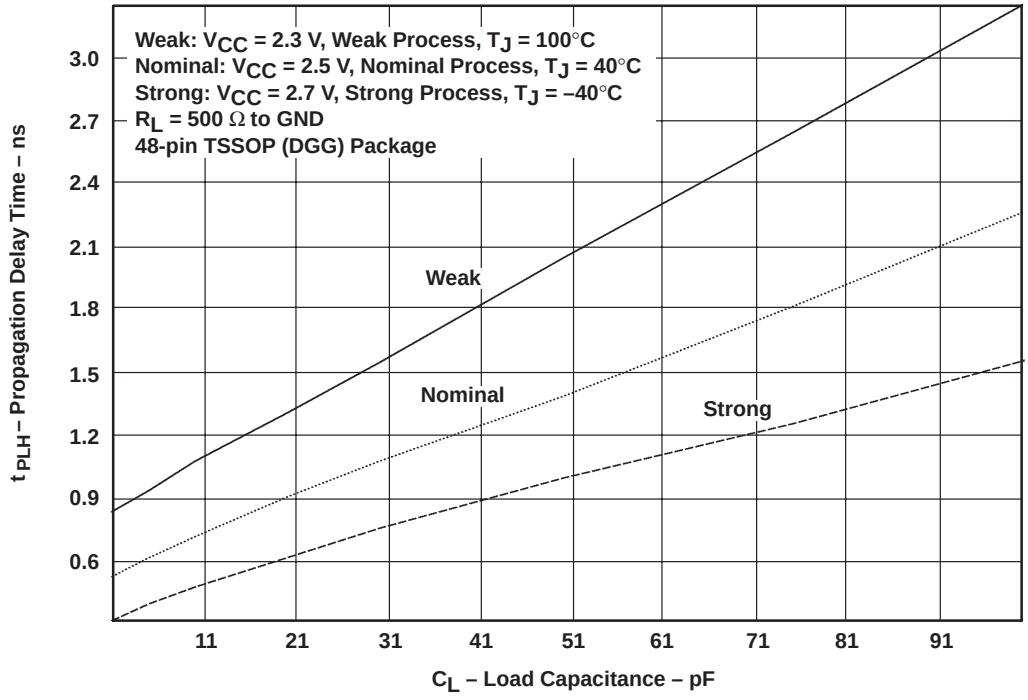


Figure 14. t_{PLH} vs Load Capacitance, One Output Switching

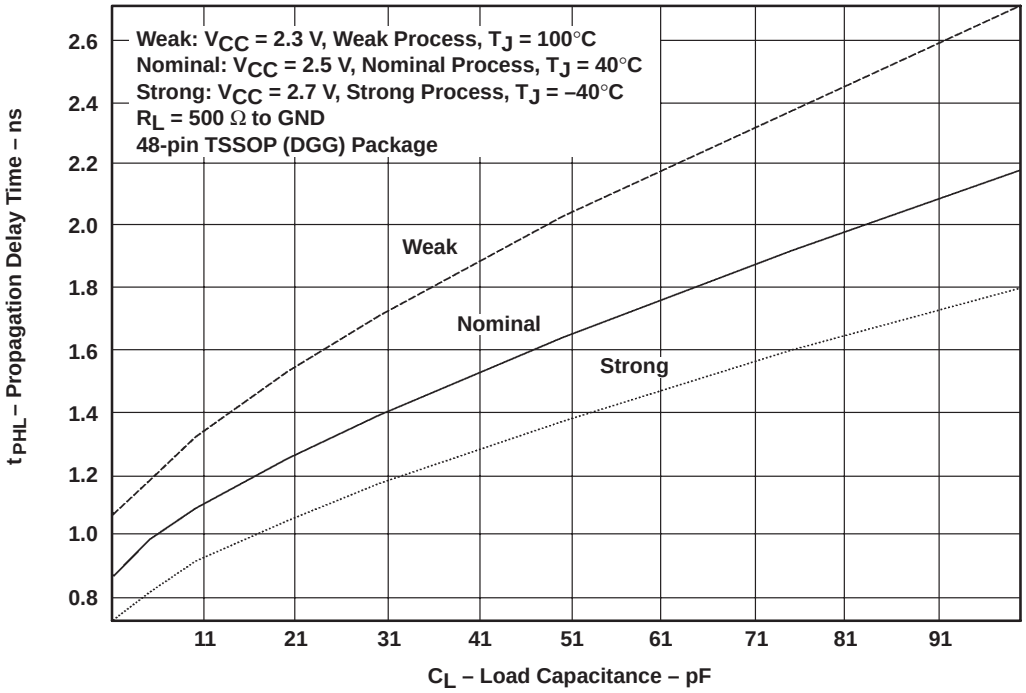


Figure 15. t_{PHL} vs Load Capacitance, 16 Outputs Switching

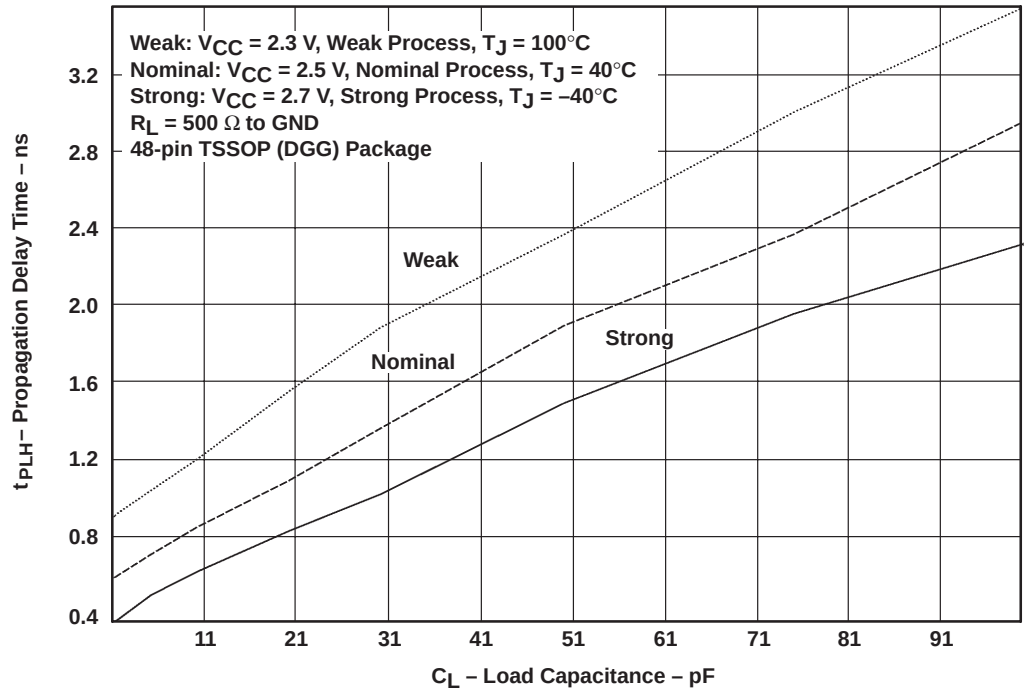


Figure 16. t_{PLH} vs Load Capacitance, 16 Outputs Switching

Signal Integrity

Perhaps the most important measure of a device's performance in the dynamic domain is the effect of varying conditions upon signal integrity. Figures 17 through 20 show SPICE simulations of the device dynamic behavior. The effect of multiple outputs switching simultaneously on one that is held at a valid logic level is shown (see Figures 17 and 18). The effects of slow input-transition time (see Figure 19), and pin-to-pin skew (see Figure 20) are shown.

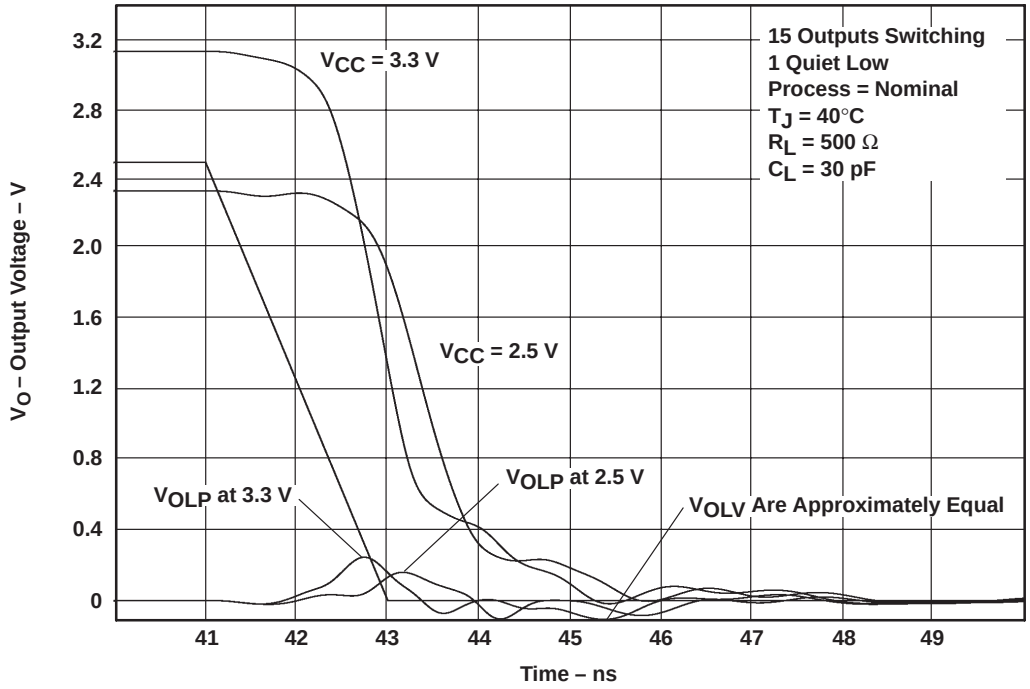


Figure 17. Simultaneous-Switching Voltage (V_{OLP}, V_{OLV}) vs Time

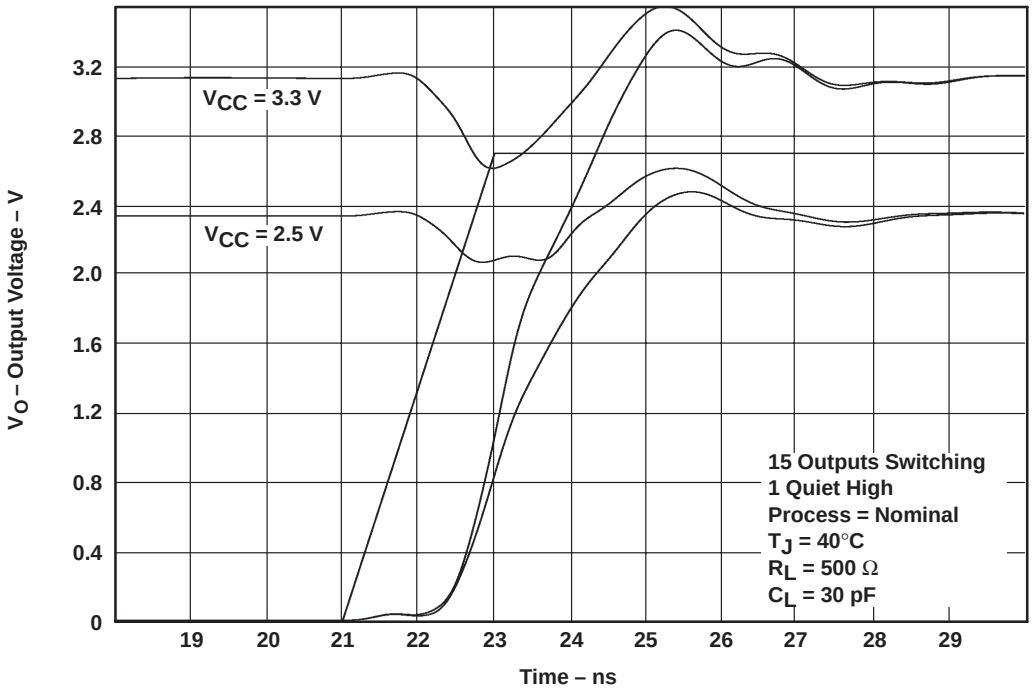


Figure 18. Simultaneous-Switching Voltage (V_{OHP}, V_{OHV}) vs Time

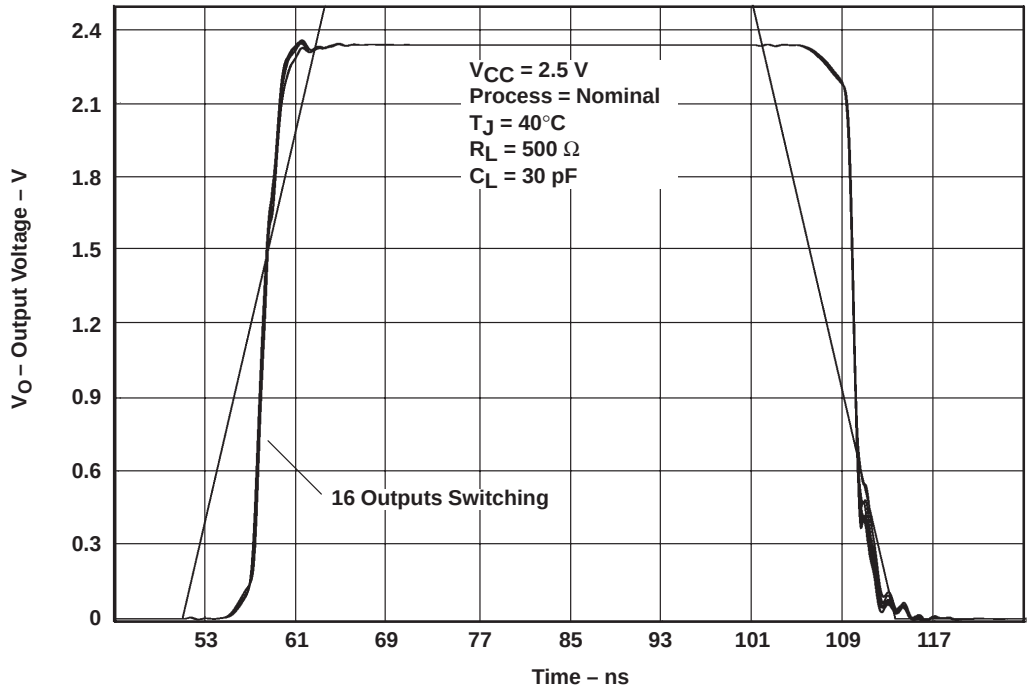


Figure 19. Slow Input-Transition Time

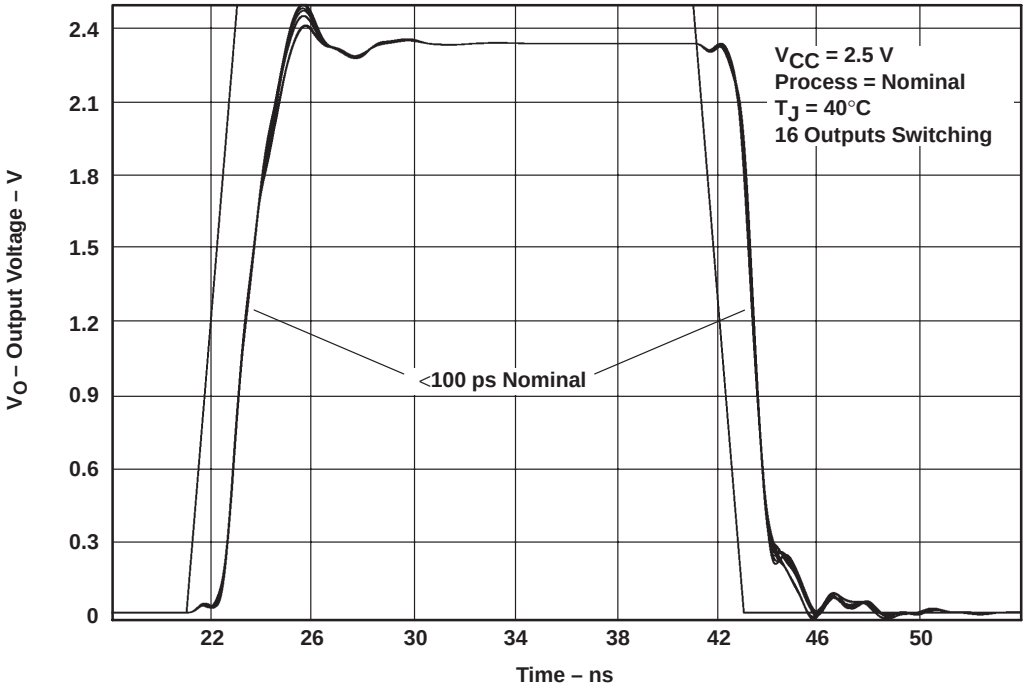


Figure 20. Pin-to-Pin Skew (t_{PHL}, t_{PLH}) (<100 ps nominal)

Output Characteristics With DOC

Selecting a component with improved output drive characteristics simplifies the design engineer's job of ensuring signal integrity and meeting timing requirements. For signal integrity, the output must have an output impedance that minimizes overshoots and undershoots. A component with 26-Ω series damping resistors on the output ports was sometimes necessary to improve the match of the impedance with the transmission-line load on the output of the buffer. The opposing characteristic that must be considered is having sufficient drive to meet the timing requirements. The AVC family features TI's DOC circuit that automatically lowers the output impedance of the circuit during a signal transition and subsequently raises the impedance to reduce overshoot and undershoot. Figures 21 and 22 contain typical voltage and current curves that illustrate the operation of the circuit as it transitions from one state to another.

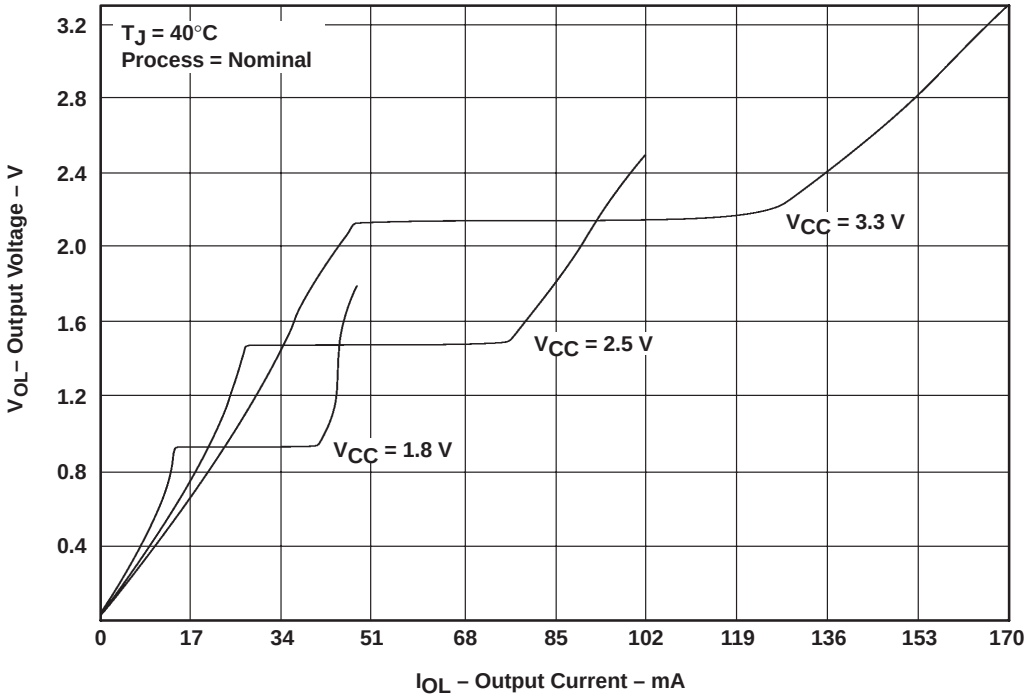


Figure 21. V_{OL} vs I_{OL}

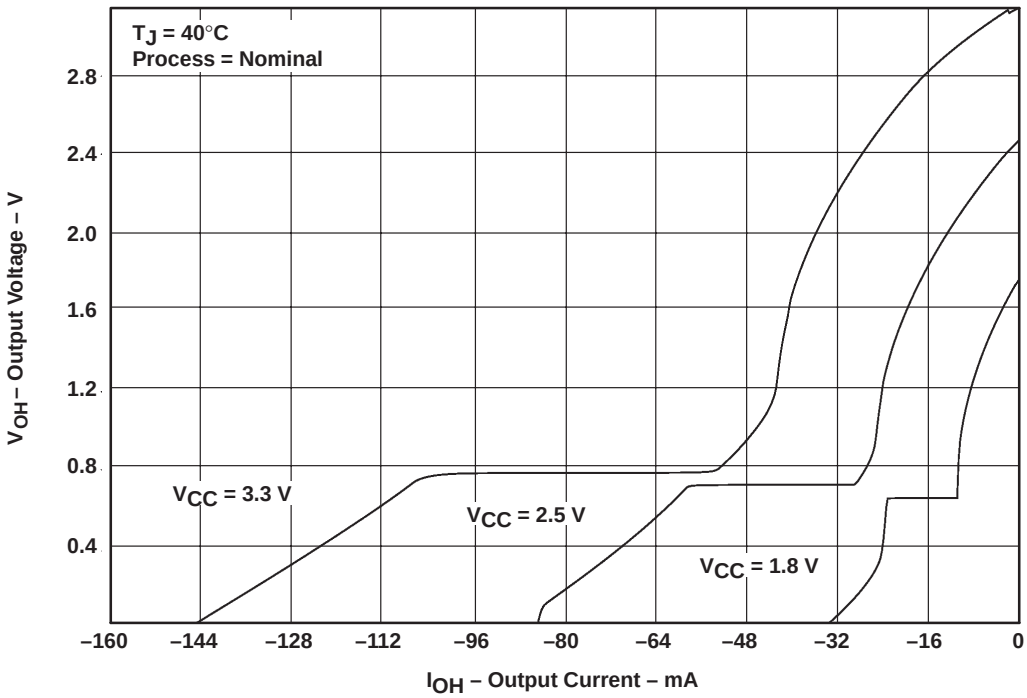


Figure 22. V_{OH} vs I_{OH}

The DOC circuitry provides enough drive current to achieve faster slew rates and meet timing requirements, but quickly switches the impedance level to reduce the overshoot and undershoot noise that is often found in high-speed logic. This feature of AVC logic eliminates the need for damping resistors in the output circuit, which are often used in series, and sometimes integrated with logic devices, to limit electrical noise. Damping resistors reduce the noise, but increase propagation delay due to the decreased drive current.

Because of the excellent signal integrity characteristics of the DOC output, transmission-line termination typically is unnecessary. Due to the high-impedance drive characteristics of the output in the static state, *the use of dc termination is specifically discouraged*. The output current that is required to bias a dc termination network could exceed the static-state output-drive capabilities of the device. AVC with DOC circuitry is ideally suited for any high-speed, point-to-point application or unterminated distributed load, such as high-speed memory interfacing.

Design Support

Examination of the characteristics of the device is a critical portion of a successful design. To aid the design engineer in analysis of device characteristics, the latest versions of IBIS models can be obtained from TI's website at http://www.ti.com. SPICE models are also available from TI. Please contact your local TI field sales representative for more information.

Features and Benefits

Table 2 provides selected AVC family features and benefits.

Table 2. Selected AVC Family Features and Benefits

FEATURES	BENEFITS
Optimized for 2.5-V V_{CC}	Enables low-power designs
Broad product offerings	Simplifies component choice
Advanced EPIC fabrication process; turbo-circuit design	Sub-2-ns (maximum) speeds at 2.5 V. Easier to meet timing windows in advanced high-speed designs
DOC outputs do not require series damping resistors internally or externally	Reduced ringing without series output resistors, increased performance and cost savings
Bus-hold option	Eliminates pullup or pulldown resistors on inputs
I_{OFF} – reverse-current paths to V_{CC} blocked on the inputs and outputs	Outputs disabled during power off for use in partial power down and mixed-voltage designs

Conclusion

For designs that require 1.8-V, 2.5-V, and 3.3-V logic functions with the highest performance, the AVC family provides the fastest, quietest logic devices optimized for 2.5-V and unterminated load conditions. AVC offers a broad line of Widebus and Widebus+ functions, logic gates, and octal bus-interface functions.

Acknowledgment

The authors of this application report are Stephen M. Nolan and Tim Ten Eyck.

Glossary

A

AVC	Advanced very-low-voltage CMOS

C

CMOS	Complementary metal-oxide semiconductor

D

DOC	Dynamic output control (patent pending)

E

EPIC	Enhanced-performance implanted CMOS

I

IBIS	I/O buffer information specification
I_I	Input current
$I_{I(hold)}$	Input current (bus hold)
I_{OH}	High-level output current
I_{OL}	Low-level output current

L

LVTTL	Low-voltage TTL (3.3-V power supply and interface levels)

P

PC	Personal computer

S

SPICE	Simulation program with integrated-circuit emphasis

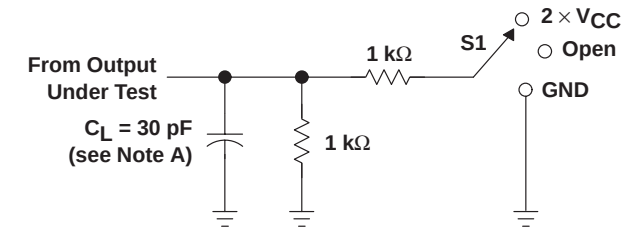
T

t_{pd}	Propagation delay time
t_{PHL}	Propagation delay time, high- to low-level output
t_{PLH}	Propagation delay time, low- to high-level output
TSSOP	Thin shrink small-outline package
TTL	Transistor-transistor logic

V

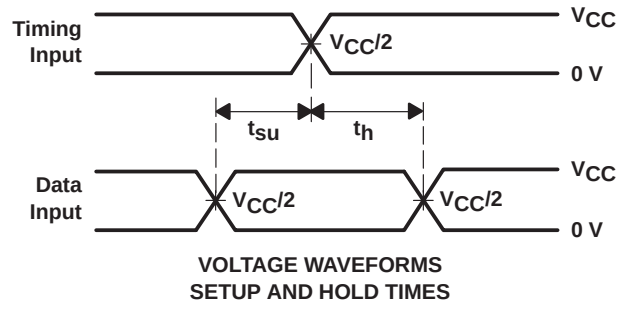
V_{OH}	High-level output voltage
V_{OL}	Low-level output voltage
V_{OHP}	High-level output voltage peak
V_{OHV}	High-level output voltage valley
V_{OLP}	Low-level output voltage peak
V_{OLV}	Low-level output voltage valley

Appendix A – Parameter Measurement Information

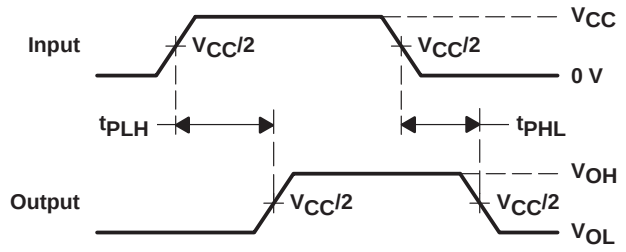


TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2 × V_{CC} GND

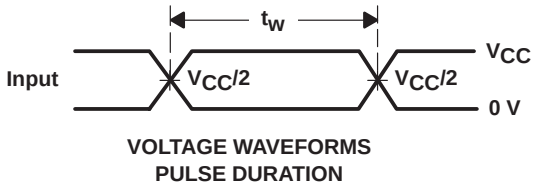
LOAD CIRCUIT



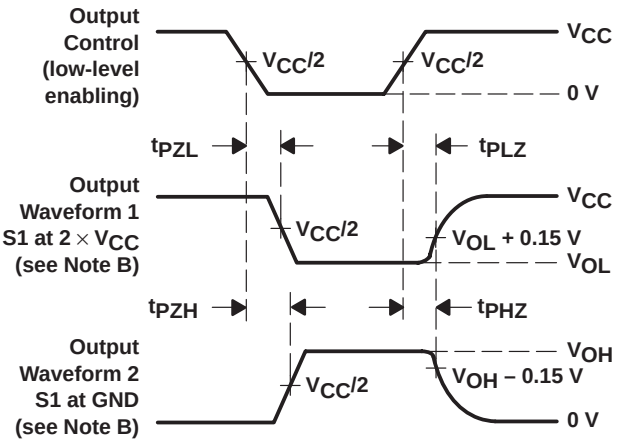
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



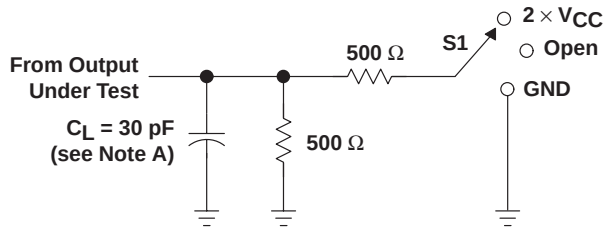
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

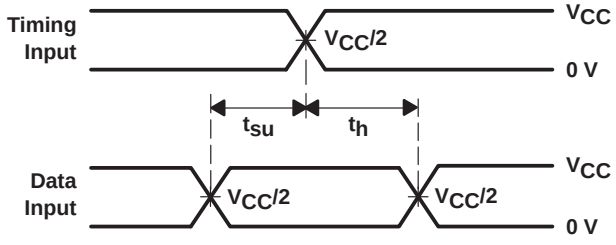
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure A–1. AVC Parameter Measurement Information (1.8 V ± 0.15 V)

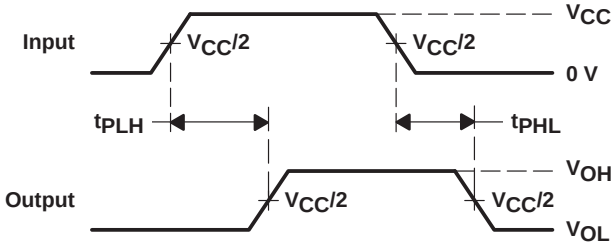


TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2 × V_{CC} GND

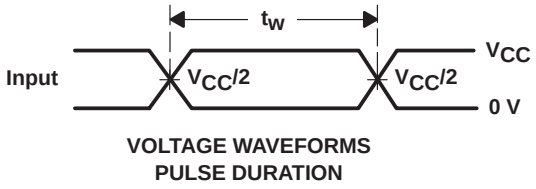
LOAD CIRCUIT



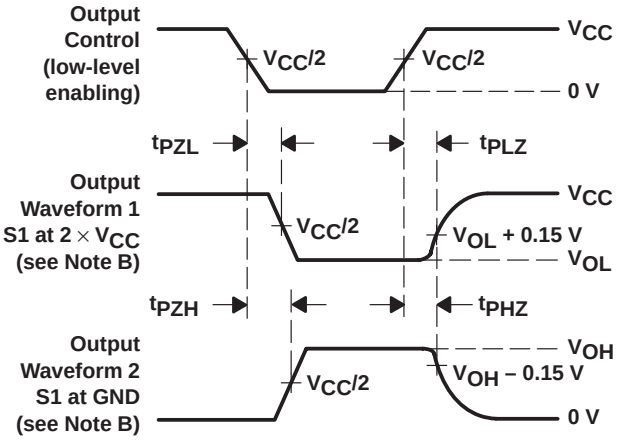
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



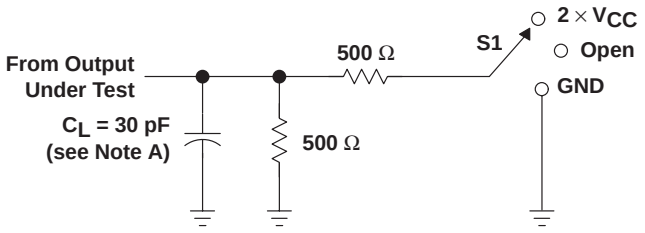
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

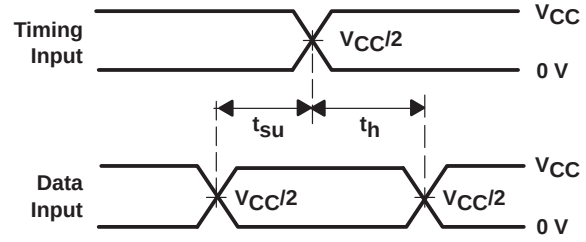
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure A–2. AVC Parameter Measurement Information (V_{CC} = 2.5 V ± 0.2 V)

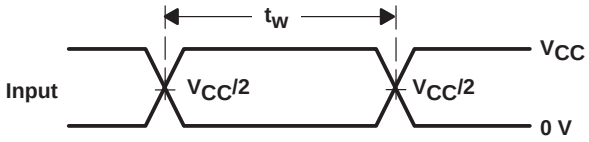


TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2 × V_{CC} GND

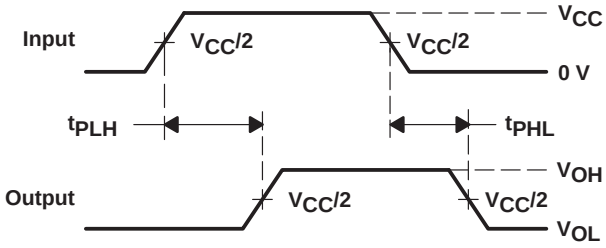
LOAD CIRCUIT



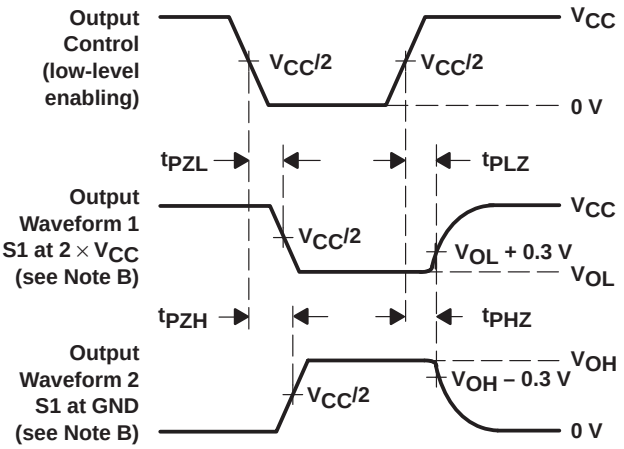
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure A–3. AVC Parameter Measurement Information (V_{CC} = 3.3 V ± 0.3 V)