Save Power with Negative-Edge-Triggered Flip-flops in Automotive CAN Applications

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TEXAS INSTRUMENTS

Introduction

In the ideal case, an idle electronic control unit (ECU) would consume no current when the vehicle is powered off. Unfortunately, Controller Area Network (CAN) controllers must continue to monitor the CAN bus for communications, therefore they are often left powered on and consume a significant amount of power, which eats into the standby power budget. By using the Schmitt-Trigger Integrated High Speed CMOS (HCS) logic family's new negative-edge triggered D-type flip-flop function, SN74HCS72-Q1, the majority of the power-hungry components can be turned off until they are required for operation.

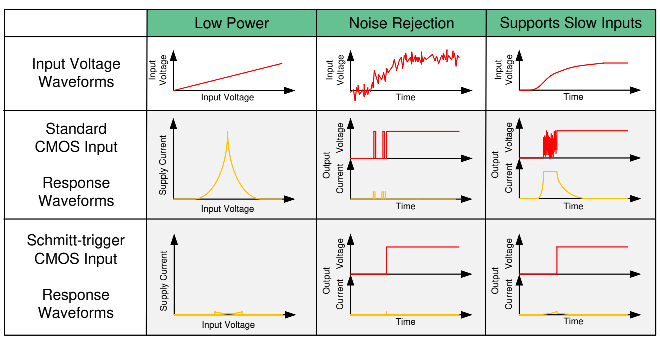

Figure 1. Benefits of HCS Schmitt-trigger Inputs

Benefits of Using SN74HCS72-Q1

- Triggers off falling edge for immediate response from CAN wake-up pattern
- Low standby power consumption (2-µA max)
- High input noise margins help mitigate false triggers
- Flexibility to accommodate active-high or active-low enables with complementary outputs
- Allows for less complex CAN transceivers saving power, size, and cost

Solution Implementation

The CAN protocol has a predefined wake-up pattern that tells the CAN transceiver to come out of standby mode. This wake-pattern will be key to the implementation of this low power CAN wake solution. An example of this circuit is illustrated in Figure 2.

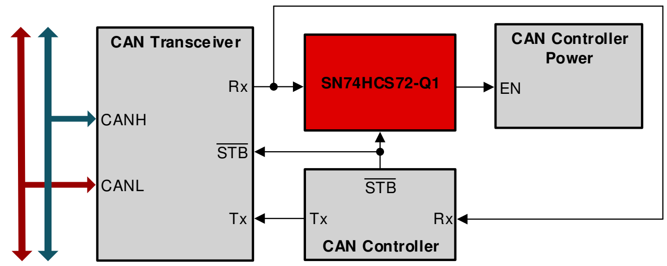

Figure 2. Low Power CAN Wake Solution

When the CAN transceiver interprets the wake-up pattern, it creates a LOW pulse at the RX pin which is typically HIGH in standby mode. With the RX pin connected to the flip-flop's $\overline{CLK}$ pin, the SN74HCS72-Q1 will utilize the falling edge of that LOW pulse to assert the enable of whatever controls the power of the CAN controller. This can be a SBC, LDO, DC/DC or PMIC, which can then begin power sequencing or just powering the CAN controller. Once the CAN controller is done performing the actions needed, it will send a LOW signal to both clear the SN74HCS72-Q1 and put the CAN transceiver back into standby mode to await the next wake-up pattern. An example timing diagram is provided in Figure 3 to illustrate this process.

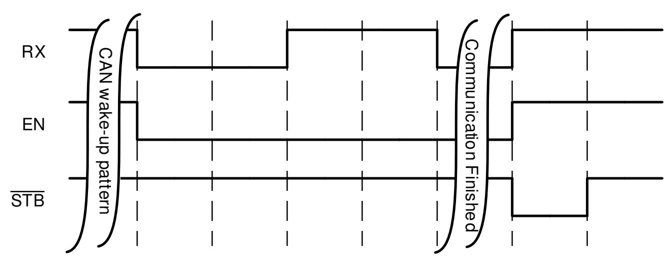

Figure 3. CAN Wake Timing Diagram

The SN74HCS72-Q1 is the recommended solution for this application because it provides flexibility using complimentary outputs and conserves standby mode power budget with a maximum I_{CC} of only 2 µA. Other devices in the HCS family can also be implemented for additional functionality in the circuit, for example if there are multiple CAN channels to monitor, an OR gate can be added to combine the enable signals.

1 References

1.1 Trademarks

All trademarks are the property of their respective owners.

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