Application Brief

Optimizing DC Fast Charger Systems Using Logic and Translation

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Functional Block Diagram

For the purpose of this report, a simplified DC fast charger block diagram is used to illustrate the logic and translation use cases, see Figure 1 and Figure 2. Each red block has an associated use-case document. Links are provided in Table 1 and Table 2. For a more complete block diagram, see the Interactive Online end Equipment Reference Diagram for DC Fast Charging Stations.

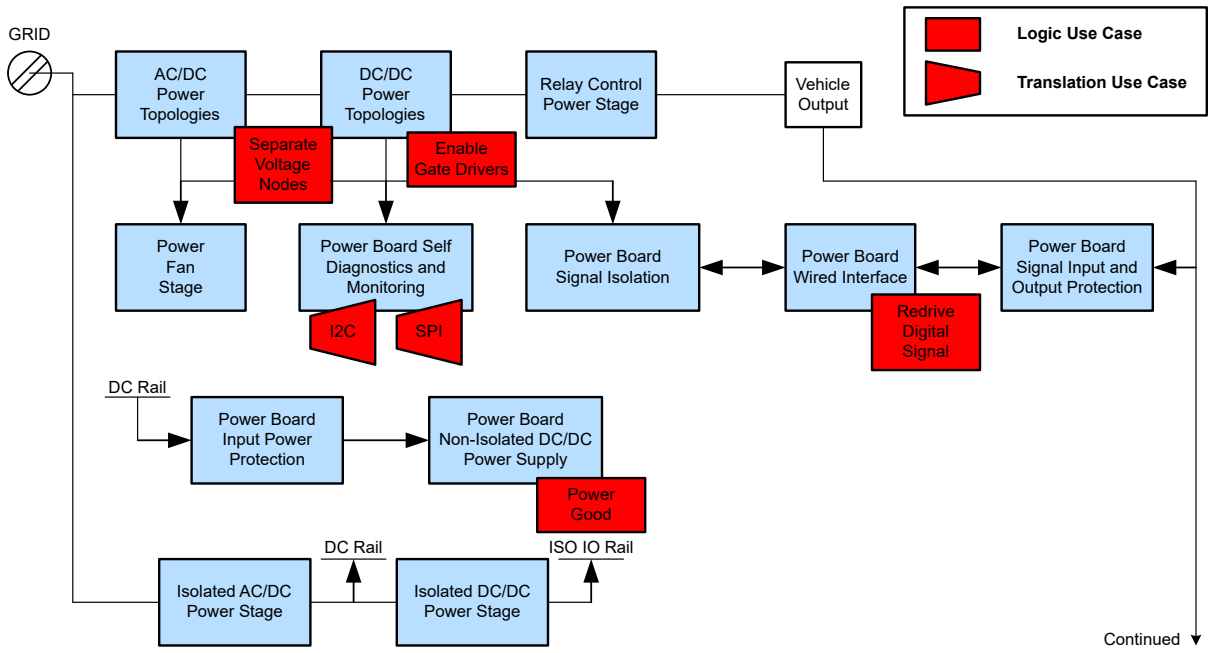

Figure 1. Simplified Block Diagram for DC Fast Chargers Power Section

Logic and Translation Use Cases for Power Section

Each use case is linked to a separate short document that provides additional details including a block diagram, design tips, and part recommendations. The nearest block and use-case identifiers are listed to match up exactly to the use cases shown in the provided *simplified block diagram*.

Table 1. Logic Use Cases

Nearest Block	Use-Case Identifier	Use Case
AC/DC Power Topologies	Separate Voltage Nodes	*Separate Digital Voltage Nodes*
DC/DC Power Topologies	Enable Gate Drivers	*Add Enable to Gate Drivers*
Power Board Wired Interface	Redrive Digital Signal	*Redrive Digital Signals*
Power Board Non-Isolated DC/DC Power Supply	Power Good	*Combine Power Good Signals*

Table 2. Translation Use Cases

Nearest Block	Use-Case Identifier	Use Case
Power Board Self Diagnostics and Monitoring	I2C	*Translate Voltages for I2C*
	SPI	*Translate Voltages for SPI*

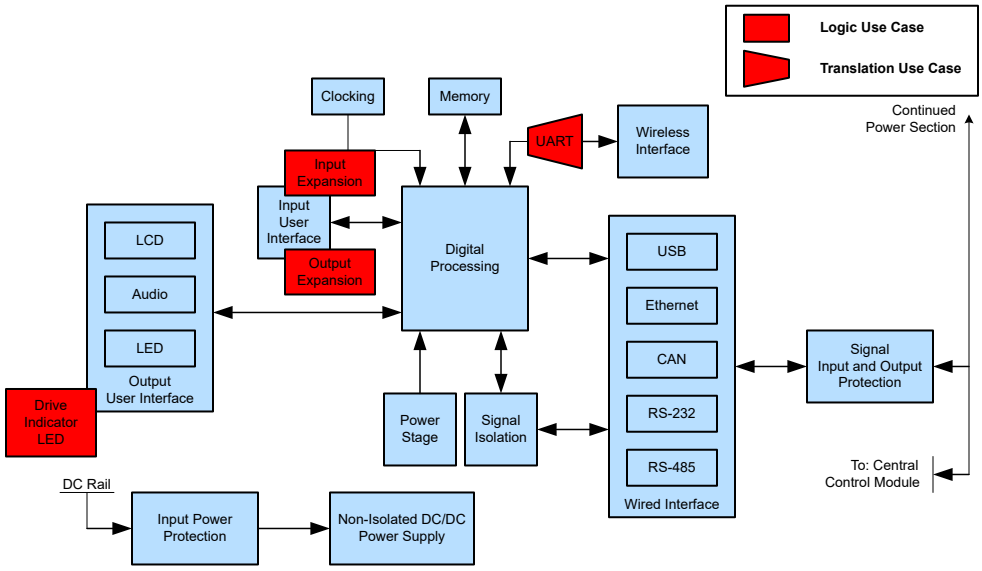

Figure 2. Simplified Block Diagram for DC Fast Chargers Human-Machine Interface Section

Logic and Translation Use Cases for Human-Machine Interface Section

Each use case is linked to a separate short document that provides additional details including a block diagram, design tips, and part recommendations. The nearest block and use-case identifiers are listed to match up exactly to the use cases shown in the provided *simplified block diagram*.

Table 3. Logic Use Cases

Nearest Block	Use-Case Identifier	Use Case
Output User Interface	Drive Indicator LED	*Drive Indicator LEDs*
Input User Interface	Input Expansion	*Increase the Number of Inputs on a Microcontroller*
	Output Expansion	*Increase the Number of Outputs on a Microcontroller*

Table 4. Translation Use Cases

Nearest Block	Use-Case Identifier	Use Case
Wireless Interface	UART	*Translate Voltages for UART*

Add Enable to Gate Drivers

It is common to see DC fast chargers include multiple gate drivers. The gate driver can have safety features included, they can be included in software, or an added logic circuit can be used to disable signals when required. By using AND gates, a single input can be used to control many gate drivers, forcing them all into the off state at the same time.

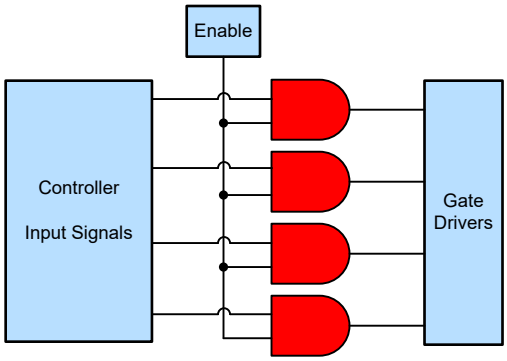

Figure 3. Example block diagram to use AND gates to enable gate driver signals

Design Considerations

- Open-drain outputs require pull-up resistors
- Keep traces relatively short to reduce capacitive loading and improve performance
- Easily enable multiple gate drivers through one signal
- [FAQ] How do I Calculate Power Consumption for my CMOS Logic Device?
- [FAQ] How does a slow or floating input affect a CMOS device?
- Need additional assistance? Ask our engineers a question on the *TI E2E™ Logic Support Forum*

Recommended Parts

Part Number	AEC-Q100	V_{CC} Range	Channels	Features
SN74LVC08A		1.65 V — 3.6 V	4	High Drive Strength - 24 mA
SN74LVC08A-Q1	✓	2 V — 3.6 V		
SN74AHCT08		4.5 V — 5.5 V	4	TTL-compatible inputs
SN74AHCT08Q-Q1	✓			
SN74HCS08		2 V — 6 V	4	Schmitt-trigger inputs
SN74HCS08-Q1	✓			

For more devices, browse through the *online parametric tool* where you can sort by desired voltage, channel numbers, and other features.

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