Application Note

Protect PFC and Achieve High Performance with DC Input Using TPSI3052

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ABSTRACT

Data center, or enterprise server switch-mode power supplies, typically implement a totem pole bridgeless Power Factor Correction (PFC) block using digital implementations instead of analog implementations to improve efficiency and reduce solution size and space. This application note explains how to protect PFC, achieve higher efficiency under DC input by configuring a circuit using TPSI3052. This can be used in designs to further reduct power loss and alleviate thermal issues. A simple external circuit is introduced and the working principle is explained in detail. Test results show that this is effective in solving heat generation and efficiency reduction issues due to current flow under DC input.

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Trademarks

1 Introduction

Server power SMPS modules must be able to operate normally not only with AC input voltage, but also with DC input voltage (battery power). When the DC input voltage is applied, the polarity is sometimes reversed (live terminal (-) voltage, neutral terminal (+) voltage). In this case, the slow switch high-side FET turned on, but the existing charge pump circuit cannot generate the VDD voltage (this does not switch because this is referenced to the opposite DC input), so the high-side FET cannot be turned on. The current flows to the parasitic diode, causing heat generation and reduced efficiency. Therefore, an appropriate IC and external circuit design is needed to make sure of stable operation.

2 Using a Solid-State Relay as an Isolated 15V Supply

The TPSI3052 is a fully integrated, isolated switch driver with integrated bias, which when combined with an external power switch, forms a complete isolated solid state relay implementation. With a nominal gate drive voltage of 15V with peak source current (1.5A) and peak sink current (3.0A), a large variety of external power switches such as MOSFETs, IGBTs, or SCRs can be chosen to meet a wide range of applications. The TPSI3052 generates a secondary bias supply from the power received from the primary side, so no isolated secondary supply bias is required. In this case, the TPSI3052 is not used for a solid-state relay, but instead serves as a low-cost isolated bias supplyto generate a floating 15V output.

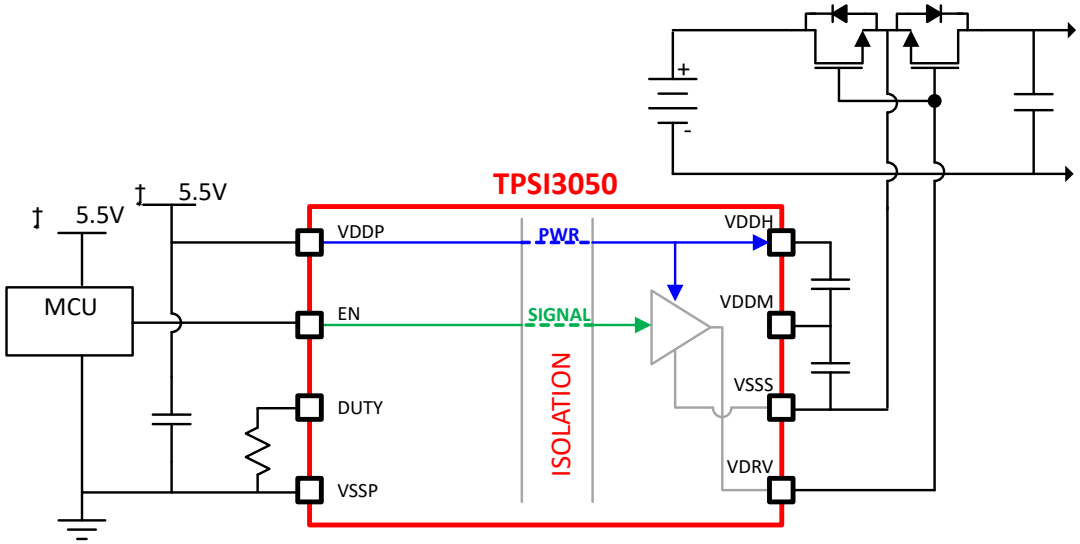


Figure 2-1. TPSI3052 Simplified Schematic

3 Topology of Totem Pole PFC for Applying Turn On Switch

A basic totem-pole PFC structure is shown in Figure 3-1. Note that Q3, Q4 and the inductor consist of a boost converter. Based on VAC polarity, Q3 and Q4 alternately work as a PFC main switch or sync switch. During a positive VAC cycle, Q4 is the main switch, while Q3 works as a sync FET. The driving signals for Q3 and Q4 are complementary: Q4 is controlled by the duty cycle (D) from the control loop, while Q3 is controlled by 1 – D. During a negative VAC cycle, the function of Q4 and Q3 is swapped where Q3 becomes the main switch, and Q4 works as a sync FET. The driving signals for Q3 and Q4 are still complementary, but Q3 is now controlled by D while Q4 is controlled by 1 – D. Because of the reverse recovery issue, a regular MOSFET cannot be used in a continuous-conduction mode (CCM) totem-pole PFC, therefore, Q3 and Q4 need to be gallium nitride (GaN) FETs, which have no reverse recovery. Q1 and Q2 diodes are paralleled with regular MOSFETs to further improve efficiency.

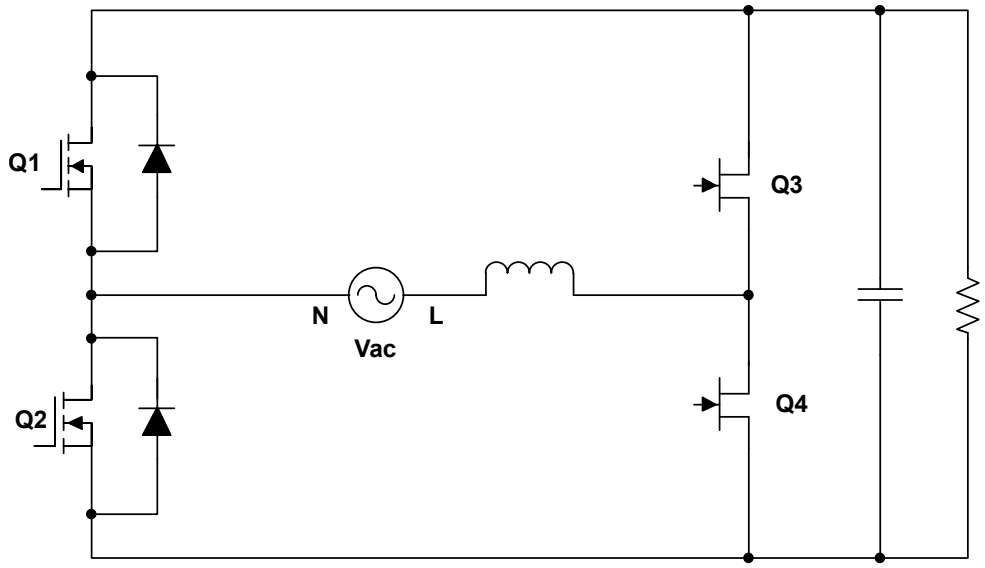


Figure 3-1. Basic Totem Pole PFC Circuit Structure

4 Original Implementation for Driving PFC Slow Switch at High-side and Low-side

When the DC input voltage is applied and the polarity is reversed (live terminal (-) voltage, neutral terminal (+) voltage), the slow switch high side FET turned on, but the existing charge pump circuit cannot generate VDD voltage. Since this is a DC input, this does not switch, so the high-side FET cannot be turned on, and current flows to the parasitic diode, causing heat generation and reduced efficiency.

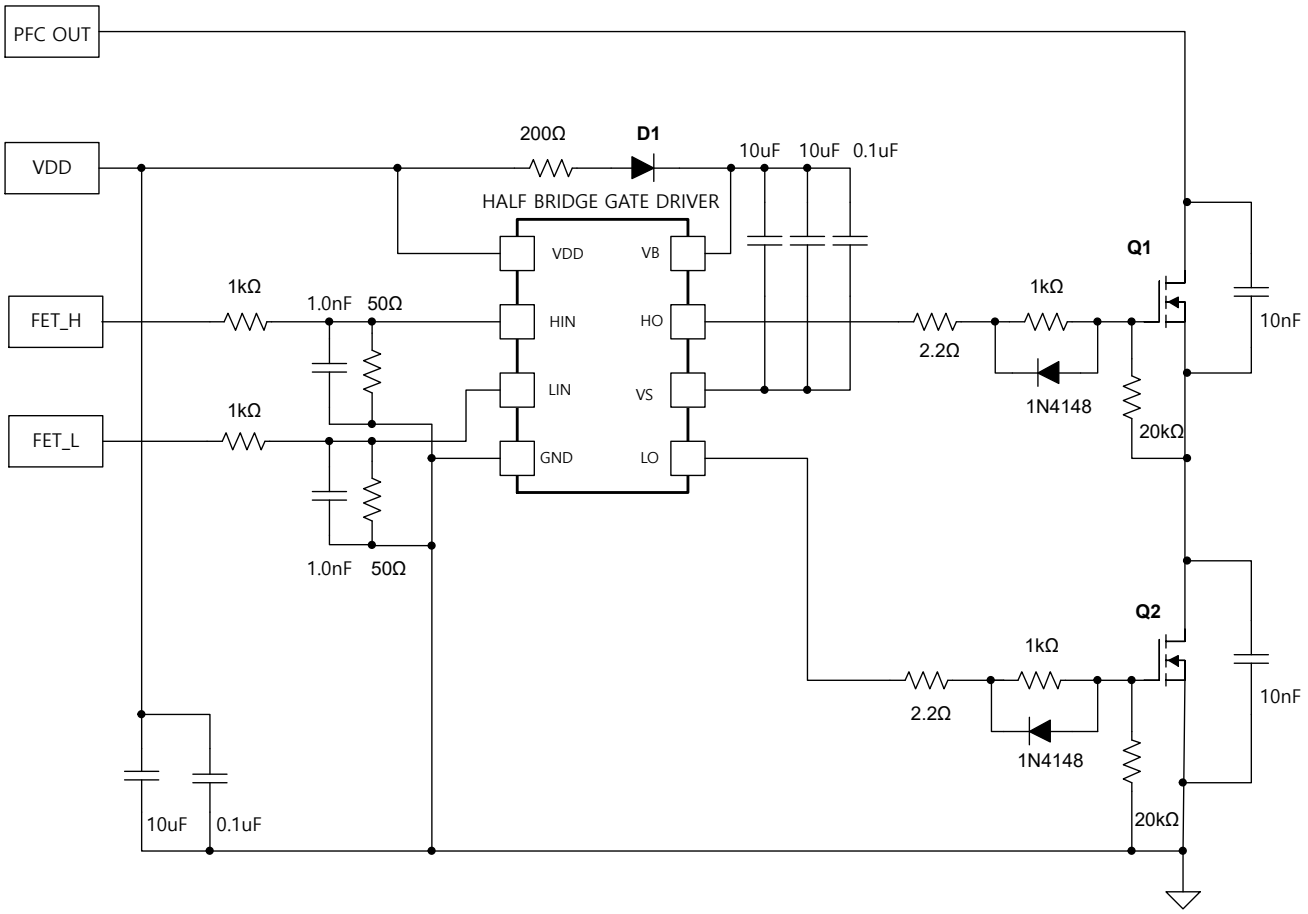


Figure 4-1. Conventional Circuit for Operating PFC Slow Switch at High-side (Q1)

5 Achieving Performance for Driving PFC Slow Switch at High-side and Low-side

To improve the driving capability of not only the AC input voltage, but also of the DC input voltage or the battery voltage, the VDD of the driver IC high-side is generated using TPSI3052. The high-side FET can be driven even when the FET is a DC input, and the circuit is configured as seen in Figure 5-1.

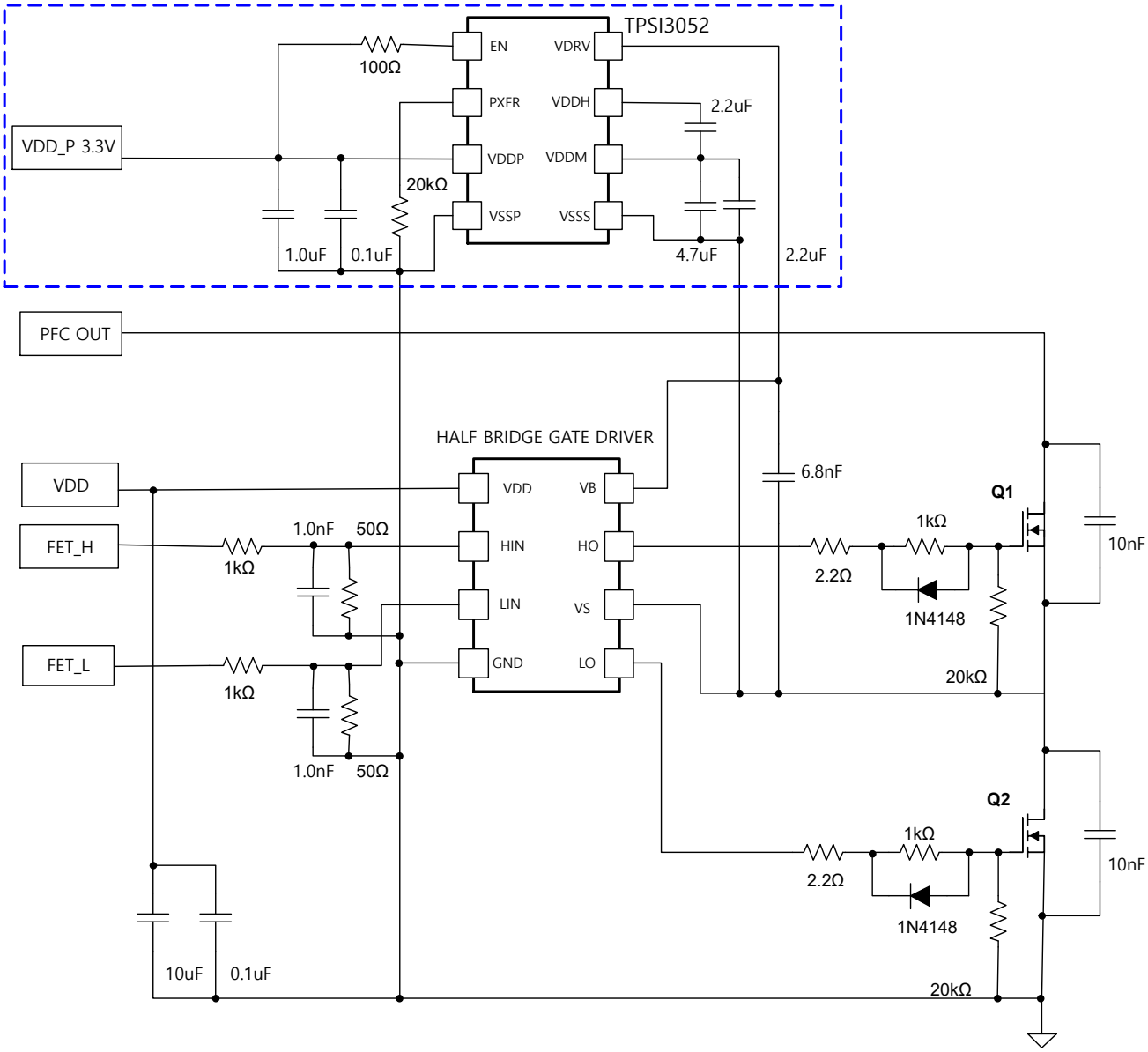
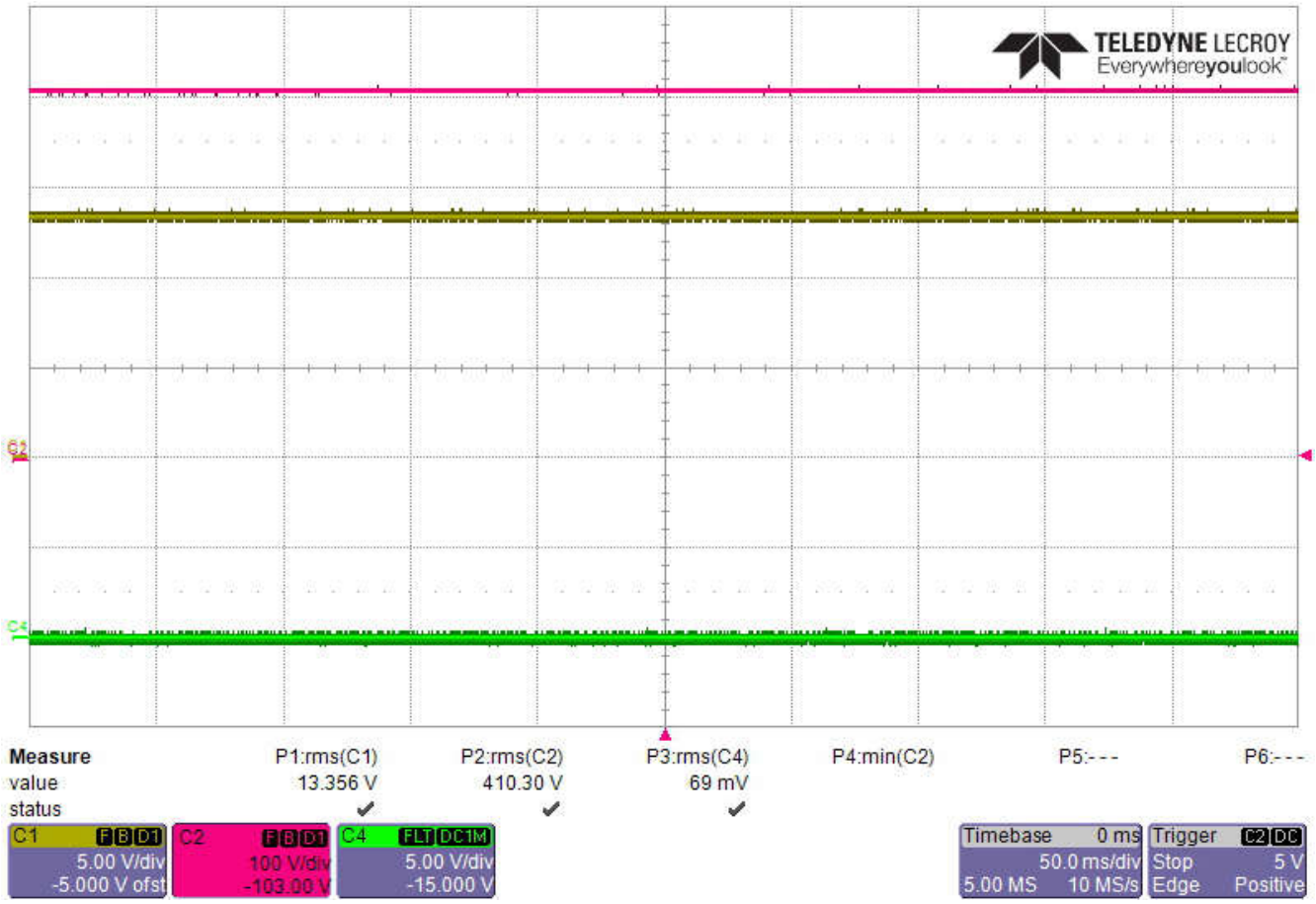


Figure 5-1. Improving Additional Circuit for Operating PFC Slow Switch at High-side (Q1)

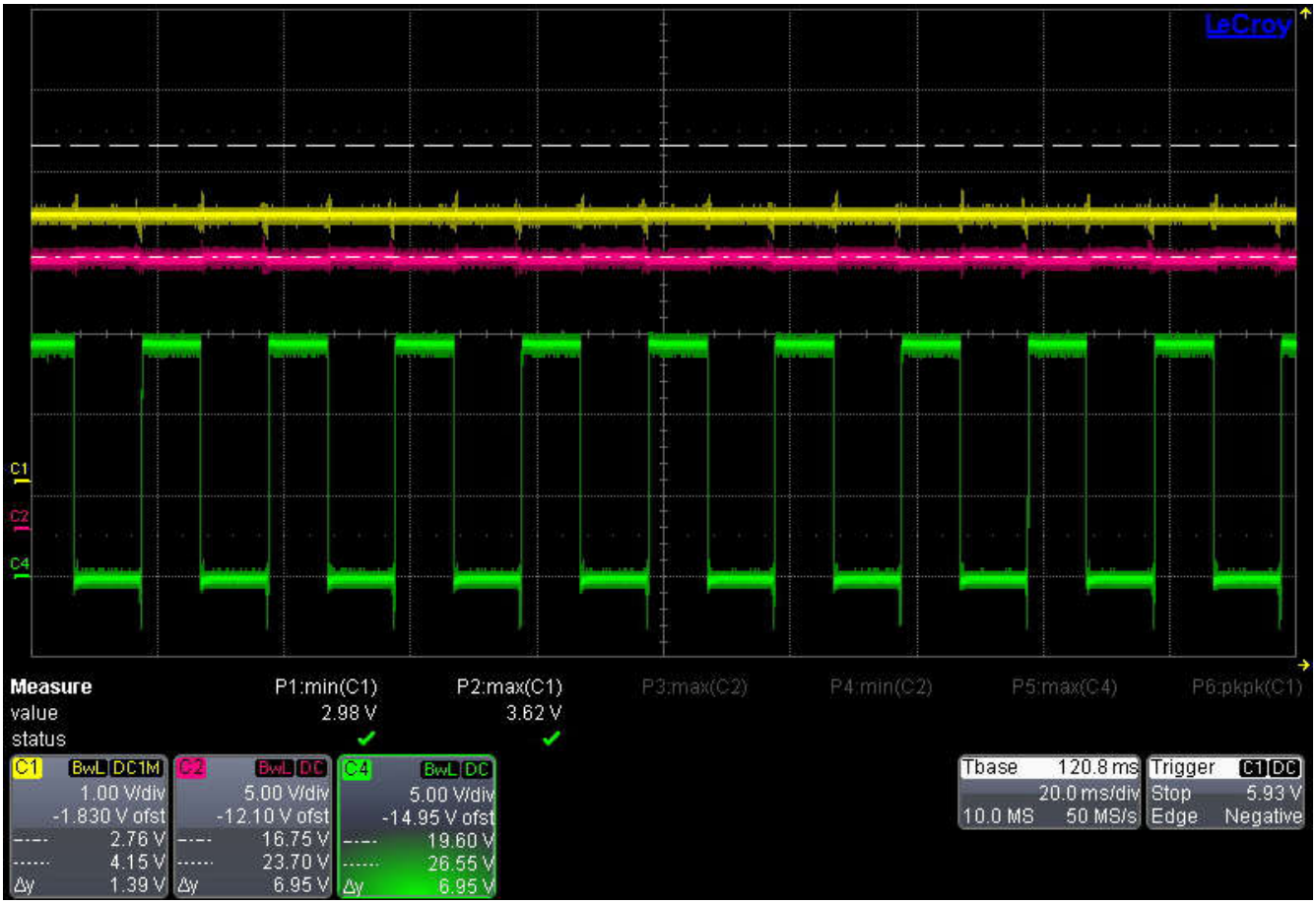
6 Test Results Comparing Before and After for High-side Implementation

Figure 6-1 is the waveform before the change that caused the issue. As a result of adding and operating the improved circuit, the high-side FET (Q1) operates normally as shown in Figure 6-2. The entire system operates normally, and the temperature and efficiency are improved.



A. CH1 (Yellow): VCC_P, CH2 (Red): VB Pin, CH4 (Green): PFC low side Vgs

Figure 6-1. Waveform of Original Circuit for Operating PFC Slow Switch at High-Side (Q1)



A. CH1 (Yellow): 3.3V Input, CH2 (Red): Vdrv Pin, CH4 (Green): PFC low-side Vgs

Figure 6-2. Waveform of Applying Circuit for operating PFC Slow Switch at High-Side (Q1)

7 Summary

This application note describes how to enable operation with DC input voltage (battery), and to solve the issue of when the polarity of the DC input voltage is reversed (live terminal (-) voltage, neutral terminal (+) voltage). The VDD of the driver IC high-side is generated using TPSI3052. The high-side FET operates normally even when the DC input is used.

8 References

1. Texas Instruments, TPSI3052 Isolated Switch Driver with Integrated 15V Gate Supply, data sheet
2. Texas Instruments, Control challenges in a totem-pole PFC, analog design journal

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