Application Note

DC to AC Conversion with DC to DC Buck Converters for PDLC Displays

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ABSTRACT

Polymer Dispersed Liquid Crystals (PDLCs) are materials that combine liquid crystals with a polymer matrix. PDLCs are known for having unique optical properties and are often used in applications such as smart windows, displays and optical devices. Liquid crystals are substances that can flow like liquid but have an ordered structure like a solid. However, what is useful is that PDLCs can change orientation when exposed to an electric field. In the absence of an electric field the liquid crystals are randomly oriented within the polymer matrix which causes light to scatter making the PDLC appear opaque or frosted. When an electric field is applied across the PDLC, the liquid crystals realign along the direction of the electric field. This phenomenon reduces light scattering, allowing more light to get through the material making the PDLC appear clear or transparent.

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1 Introduction

Typical PDLC applications require an AC voltage in the range of 15-100V at 50-60Hz although the exact voltage and switching frequencies heavily depend on material thickness and desired switching speeds. There are many ways to power a PDLC application. The most common way adopts a discrete approach where a microcontroller, high voltage MOSFET drivers and external power stage realize the AC output voltage at the desired frequency. PDLC power stage circuits today are bulky and have high BOM costs. The PDLC dual-buck configuration presented here can replace the old application circuit using fewer, less expensive components. Additionally in the dual-buck configuration, the LM6565X5 is designed to minimize the number of external components by including output capacitors and integrating loop compensation into the power stage buck regulators.

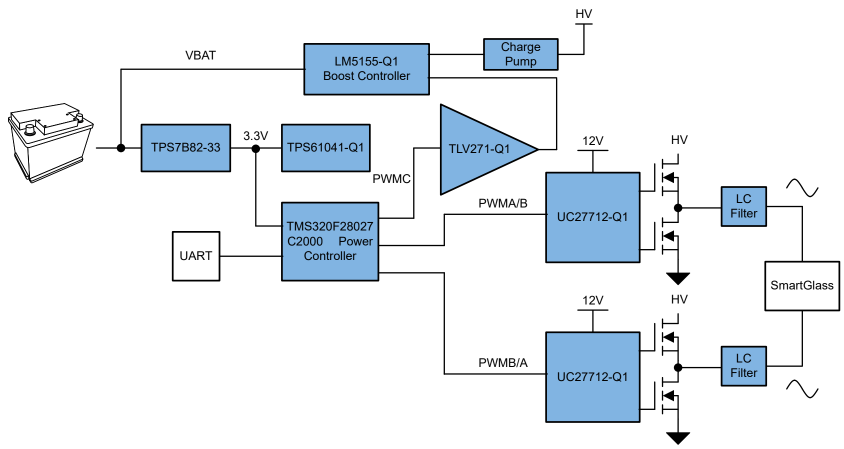

Figure 1-1. Typical PDLC Full Application

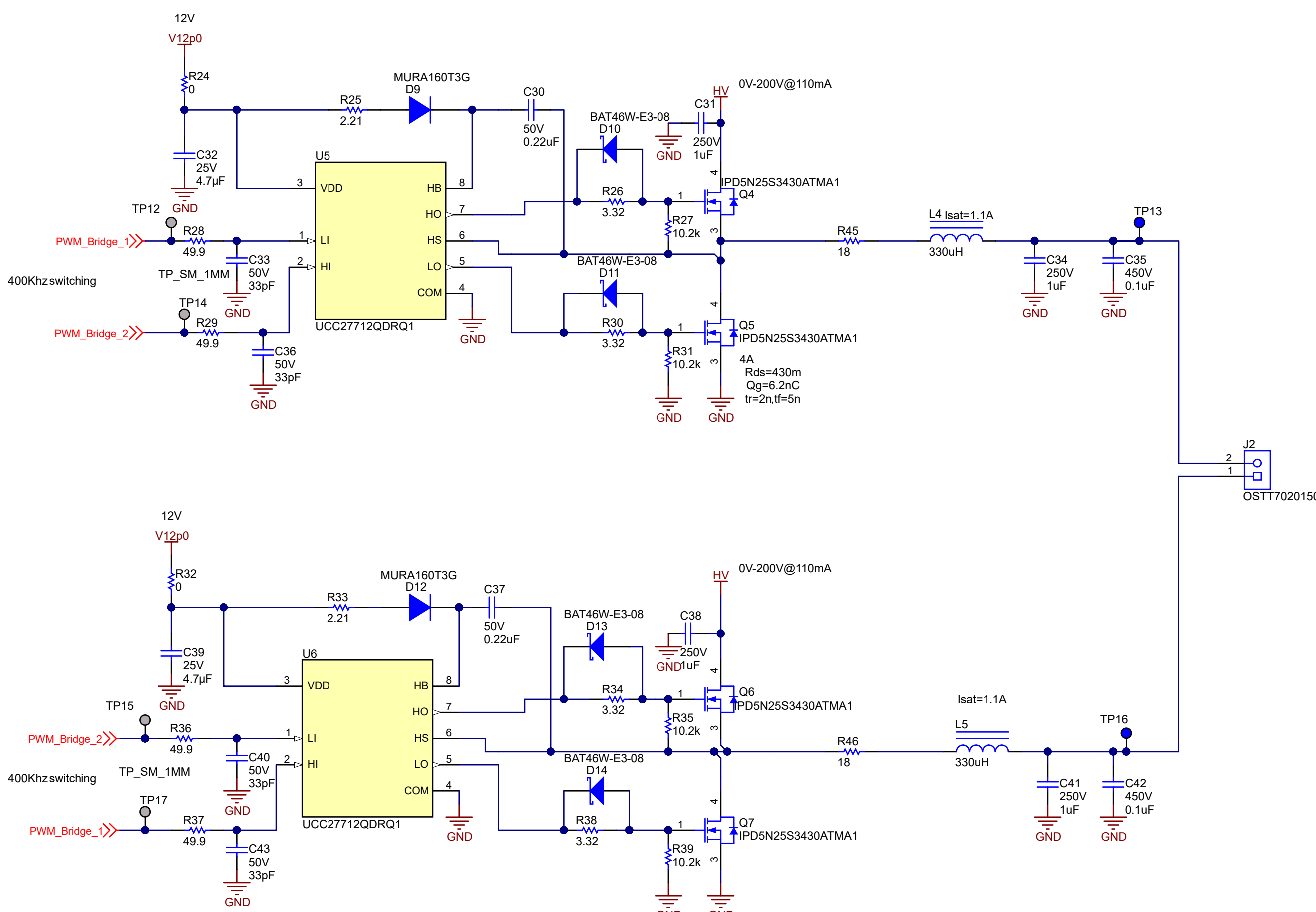

Figure 1-2. Existing PDLC Power Stage with MOSFET DRIVERS

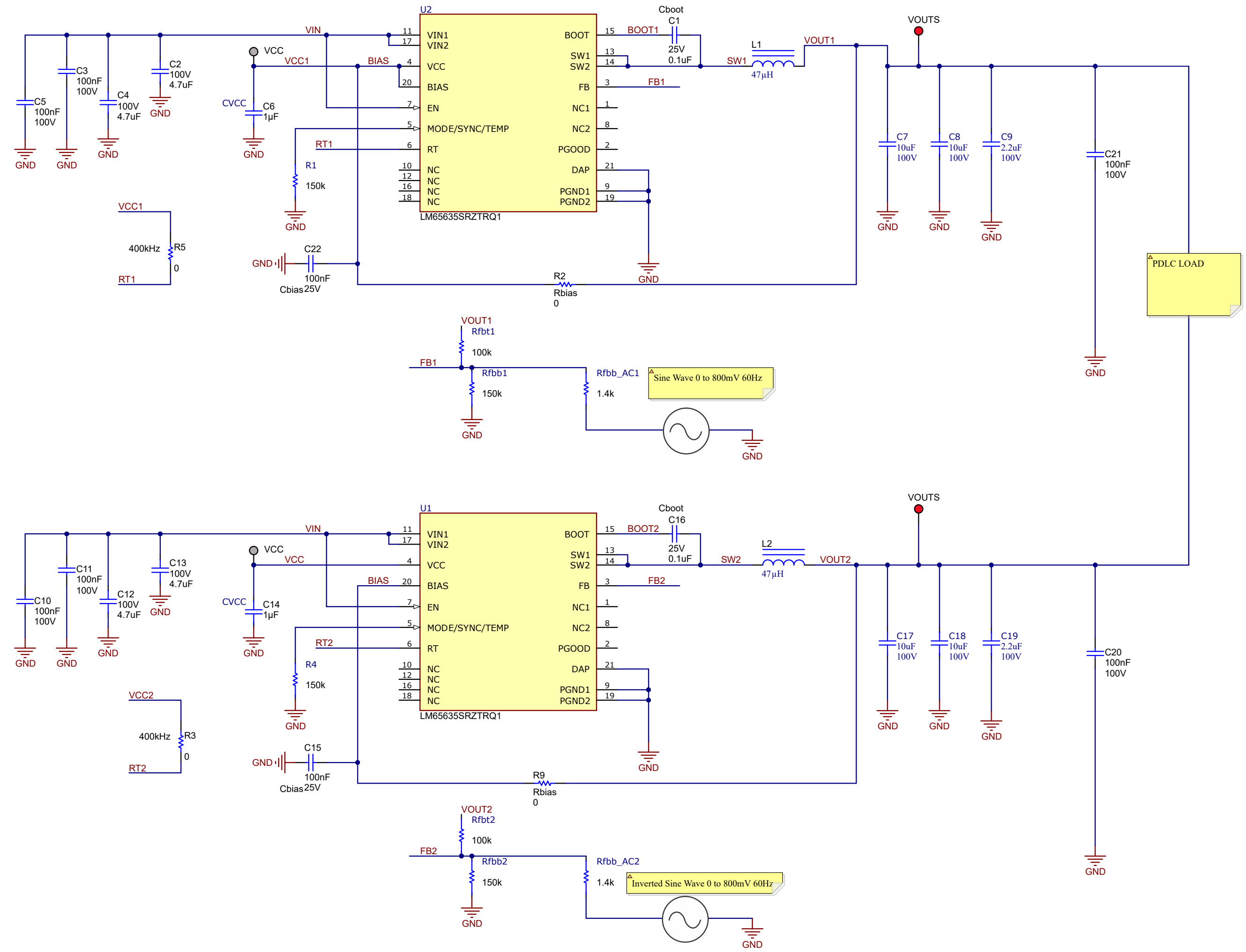

Figure 1-3. PDLC Dual-Buck Power Stage Circuit

2 PDLC Circuit Implementation

For this application the output voltage varies between 1.6V and 57V at 60Hz. One of the main characteristics of the LM65625 is the minimum on-time 35ns (TYP) which allows for low duty cycle conversions at high switching frequencies when the output voltage is low. For this design, 400kHz was selected as operating switching frequency as 400KHz enables a small circuit size while maintaining constant PWM control without folding back the switching frequency. The LM65625 switching at 400KHz can effectively buck at both high and low duty cycles that this application requires during the V_{OUT_PK} and V_{OUT_TROUGH} phases.

The LM65625 Utilizes a peak current control scheme and since the output voltage is a sinusoidal waveform alternating between 1.6V and 57V the effective (RMS) output voltage is V_{OUT_PK} / Sqrt(2) = 40V. Sizing the output components was done with consideration of the RMS output voltage. This avoids the design complexity of over-designing for low and high gain swings on the AC output voltage. However, note that the voltage rating of the capacitor must be compliant with AC V_{OUT_PK}. In this example, 100V rated capacitors were selected. Bucks one and two must have identical circuitry. Counter-intuitively the design of the circuit does not need to follow Equation 1 for V_{OUT_PK} because that can oversize the inductor for this application. Instead, because the voltage is sinusoidally oscillating, the RMS voltage can be used. In testing for this application there were no issues with subharmonic oscillations when either buck had a >50% duty cycle during the 60Hz sinusoidal cycle while switching at 400KHz. At higher frequencies, the minimum on time can be a concern for the low duty cycle required for V_{OUT_TROUGH}. To solve this, to achieve the same magnitude for V_{PDLC_pk}, V_{OUT_TROUGH} and V_{OUT_pk} can be raised by the same magnitude.

$$L_{MIN} \geq 0.47 \cdot \frac{V_{OUT\_rms}}{F_{SW}} \quad (1)$$

A novel approach was implemented using the LM65625 DC-DC converter to generate the AC output voltage for the PDLC. Two buck converters are connected in a bridge configuration to supply the PDLC. The feedback networks of each converter are fed with 60Hz sine waves, 180° out of phase. In this way, a ± 57V peak A.C. sine wave is generated across the display, providing about 40Vrms at 2A. Two LM65625 buck ICs were used to generate the sourcing and sinking requirements to power a 80W PDLC. The sine waves were generated by a function generator for this example, but 60Hz sine waves can be generated using any DAC sine wave generator such as the one from the TMS320F28027 microcontroller.

Figure 2-1 shows the simplified PLDC application using LM65625-Q1.

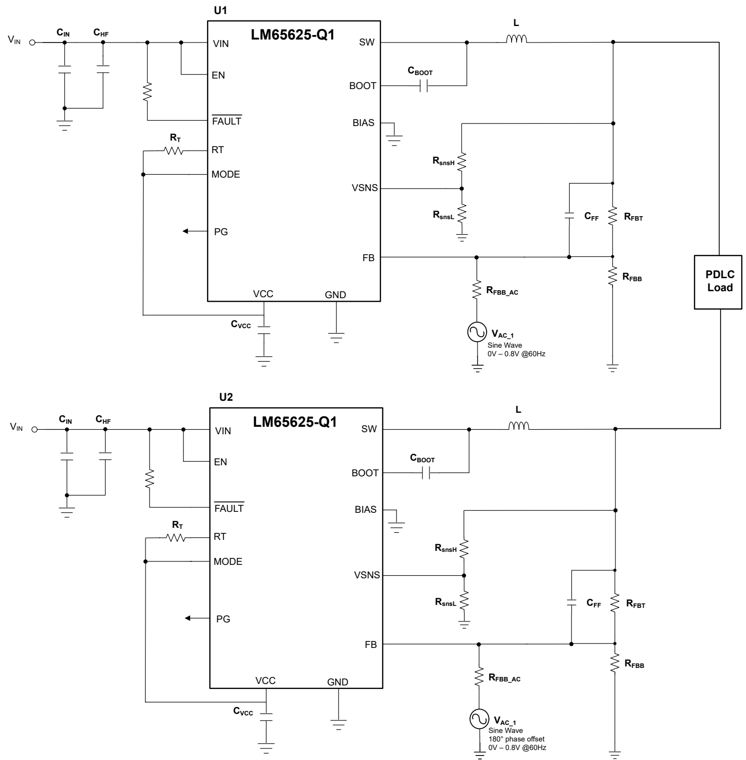

Figure 2-1. Application Schematic

A 47uH (XGL6060) inductor was chosen which allowed for stable and reliable design without compromising circuit size. For C_{OUT}, 22uF effective output capacitance was required. 2 x 10uF + 2.2uF MLCC output capacitors were selected using the equations below. I was set to 0.8A (30% of the full load), and again the rms value of VOUT is used where applicable.

$$V_R \cong \frac{\Delta I}{8 \cdot F_{SW} \cdot C_{OUT}} \tag{2}$$

$$\Delta I \cong \frac{\left(V_{IN} - V_{OUT\_rms}\right) \cdot V_{OUT\_rms}}{V_{IN} \cdot F_{SW} \cdot L} \tag{3}$$

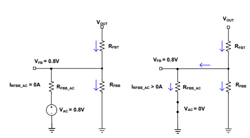

Figure 2-2. Feedback Circuitry

The AC output waveform comes from the AC voltage applied on the FB voltage. Figure 5 shows how current flows through the feedback divider system to generate the V_{OUT_TROUGH} and V_{OUT_pk} for the system. As the AC signal decreases the current flowing through the AC resistor increases and the effective VOUT decreases. The buck regulator essentially acts as an amplifier for the smaller signal to become an AC voltage source. Below are a series of equations for how to set the values for the feedback resistor circuitry. V_{PDLC_pk} is a system parameter set by the specification for the specific application. Generally, 100Kohm is a robust value to choose for R_{FBT}. The V_{REF} for LM65625 is 0.8V, but that value can vary from buck to buck.

$$V_{PDLC\_pk} = V_{OUT\_pk} - V_{OUT\_trough} \tag{4}$$

$$R_{FBB} = R_{FBT} \cdot \frac{V_{REF}}{V_{OUT\_trough} - V_{REF}} \tag{5}$$

$$R_{EQ} = R_{FBB} \,||\, R_{FBB\_AC} \quad (6)$$

$$R_{EQ} = R_{FBT} \cdot \frac{V_{REF}}{V_{OUT\_pk} - V_{REF}} \quad (7)$$

$$R_{FBB\_AC} = \frac{V_{FBB} \cdot R_{EQ}}{V_{FBB} - R_{EQ}} \quad (8)$$

Below shows the output waveforms of the output voltage from the bucks as well the inductor current. The design provides a stable 60Hz output voltage. Simulation software such as SIMPLIS is useful for providing quick results and for quickly checking if the design is stable.

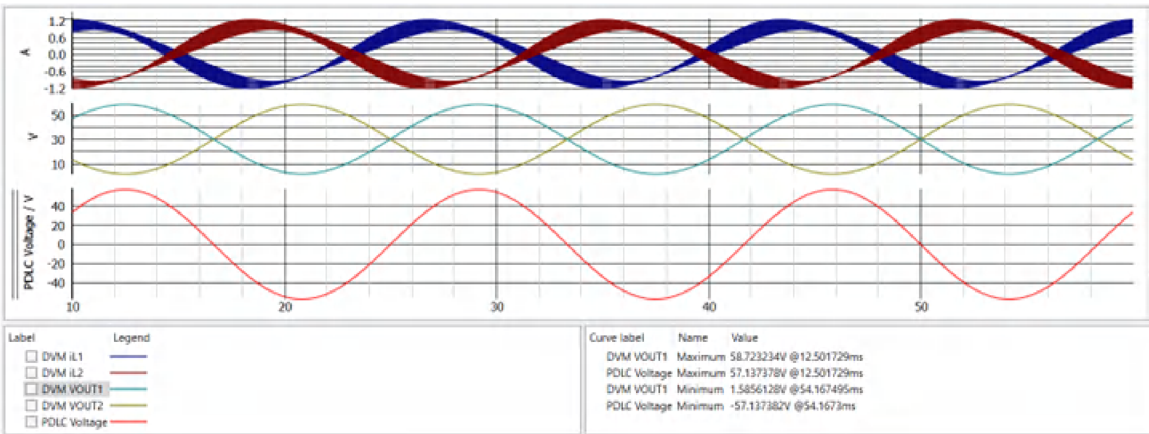

Figure 2-3. Simulation Results

The application circuit was also verified to work in the lab. Two LM65645EVMs and a function generator were configured to test the design. Figure 2-4 shows that this type of topology can generate the PLDC's required 60Hz voltage.

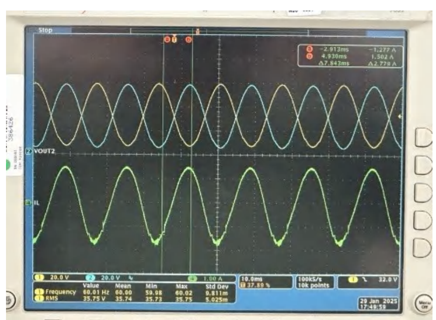

Figure 2-4. Lab Results

3 Summary

Based on the analysis and assessment of the PDLC dual-buck application circuit, the following conclusion can be made. The Dual Buck application circuit is lower-BOM, due to the integration of drivers and MOSFETs than the typical PDLC application circuit. The 35nS minimum on-time of the LM656x5 allows for high frequency operation and a large conversion ratio required to obtain the maximum AC voltage swing for a given input voltage. The buck application circuit also has a higher power density and higher FIT rate due to reduce component count. If a lower output current is required, a smaller current device such as the LMR604X0 can be used for this type of application.

4 References

Texas Instruments, *Automotive SPD-SmartGlass™ Driver Reference Design*, design guide.

Texas Instruments, *Understanding and Applying Current-Mode Control Theory*, application note.