Application Note

Single Cell Battery Charger Applications with Dual Sources

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ABSTRACT

Many applications require the use of two independent power sources as the input for a Texas Instruments single cell battery charger IC. Some of TI's multicell battery charger ICs have dual input features and can be used in a single cell application however these are generally larger and more expensive. This application note presents alternative designs that in most applications are more cost effective and feature a smaller footprint.

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1 Introduction

There are several circuit topologies that can be used to design a dual input battery charger system. This application note methodically explores the use of a power mux in combination with a single cell battery charger IC. The document also discusses a number of other possible designs including two parallel chargers, a multicell charger with dual input functionality, and the use of eFuses.

The power mux design is likely the most simple to implement and is preferred for a variety of applications, however each of the following designs has a place in certain applications. The advantages and disadvantages of each architecture are discussed thoroughly including a comparison of the prices for a particular example of each design presented.

2 Possible Architectures

2.1 Power Mux

The example presented uses the TPS2121 power mux and the BQ25638 battery charger IC. The circuitry interfacing the two devices is simple: connect the OUT pin of the power mux to the VBUS pins of the battery charger IC.

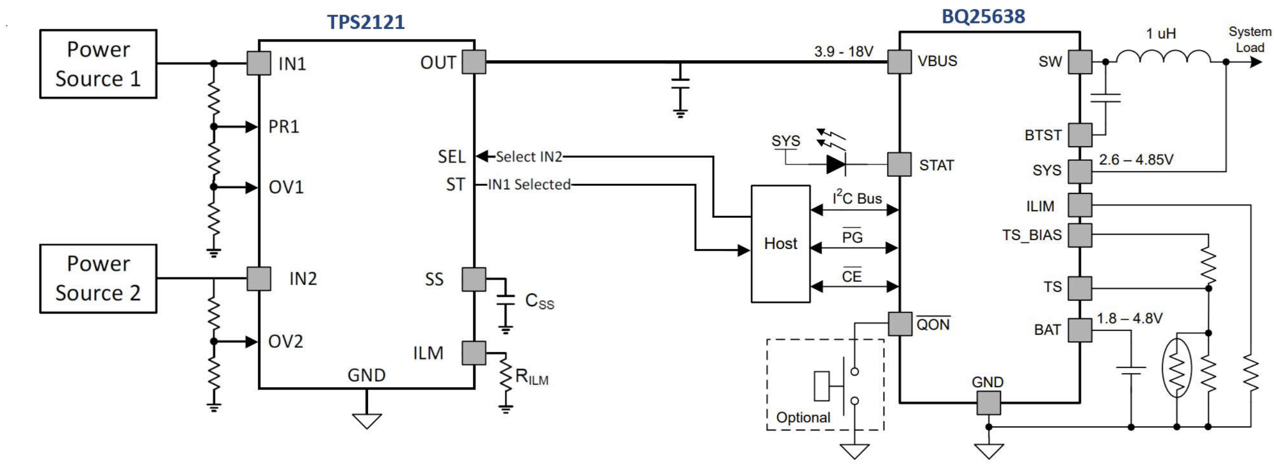

Figure 2-1. Power Mux System Diagram

Pay special attention to the input capacitor for the BQ25638. In this application selecting a larger capacitor than is normally selected when the charger IC is connected directly to a power supply can be helpful. This helps hold up the input voltage to the battery charger IC during a power mux switch-over. The BQ25638 data sheet recommends using a 1uF capacitor and this is likely large enough in the case of the TPS2121 which has a fast switch over time of 5us. In contrast, for other power mux ICs such as the TPS2120, which has a 100us switch over time, a larger capacitor must be selected. The particular value must be selected based on the current draw of the specific application and sensitivity to voltage dips. The voltage dip can be found using Equation 1

$$V_{DIP} = t_{sw} \times \left(\frac{I_{out}}{C_{out}}\right) \quad (1)$$

2.1.1 Other Power Mux Considerations

The TPS2121 maximum input voltage and current characteristics meet or exceed those of the BQ25638 meaning that the inclusion of the power mux does not limit any features of the BQ25638. However, at high input currents, such as the 3.2A maximum of the BQ25638, the resistance across the power mux results in a significant voltage drop across the power mux.

ON-RESISTANCE (INx to OUT)						
R_{ON}	ON-State Resistance (TPS2120)	I_{OUT} = -200 mA $V_{PRI} > V_{REF}$ $V_{INx} \geq 5.0$ V	25°C	62	75	mΩ
			-40°C to 85°C		90	mΩ
			-40°C to 105°C		100	mΩ
			-40°C to 125°C		120	mΩ
	ON-State Resistance (TPS2121)	I_{OUT} = -200 mA $V_{PRI} > V_{REF}$ $V_{INx} \geq 5.0$ V	25°C	56	70	mΩ
			-40°C to 85°C		85	mΩ
			-40°C to 105°C		90	mΩ
			-40°C to 125°C		100	mΩ

Figure 2-2. Typical and Maximum Resistance values for the TPS2121 and TPS2120

This voltage drop can be of concern in applications using linear or buck only charging ICs (including the BQ25638), where the battery regulation voltage approaches the input voltage. For example, in the common case of a 4.2V Li-ion cell and a 5V USB source there is only a 0.8V of headroom even before considering the impedance of the power source and the dropout voltage required by the charging device.

If lower resistance is required, similar functionality can be accomplished with dual eFuses from TI's large catalog of eFuses. However, if the full voltage range of the charger IC is not required the TPS2117 power mux with a voltage limit of 5.5V and current limit of 4A can be used. This device has a typical on-resistance of only 20mΩ and a lower cost.

2.1.2 Power Mux Over Voltage and Priority Settings

The TPS2121 and TPS2120 have a number of different functional modes, allowing the system designer to configure different source selection operations. These various functional modes are set using different values of resistors, and are described in depth in section 9.4 of the TPS212x data sheet. This is particularly important when switching between different voltage levels. In addition, this must be carefully considered if using a USB-PD source where the voltage can change as different voltage levels are requested.

2.1.3 Power Mux Testing

This method was tested using the BQ25638 and TPS2121 evaluation modules. The modules were connected using the output screw terminal of the TPS2121 EVM and the VBUS input of the BQ25638 EVM. Using the ICHG register the BQ25638 was set to produce a charge current of 1.04 amps, to simulate a battery the charger was connected to a source meter set with a potential of 3.7V. In addition the system output was connected to an electronic load set to consume another 0.5A. The two TPS2121 inputs were connected to DC power supplies set to output 12V.

Figure 2-3. Test One, 0uF Added Capacitance, Nominal Load

In this first test, there is no added capacitance on the node between the power mux and charger IC. Input 1 (not shown) is set to 12V and is actively powering the BQ25638, the DC power supply on input 2 (IN_2), the priority input, is then switched on. At approximately 4ms on the waveform the TPS2121 switches over and there is a significant drop in the system voltage to 3V. In addition, there is significant spike in the input voltage to nearly 15V.

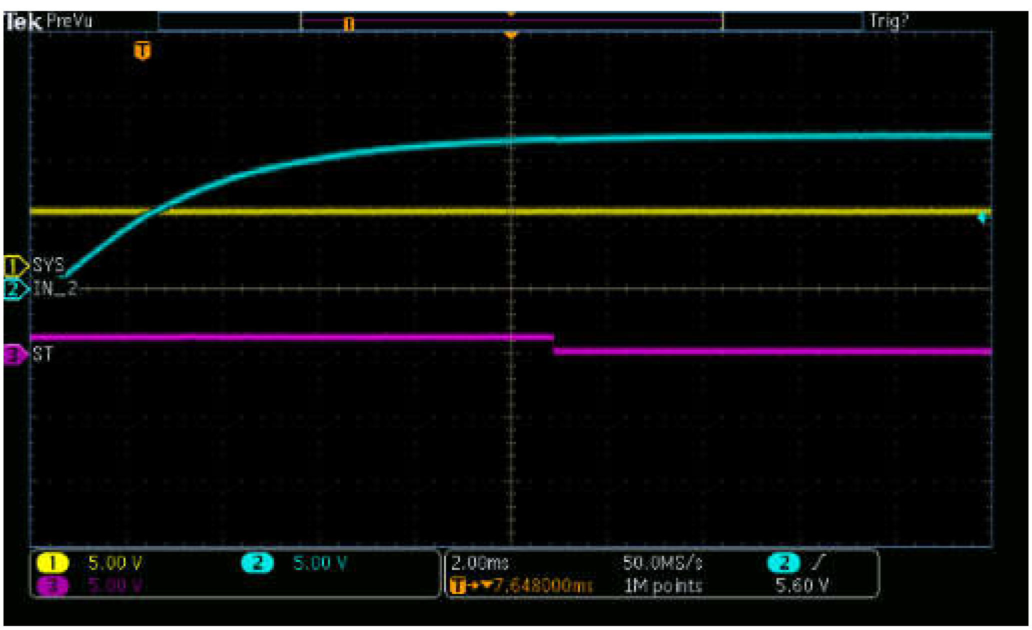

Figure 2-4. Test Two, 10uF Added Capacitance, Nominal Load

The same test is preformed in this waveform with the addition of a 10uF capacitor on the node connecting the two devices. This eliminates the drop-in system voltage, and spike in input voltage.

Figure 2-5. Test Three, 0uF Added Capacitance, Nominal Load

The same test is performed here (without added capacitance), and with the yellow waveform representing the connection node voltage (VBUS). The connection node voltage drops to nearly 2.5V

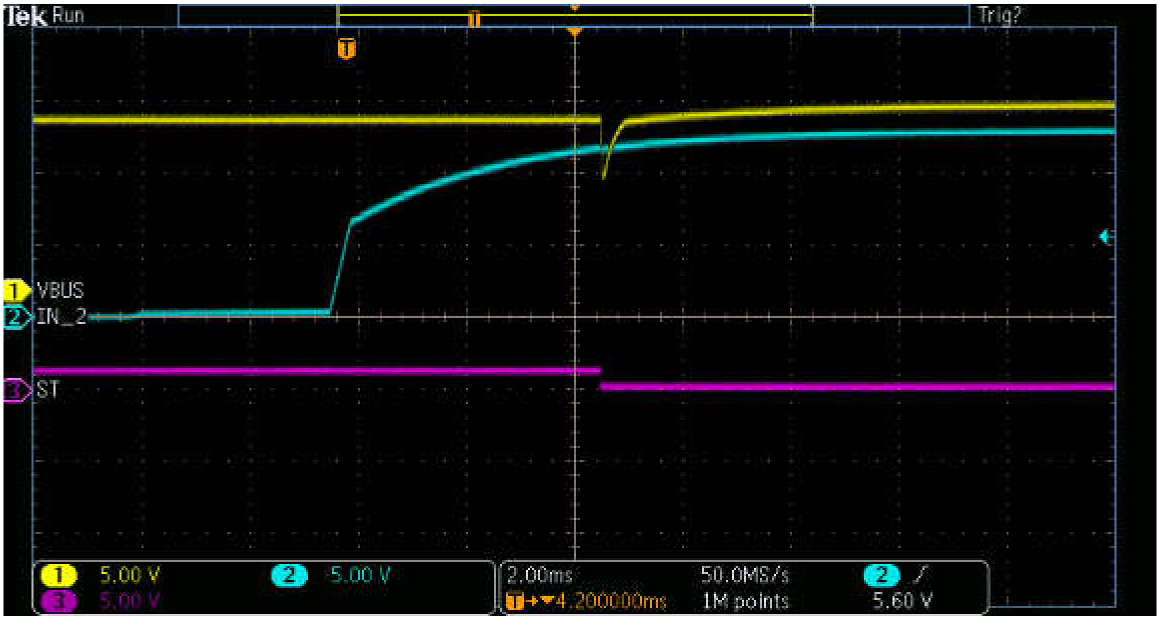

Figure 2-6. Test Four, 10uF Added Capacitance, Nominal Load

The same test is performed here with the 10uF capacitor, and with the yellow wave form representing the connection node voltage (connection between the TPS2121 output and BQ25638 VBUS). The connection node drops in voltage to a much more reasonable 7.5V. This can be improved further with a larger capacitor and can be required when drawing increased current from the device.

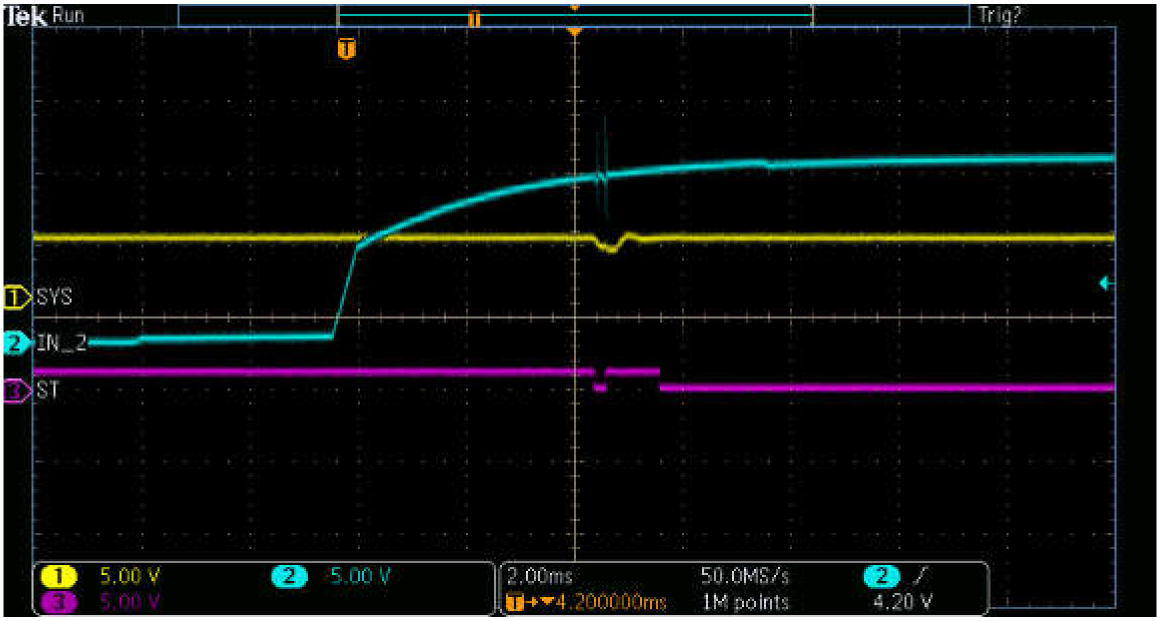

Figure 2-7. Test Five, 0uF Added Capacitance, 3A Output Current

Figure 2-8. Test Six, 100uF Added Capacitance, 3A of Output Current

These two tests were run under much greater load conditions, and required much higher capacitance values on the TPS2121 output node. In this waveform, there is a drop in system voltage, as well as the significant oscillations in the input waveform.

The voltage drop across the TPS2121 was also tested while drawing two amps at 12V from the TPS2121 with the electronic load. The voltage drop is approximately 0.11V closely following the 56mΩ listed on resistance

2.2 Multicell Charger IC

Another method of using dual sources in a battery charging application is the use of one of TIs multicell battery charger ICs with dual input selector (BQ25798, BQ25672, BQ25692). Note that the BQ25692 has a much higher minimum input voltage of 6V compared to the 3.6V-3.9V for the other products presented making the devices not preferred for many single cell applications.

The implementation of the dual input feature is well documented in the data sheets of the respective devices and recommendations for the external FETs required for this feature can be found in the EVM user guides for the ICs.

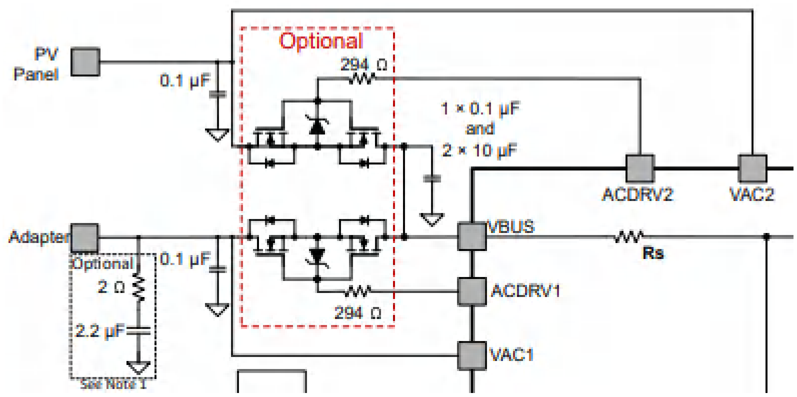

Figure 2-9. Section of the Application Diagram

2.3 Dual Chargers

For this example, the BQ25638 is used along with a BQ25186 linear 1A battery charger IC. In this application each of the two sources are connected to the respective charger ICs, the battery (BAT) pins of each IC are again shorted to each other and connected to the battery and the system output of the switching charger is connected to the system load.

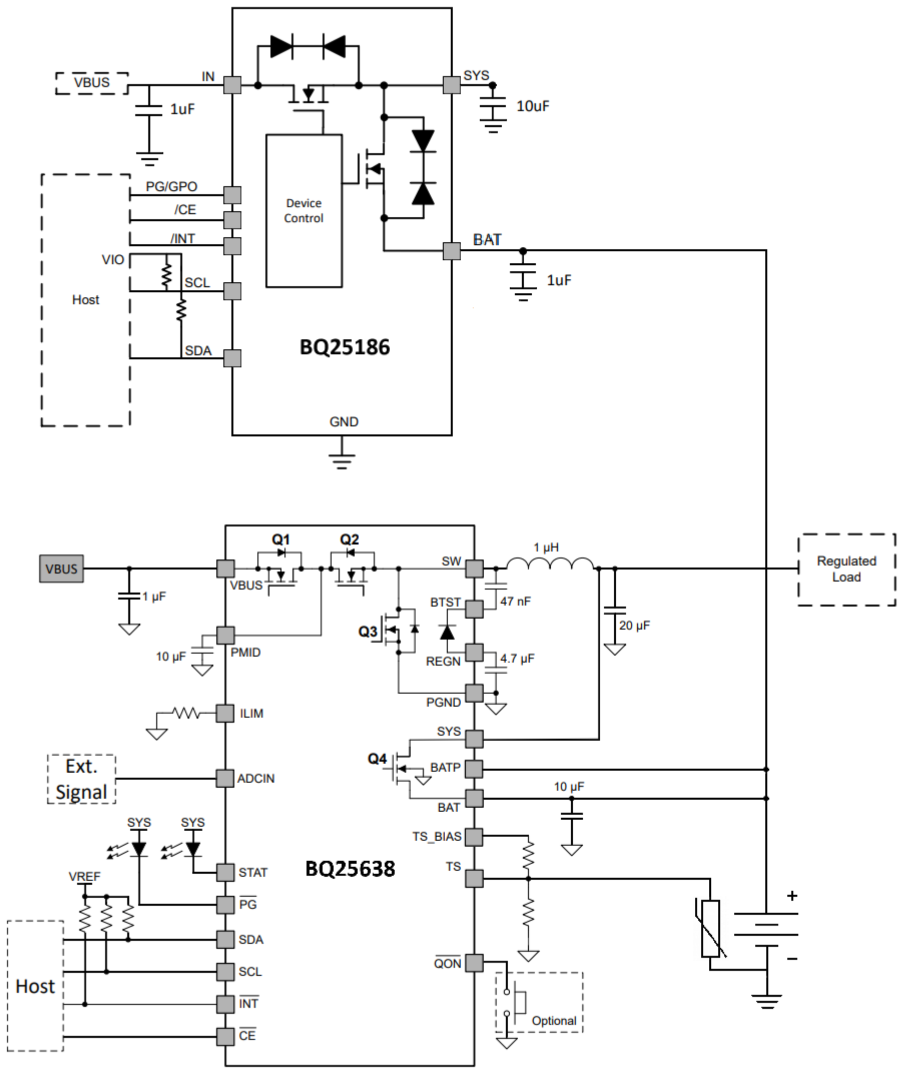

Figure 2-10. Parallel Chargers Block Diagram

While a system designer can connect the system outputs of both devices to the system load, this comes with relatively complex control implications, and we recommend the configuration shown in Figure 2-10. This configuration still allows for the linear charger current to contribute to the system load though the BATFETs of both devices. This comes with the obvious disadvantage the increased resistance by going through both BATFETs. If the system designer still wants to connect both chargers with BAT and SYS outputs in parallel, the system designer must make sure that the BATFET of the non charging device is not active. This can be accomplished a few ways but if not done properly can result in damaging one or both of the charging ICs

While less critical then the above considerations regarding the system output, TI recommends that the host processor control the chargers so that even if the system and the host both have valid inputs only one is actively charging. The chargers being active simultaneously does not cause any damage to the system. However each of the charge currents adds to each other and the system designer must make sure that if this functionality is desired that the combined charge currents do not exceed the rated charge current of the battery.

Make sure that the proper output capacitors are placed close to there respective ICs, especially for the switching charger, as the 20uF capacitance shown in the application diagram plays a key role in the buck converter circuit. In addition the I2C lines can also be tied together as the devices have different I2C addresses (0x6A for the linear charger, and 0x6B for the switching charger). In addition the interrupt pins can also be wired together as the interrupt pins are both open drain outputs.

2.4 eFuses (USB OTG)

As most TI power muxes do not allow for reverse current, the USB OTG feature which allows the battery charger IC to boost the battery voltage and act as a power source is not available. This can however be accomplished using two eFuses. In most dual source applications both sources are not USB OTG ports, and as a result, for greatest cost effectiveness a unidirectional eFuse must be used for the non-USB OTG source, while a bidirectional eFuse is used for the USB OTG port.

The parts selected for this example are the TPS25948 bidirectional eFuse and the LM7310 unidirectional eFuse. The TPS25948 typical application diagram in the data sheet features the use of two of these eFuses along with a battery charging IC.

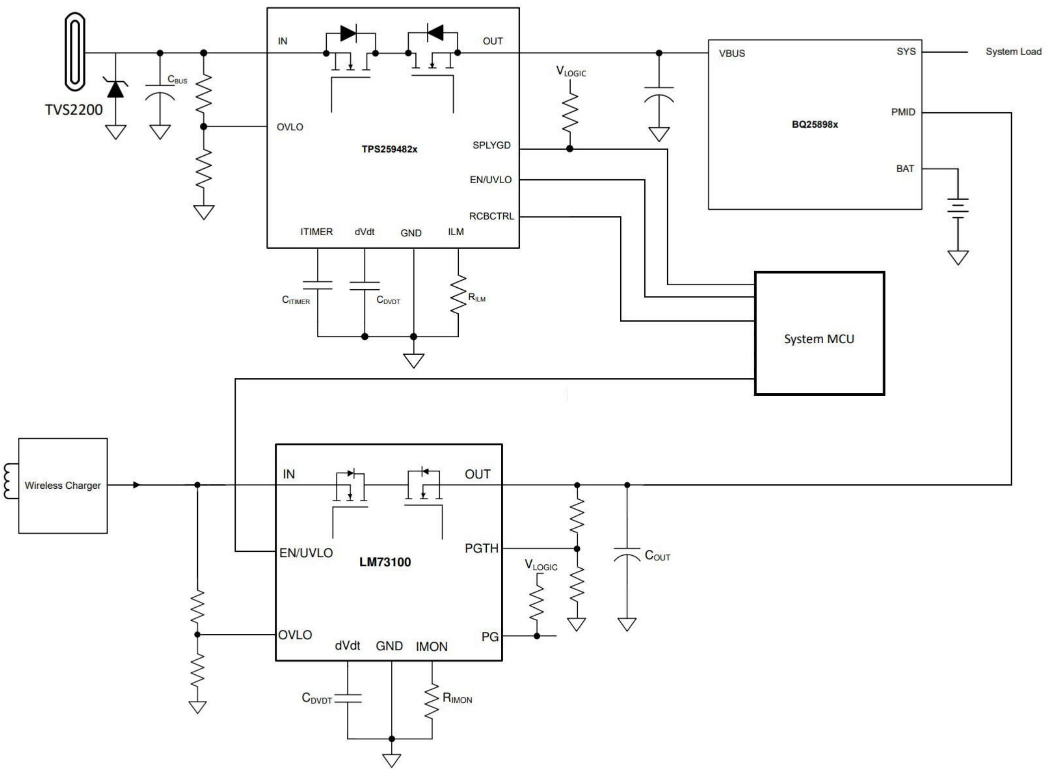

Figure 2-11. Application Diagram for Dual Source Using eFuses

One feature of note is the connection of the second eFuse output to the PMID pin of the battery charger IC. The PMID pin provides a direct connection to the node between the back to back FETs in the battery charger IC and is usually used for an additional decoupling capacitor. Note that for some chargers the OTG output must be taken from the PMID pin (for example, BQ2589x) while on other chargers the OTG output must be taken from VBUS (for example, BQ25638).

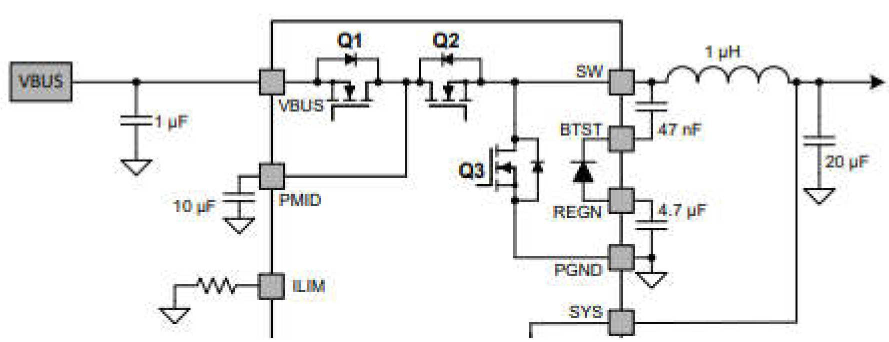

Figure 2-12. Section of the Application Diagram

3 Summary

Table 3-1. Architecture comparison

Topology	Power Mux	Power Mux	Dual Chargers	Multi-Cell	E-Fuse
Charger	BQ25638	BQ25622E	BQ25638 + BQ25186	BQ25798	BQ25638
Input control	TPS2121	TPS2116	None	4x CSD17581	TPS25948+ LM3710
Price	$2.10	$1.25	$2.12	$2.53/$2.08	$2.29
Combined Footprint	9.8mm²	10. 86mm²	9.8mm²	136mm² /20.7mm²	13.16mm²
Additional Control	None	None	Active	None	Active

The comparison table above represents a number of possible designs each with advantages and disadvantages. The prices use 1k quantity prices from TI.com where available. The first two designs presented are based around the power mux topology that is explored thoroughly in the first part of the application note.

The first design presented uses the BQ25638 and TPS2121 which makes sure the system designer can use the full range of the charging ICs capabilities including the maximum input voltage of 18V and maximum input current of 3.2A. The power mux design also requires very few additional passive components, depending on the features required this can be limited to only a few small resistors.

The second power mux design intends to showcase a more cost-conscious design, using a different charger IC, which has many of the same features including a charge current of 3.2A with the main differences being a larger package (QFN type), lower max input voltage, and higher resistance BATFET. In addition, a different power mux is selected for this design to reduce cost. This power mux however has lower specifications than the charger limiting input current and voltage to 2.5A and 5.5V. In addition some input protections can be required to protect the rest of the circuit from higher voltages.

The dual charger design provides a unique advantage in applications where the two input sources benefit from two different charger topologies. For example if one input is relatively low power, such as a small solar cell a low specification linear charger can be selected for that input, and a different switching charger can be selected for the other input. This allows the system designer to minimize cost by selecting a charger with the specifications required only for each input.

The fourth design uses one of TIs multicell chargers which when combined with four FETs provides dual source capabilities. Two footprints and prices are provided for this design, the first of each describes the cost and footprint when using the FETs described in the EVM for the charging chip. The second shows the cost and footprint when using the CSD13385F5 FETs from TIs FemptoFET line. The original FETs have much greater current and voltage ratings than is required in most single-cell charging applications. To create a more cost and footprint competitive system, TI recommends selecting new FETs based the application requirements.

The last design is applicable in USB OTG applications where the device is being used as a power source. In addition, the eFuses have the advantage of having very low on resistance when compared to the power mux designs. The main disadvantages are the footprint as this design uses three independent ICs and the requirement for increased host interaction to control which fuse is active.

4 References

Texas Instruments, *TPS212x 2.8-V to 22-V Priority Power MUX with Seamless Switchover*, data sheet.

Texas Instruments, *BQ25638 I2C Controlled, 5-A, Maximum 18-V Input, Charger with NVDC Power Path Management and USB OTG Boost Output*, data sheet.

Texas Instruments, *BQ25622E I2C Controlled 1-Cell, 3A, Maximum 18V Input, Buck Battery Charger with NVDC Power Path Management*, data sheet.

Texas Instruments, *TPS2116 1.6 V to 5.5 V, 2.5-A Low IQ Power Mux with Manual and Priority Switchover*, data sheet.

Texas Instruments, *BQ25186 1-Cell, 1A I2C Linear Battery Charger with Power Path, Ship Mode, Shutdown Mode, and Battery Tracking VINDPM*, data sheet.

Texas Instruments, *BQ25798 I2C Controlled, 1- to 4-Cell, 5-A Buck-Boost Battery Charger with Dual-Input Selector, MPPT for Solar Panels and Fast Backup Mode*, data sheet.

Texas Instruments, *CSD17581Q5A 30-V N-Channel NexFET™ Power MOSFETs*, data sheet

Texas Instruments, *LM73100, 2.7 - 23 V, 5.5 A Integrated Ideal Diode with Input Reverse Polarity and Overvoltage Protection*, data sheet.

Texas Instruments, *TPS25948xx 3.5V–23V, 12.2mΩ, 8A eFuse With Bi-directional Power Delivery*, data sheet.

Texas Instruments, *CSD13385F5 12-V N-Channel FemtoFET™ MOSFET*, data sheet