Application Note

A Designer's Guide to Class-H Implementation in TAS5815, TAS5825P, TAS5827, TAS5828M, and TAS5830 Amplifiers

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ABSTRACT

The TAS58xx family of devices from Texas Instruments are dual-channel, digital input Class-D audio amplifiers that can drive 10 W - 150 W speakers, providing the power and flexibility needed for a wide range of audio applications. Various devices in this family include a Class-H algorithm for external DC-DC converters to optimize efficiency without compromising sound quality. By dynamically adjusting the PVDD power supply voltage to follow the audio signal, Class-H technology reduces heat dissipation and minimizes power consumption by reducing switching and conduction losses. Whether you're designing a high-fidelity home audio system or a portable Bluetooth speaker, the TAS58xx Class-H feature ensures that your customers will enjoy rich, detailed sound with minimal distortion - all while keeping power consumption and thermal generation to a minimum.

This document provides guidelines for integrating the Class-H feature in the TAS58xx devices, covering the internal algorithm, external hardware requirements, and the use of PurePath™ Console 3 (PPC3) software.

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1 Introduction

The audio amplifier market is increasingly adopting Class-D technology due to the rising power levels required by audio systems, limited space available for thermal dissipation, and tighter power consumption requirements. As the number of speakers grows and maximum power rail voltages increase, the power dissipation in the amplifier also increases resulting in even higher thermal levels, posing a significant challenge. To address this issue, power rail envelop tracking has emerged as a popular technique to enhance system-level efficiency. This allows audio systems to deliver the same powerful sound while prolonging battery life and minimizing heat generation.

Typically, audio systems operate with one voltage rail that can satisfy the system's maximum peak power specification. Since music is dynamic, this high voltage rail is only required for infrequent short bursts. Operating at this high voltage rail outside of those peak power levels results in significant losses without any benefit. More specifically, this inefficiency is due to switching and conduction losses. From a system level, operating at the max voltage rail only will result in poor battery life and higher operating temperatures. By implementing an envelope-tracking power-supply system, these system challenges can be effectively addressed. This approach involves analyzing the input audio signal to determine the optimal supply voltage level, and then dynamically adjusting the DC-DC converter's output voltage to match the audio signal's needs in real-time. Unlike traditional systems that maintain a constant voltage based on the peak power requirement, this approach ensures that the power supply voltage is always tailored to the specific demands of the audio signal without impacting THD. As a result, switching and conduction losses are significantly reduced, leading to substantial improvements in efficiency and thermal performance.

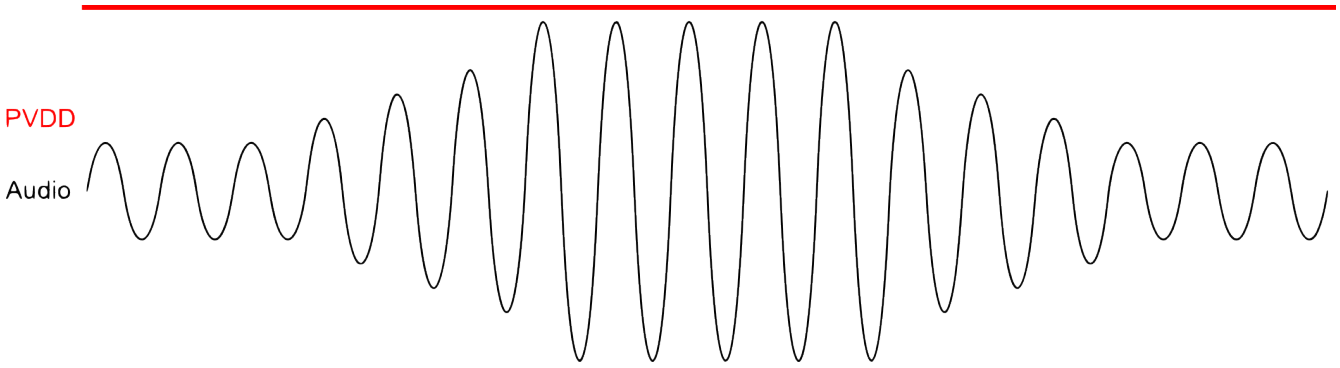

Figure 1-1. Figure 1: Class-H Disabled

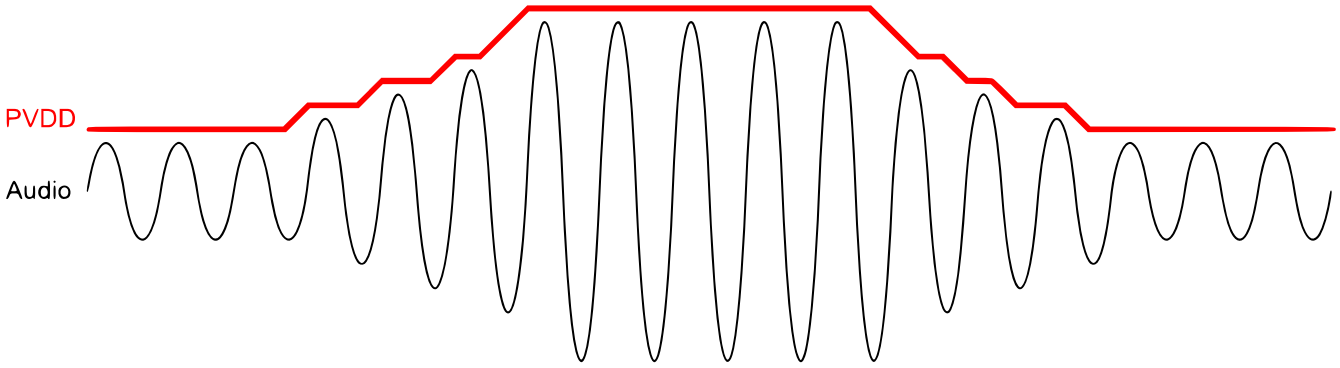

Figure 1-2. Figure 2: Class-H Enabled

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2 Detailed Description

Of the TAS58xx family, TAS5815, TAS5825P, TAS5827, TAS5828M, and TAS5830 support the Class-H algorithm in either BTL (stereo) or PBTL (mono) configuration. Overall, the algorithm works by generating a PWM signal that is ultimately used to control the amplifiers PVDD voltage. This algorithm is run inside the TAS58xx amplifier's DSP and used to control an external DC-DC converter. The block diagram view of the amplifier and DC-DC converter can be seen in Figure 2-1. This PWM signal from the TAS58xx amplifier is generated based on the audio signal post DSP processing. The duty cycle of the PWM signal will dynamically adjust based on the audio signalls level. The PWM signal is then passed through an external passive filter to become a current varying source forced on the DC-DC converter's feedback pin. This feedback pin is always fixed at one specific voltage, so injecting additional current forces the converter to compensate by adjusting its output voltage. Since the DC-DC converter is supplying the amplifier's PVDD voltage, the amplifier can then dynamically adjust its PVDD supply by adjusting the PWM signal.

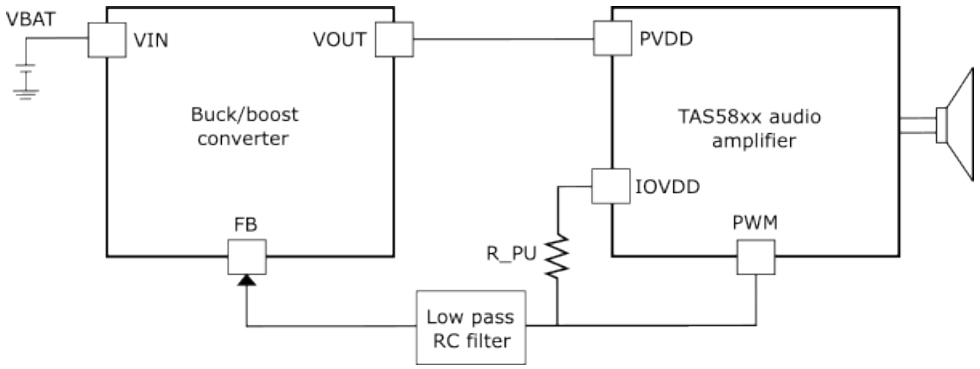

Figure 2-1. Single Device Class-H Block Diagram

The TAS58xx Class-H algorithm can also be utilized across multiple TAS58xx devices with one boost converter. When the GPIOs are tied together, they operate as a logic OR gate. In this case, the PVDD voltage will be the highest level required across all the amplifiers. This allows PVDD to be optimized for the system, while not compromising on board space and cost. To connect various TAS58xx Class-H PWM signals together, the PWM pins must be configured to open-drain and a pull-up resistor to DVDD is required. The amplifiers must also use the same DVDD voltage. Otherwise, the Class-H configuration is the same as the single device case. See below for the dual device block level diagram.

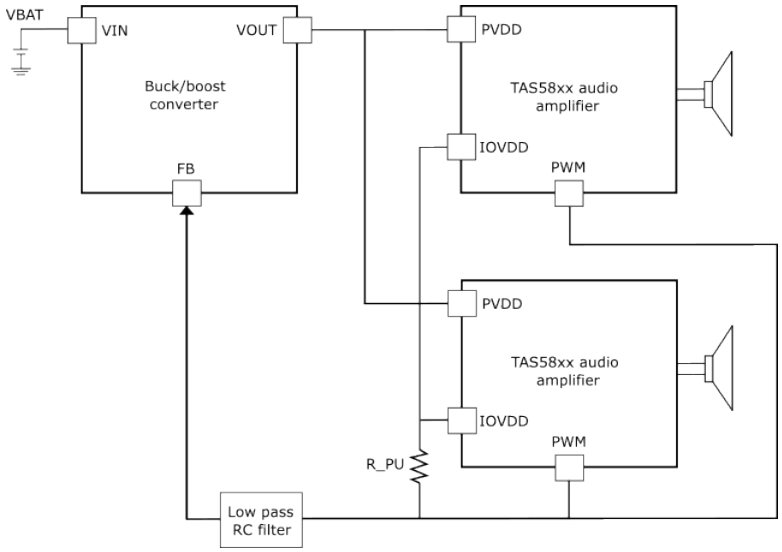

Figure 2-2. Dual Device Class-H Block Diagram

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2.1 Hardware

The external components and connections required for the Class-H algorithm are shown in Figure 2-3. The passive 2nd order low-pass filter is required as it translates the PWM signal to a current control source, which in combination with the feedback resistors, completes the loop that sets the DC-DC converter's output voltage. The pull-up resistor is not required for the single device case if the pin is configured to push-pull.

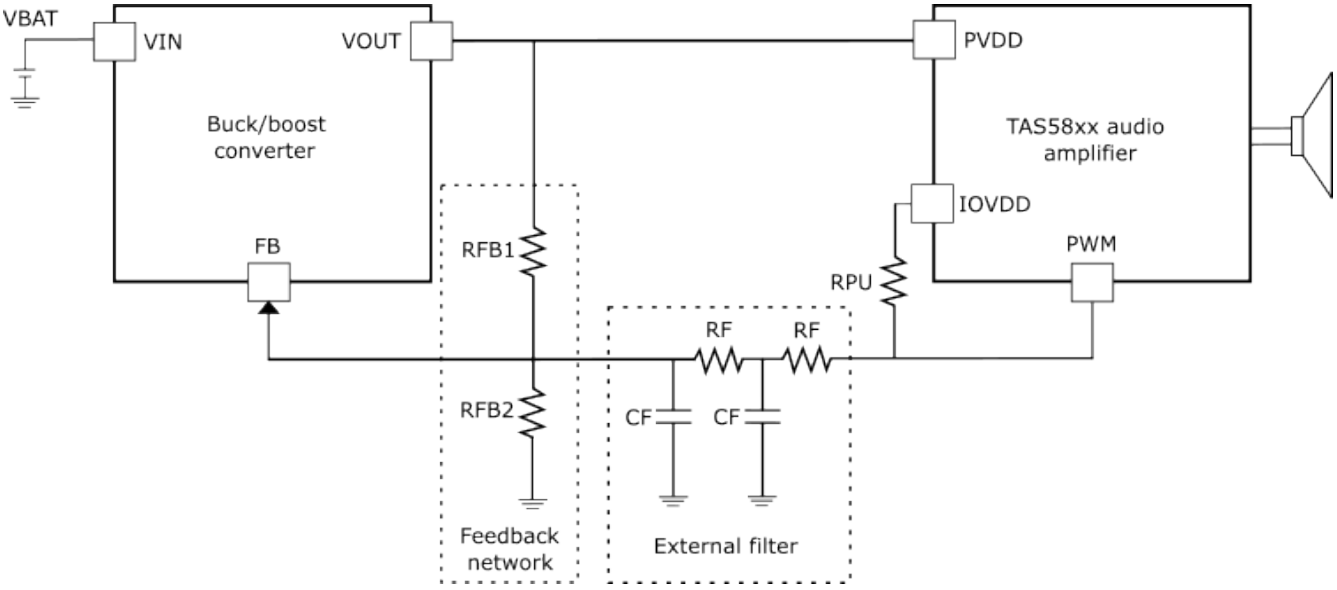

Figure 2-3. Class-H External Components

The following equations can be used to calculate external components values. These equations are used in our PurePathConsole 3 (PPC3) software in the Class-H block for quicker calculation and convenience. It is highly recommended to utilize the PPC3 software to configure Class-H in general to avoid any hand calculation errors. More details on how PPC3 can configure Class-H can be found in Section 2.2.

Equation 1 and Equation 2 are used to set the maximum and minimum PVDD voltages required by the system. The levels correspond to a 0% (GND) and 100% (DVDD) duty cycle PWM control signal respectively.

$$VBST_{Max} = V_{FB} \times \left(1 + \frac{R_{FB1}}{2 \times R_F + R_{PU}} + \frac{R_{FB1}}{R_{FB2}}\right) \quad (1)$$

$$VBST_{Min} = V_{FB} \times \left(1 + \frac{R_{FB1}}{2^{*}R_F + R_{PU}} + \frac{R_{FB1}}{R_{FB2}}\right) - DVDD \times \frac{R_{FB1}}{2 \times R_F + R_{PU}} \quad (2)$$

Where

$DVDD$ = Supply voltage of the digital interface of TAS58xx (3.3V or 1.8V)

V_{FB} = Feedback voltage of the boost converter (from boost converter data sheet)

$VBST_{Max}$ = Maximum output voltage of boost for duty cycle= 0%

$VBST_{Min}$ = Minimum output voltage of boost for duty cycle = 100%

R_{PU} = External pull-up resistor on PWM pin to interface supply of TAS58xx. Typically 1k ohm. (if no pull-up is populated, this value can be entered as 0)

Rearranging equations 1 and 2, you can use equations 3 and 4 to calculate R_F and R_{FB2} with R_{FB1} as a given value between 10 kΩ and 1000 kΩ.

$$R_F = 0.5 \times \left(\frac{DVDD \times R_{FB1}}{V_{BSTmax} - V_{BSTmin}} - R_{PU}\right) \quad (3)$$

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$$R_{FB2} = \frac{R_{FB1}}{\frac{V_{BSTmax}}{V_{FB}} - \frac{R_{FB1}}{2 \times R_F + R_{PU}} - 1} \quad (4)$$

With R_F calculated as shown, the cutoff frequency (f_c) of the low-pass filter should be set several decades lower than the PWM frequency. The capacitor C_F in the low-pass filter can be calculated using Equation 5. In PPC3 the cut off frequency is selected as 70 kHz.

$$C_F = \frac{1}{2 \times \pi + f_C + R_F} \quad (5)$$

The TAS58xx family can support the Class-H PWM signal on various pins. See the table below to identify which pins can be used for the PWM Class-H signal depending on the TAS58xx amplifier. Other than TAS5815, the PWM signal can be selected from one of three GPIO pins. The PWM pin for TAS5815 is SDOUT.

Table 2-1. Class-H PWM Pin Selection

TAS58xx Amplifier	Class-H PWM Pin
TAS5815	SDOUT (pin 9)
TAS5825P	GPIO0 (pin 9), GPIO1 (pin 10), or GPIO2 (pin 11)
TAS5827	GPIO0 (pin 9), GPIO1 (pin 10), or GPIO2 (pin 11)
TAS5828M	GPIO0 (pin 12), GPIO1 (pin 11), or GPIO2 (pin 10)
TAS5830	GPIO0 (pin 12), GPIO1 (pin 11), or GPIO2 (pin 10)

If using one of the TAS58xx EVMs, please refer to the hardware settings below to configure the Class-H connections. For further details on the jumpers and schematics please refer to respective EVM User Guide.

Table 2-2. EVM Class-H Configuration: TAS5827, TAS5828M, TAS5830

	Class-H Boost related jumpers + bananas						General jumpers				
TAS5827EVM, TAS5828MEVM, TAS5830EVM	Battery, GND J12, J13	PVDD, GND J17, J20	J14	J18	J16	J15	J8	J10	J11	J22	J23
	IN - Battery input (9V)	OUT	IN	OUT	OUT	IN	2-3	OUT	OUT	1-2	1-2

Table 2-3. EVM Class-H Configuration: TAS5815

	Class-H Boost related jumpers + bananas								General jumpers	
TAS5815PWPEVM	Battery, GND J25, J26	PVDD, GND J28, J32	J27	J29	J33	J30	J31	J13	J14	J15
	IN – Battery input	OUT	IN	OUT	OUT	IN	IN	2-3	1-2	1-2

Table 2-4. EVM Class-H Configuration: TAS5825P

	Class-H Boost related jumpers + bananas					
TAS5825PEVM	Battery, GND J1, J2	PVDD, GND J21, J23	J10	J22	J4	J3
	IN – Battery input	OUT	IN	OUT	OUT	IN

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2.2 Software

For convenience, each TAS58xx audio amplifier has a corresponding application within PurePath Console 3 software that can be used to tune the in-device DSP. For the devices that support Class-H, there is a dedicated block where the user can configure specific Class-H settings as shown in Figure 2-5. Before going to that block, the user should configure the Class-H PWM pin. For the devices with variable GPIOs, the Class-H PWM signal can be set to any of the three GPIO options. The GPIOs can be configured in the Advanced SRT tab in the Tuning and Audio Processing Page as shown in Figure 2-4. Also in this window the user can select if the GPIO is set to open-drain (checked) or push-pull (unchecked). If open-drain is selected a pull-up resistor must be populated in the RC filter path. This pull-up is optional if the GPIO is configured to push-pull. When multiple TAS58xx amplifiers share a Class-H connection, all devices must be configured for open-drain operation.

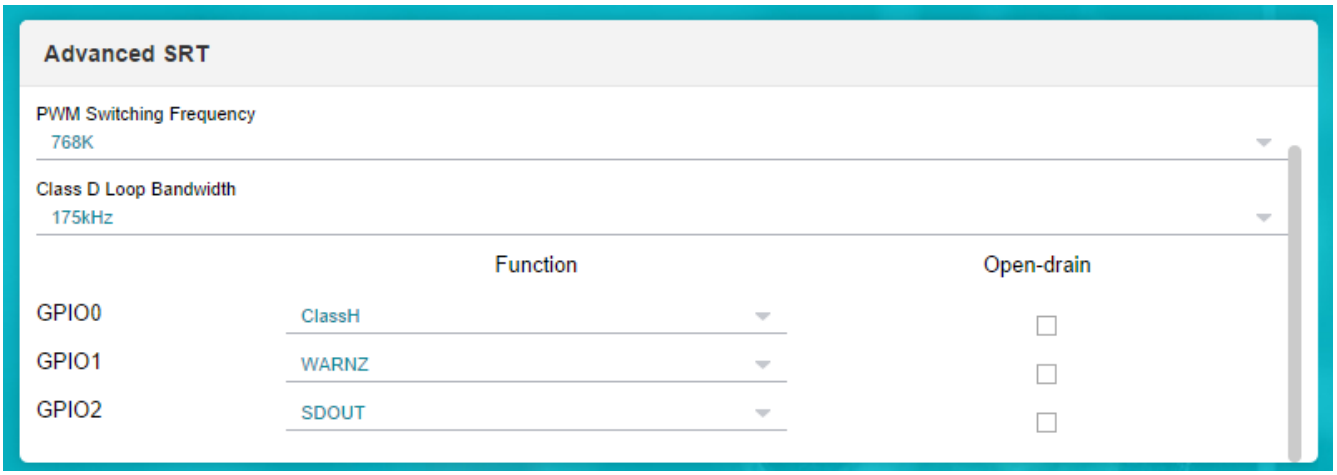

Figure 2-4. PPC3 Class-H PWM Pin Configuration

After the Class-H PWM pin is defined, the user can navigate to the Class-H block to begin tuning.

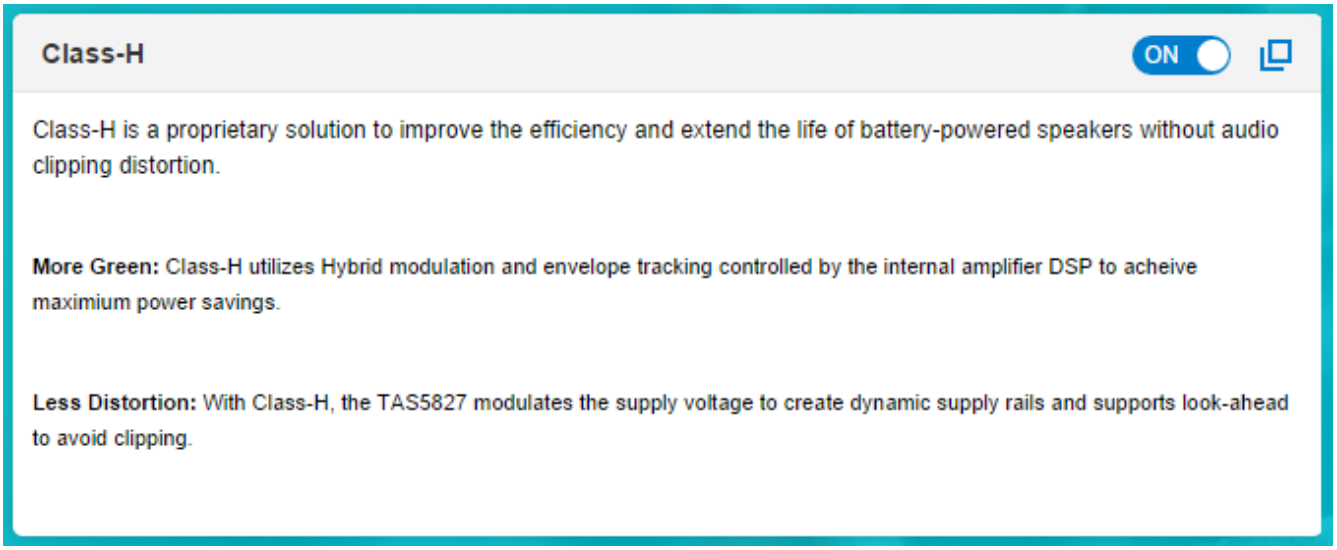

Figure 2-5. PPC3 Class-H Block

There are four sections inside the Class-H PPC3 block. These sections include the configuration window for TAS58xx, configuration window for the DC-DC converter, external hardware interface overview, and TAS58xx amplifier output voltage vs converter voltage.

The TAS58xx configuration section allows users to enter settings such as system speaker impedance and DVDD voltage. If the amplifier supports 16 step Class-H PVDD voltage, it can be selected in this section as well. Additionally, the analog gain can be manually or automatically adjusted in this section. For convenience, the

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Manual box can be unchecked so PPC3 will optimally configure the gain automatically based on the PVDD range.

In the buck / boost section, the maximum and minimum PVDD voltages required by the system should be entered. The maximum PVDD voltage can be calculated using the peak output power required by the system. The feedback voltage can be acquired from the chosen DC-DC converter's datasheet. To efficiently calculate the external components required for the Class-H feature, PPC3 populates the resistor and capacitor values based on all the entered fields and one reference resistor value. The calculated resistor and capacitor values are also updated in the diagram in the boost / buck interface overview window. The equations used for these calculations can be found in Equation 1 through Equation 5.

For a system level view, PPC3 plots the audio amplifier output voltage across the converter's output voltage to show how the Class-H algorithm varies the PVDD voltage with respect to output voltage. This plot is shown in the bottom right of the window.

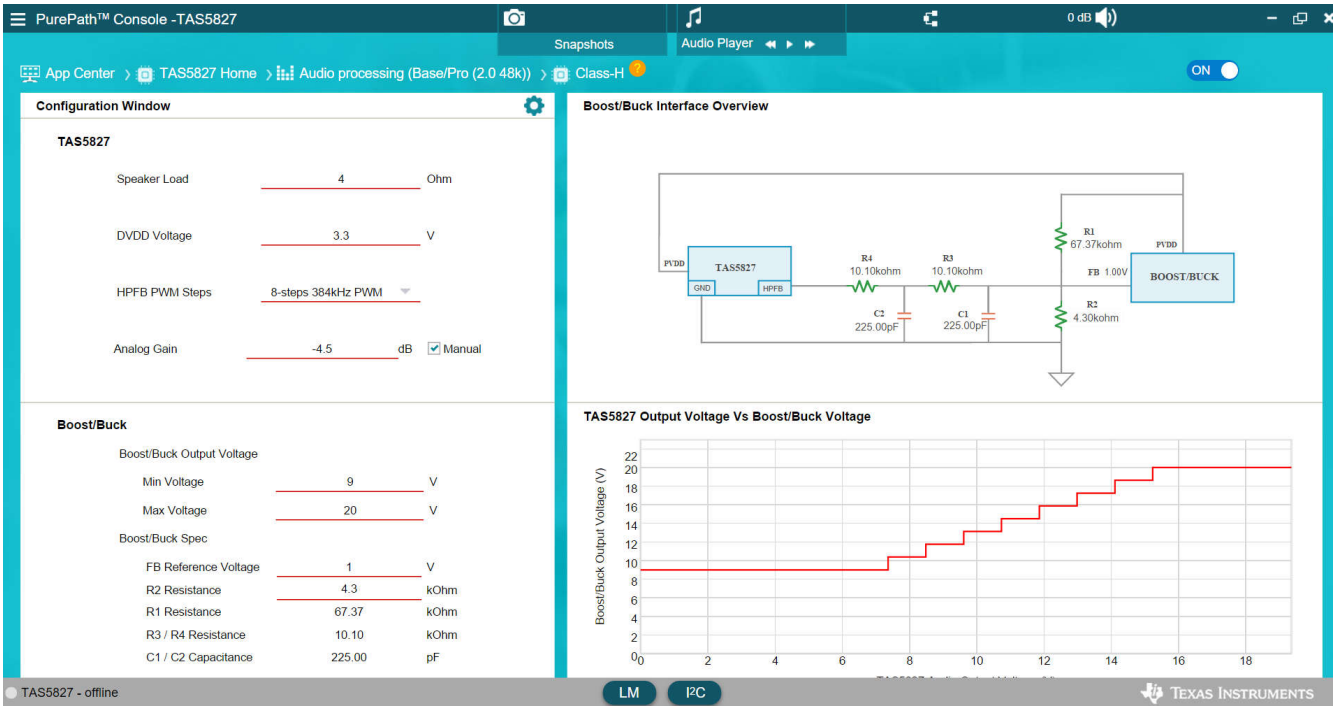

Figure 2-6. PPC3 Class-H Configuration

Within the configuration window there is a gear icon that shows advanced settings for Class-H. These registers can be used to optimize the Class-H algorithm for the end system specifications.

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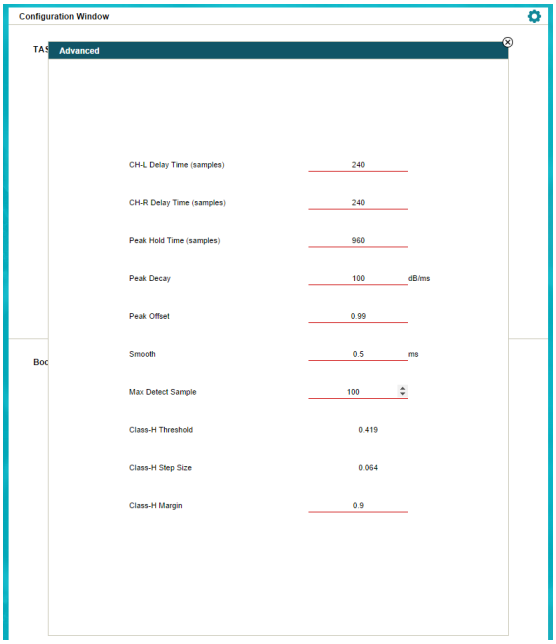

Figure 2-7. PPC3 Class-H Advanced Settings

As these advanced registers are adjusted, there is a trade-off between performance and efficiency. The closer the PVDD level is to the signal, the better the efficiency is, but as the user gets too close the amplifier will begin to clip and there will be a THD degradation. To best optimize these registers for Class-H, the user must define whether optimized means best efficiency and thermal performance, best performance and sound quality, or a balance between the two. Recommendations for tuning these registers can be found in the register descriptions in Table 2-5.

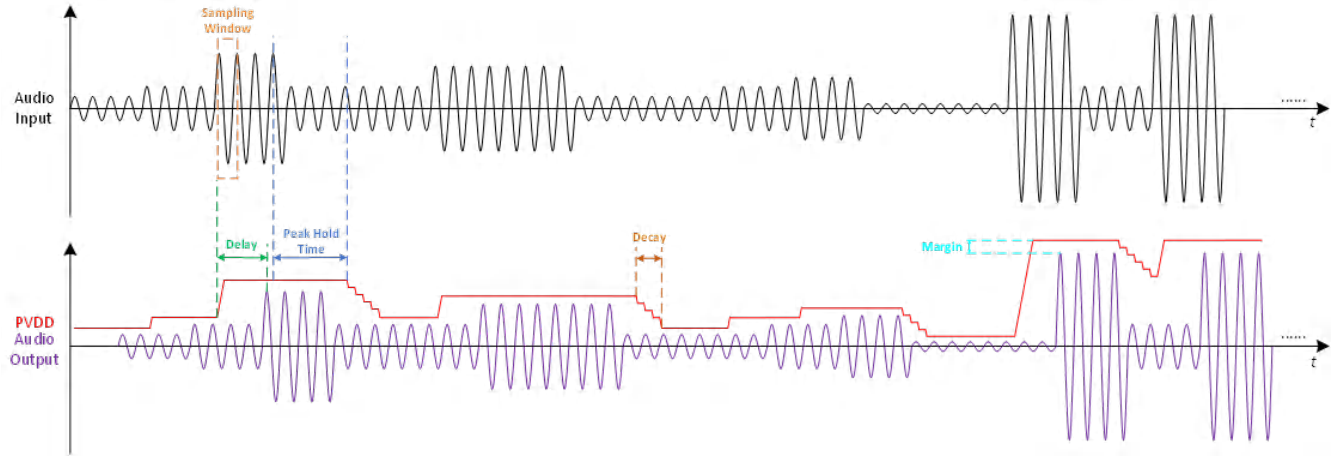

Figure 2-8. Advanced Class-H Register Timing Diagram

Table 2-5. Advanced Class-H Register Descriptions

Register	Description
Class-H Bypass	Bypass Class-H algorithm (available on TAS5827, TAS5828, and TAS5830)
Delay Left BTL / Delay PBTL	Sets the delay / look ahead between audio input and output for the left channel in BTL mode or the mono channel in PBTL mode. This parameter should be set to allow enough time for the DC-DC converter output to settle. Setting this parameter too large will reduce efficiency but guarantee the PVDD output has reached the desired level before the audio to avoid clipping.

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Table 2-5. Advanced Class-H Register Descriptions (continued)

Register	Description
Delay Right BTL	Sets the delay / look ahead between audio input and output for the right channel in BTL mode. This register is not used in PBTL mode. This parameter should be set to allow enough time for the DC-DC converter output to settle. Setting this parameter too large reduces efficiency but makes sure the PVDD output has reached the desired level before the audio to avoid clipping.
Max Detect Window	The number of input samples compared during audio signal level detection. After comparing the number of samples defined, the max value is latched, and Class-H will respond accordingly. When a maximum value is latched, the hold timer starts. For finer processing, this value can be reduced but is typically kept at 100 samples.
Peak Hold	Sets the number of samples that the PVDD level will hold before decaying to prevent rapid voltage fluctuations. This must be set larger than the delay / lookahead time. Setting this value high minimizes rapid voltage fluctuations and strain on the DC-DC converter but decreases efficiency.
Peak Detect Offset	A level between 0-1 to set hysteresis. If an input sample is larger than the previously latched max value multiplied by this offset setting, this new input sample is latched as the new maximum value and the hold timer restarts.
Peak Decay	Rate at which the PVDD level envelopes decay. This decay will start after the peak hold timer is complete.
Peak Smooth Time Constant	Alpha coefficient for the smoothing filter on the audio envelope to filter out peaks.
Class-H Margin	Class-H margin can be used to add output margin for low distortion by internally fine tuning the threshold and steps with PPC3. Higher margin results increase the headroom between PVDD and the signal which improves THD life while lower margin increases efficiency.

These registers are processed through the Class-H algorithm as shown in the Figure 2-9. The locations of the related Class-H registers can be found in Table 2-6.

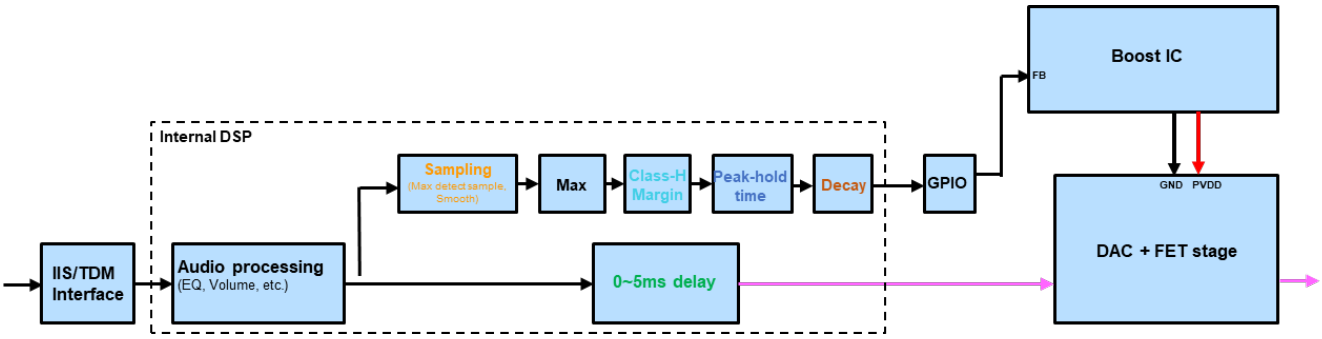

Figure 2-9. Class-H DSP Block Diagram

Table 2-6. Class-H Register Map

Register	Unit	Format	Book	TAS5815		TAS5825P		TAS5827, TAS5828, TAS5830	
				Page	Register	Page	Register	Page	Register
Class-H Bypass	-	4 / 32.0	0x8C	-	-	-	-	0x0A	0x50
Delay Left BTL / Delay PBTL	Samples	4 / 32.0	0x8C	0x2E	0x7C	0x0F	0x2c	0x0A	0x5C
Delay Right BTL	Samples	4 / 32.0	0x8C	0x2F	0x08	0x0F	0x30	0x0A	0x60
Max Detect Window	Samples	4 / 32.0	0x8C	0x2F	0x0C	0x0F	0x40	0x0A	0x68
Peak Hold	Samples	4 / 32.0	0x8C	0x2F	0x10	0x0F	0x44	0x0A	0x6C
Peak Detect Offset	Linear	4 / 1.31	0x8C	0x2F	0x14	0x0F	0x48	0x0A	0x70

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Table 2-6. Class-H Register Map (continued)

Peak Decay	dB / ms	4 / 1.31	0x8C	0x2F	0x18	0x0F	0x4C	0x0A	0x74
Peak Smooth Time Constant	ms	4 / 1.31	0x8C	0x2F	0x1C	0x0F	0x50	0x0A	0x78
Class-H Margin	-	4 / 5.27	0x8C	0x2F	0x20	0x0F	0x54	0x0A	0x7C

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3 Summary

The TAS58xx family's external Class-H feature offers an essential path to achieving high-power audio output while keeping energy consumption and thermal levels at a minimum. This enables designers to create compact solutions that meet the demanding performance expectations of today's audio markets. By following the design guidance in this application note, engineers can configure and optimize Class-H so the TAS58xx family can provide the performance and flexibility required for a wide range of audio applications.

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4 References

1. Texas Instruments, *TAS5827, TAS5828M, and TAS5830 Process Flows*, user's guide.
2. Texas Instruments, *TAS5815 and TAS5802 Process Flows*, user's guide.
3. Texas Instruments, *TAS2781 and TAS2783 Hybrid-Pro Boost Controller*, application note.

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Last updated 10/2025