Application Note

Achieve Delayed Protection for Three Phase Three-Level Inverter with Minimum CLB Resources

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ABSTRACT

Three-level inverter topologies have been commonly used in high power applications, while a special protection control scheme is required, and many users tried to implement this with costly circuits externally. This application report discusses how to use minimum configurable logic block (CLB) resources to implement the protection logic for three phase three-level inverter.

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Trademarks

1 Introduction

Figure 1-1 shows a typical single phase three-level I-Type inverter, named neutral point clamped (NPC) inverter. The single phase NPC inverter includes 4 FETs, such as IGBT, in series, where S1 and S4 are called outer switches, with S2 and S3 called inner switches.

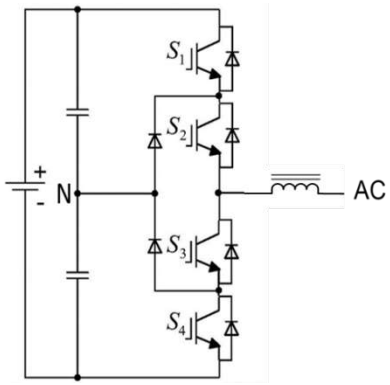

Figure 1-1. Single Phase Three-Level I-Type Inverter

Considering the difference between positive cycle and negative cycle when tied to the grid, the general switching states of four FETs in normal operation are listed in Table 1-1.

Table 1-1. General Switching States in Normal Operation

AC Cycle	Switching States			
	S1	S2	S3	S4
Positive	Alternate switch	Remaining ON	Alternate switch	Remaining OFF
Negative	Remaining OFF	Alternate switch	Remaining ON	Alternate switch

There are several events which lead to quick shut-down to protect the semiconductors and the system, like over current, thermal overload, and so on. Unlike immediately switching off all the FETs simultaneously in two-level inverter, for three-level inverter, make sure that the correct switch-off sequence is maintained: outer switches (S1 or S4) off first, inner switches (S2 or S3) off after a specific delay, while the inner one must be switched on firstly during the recover process. This delayed protection requirement has been a challenge for lots of UPS or solar inverter customers for a long time. Since using software algorithm causes too much delay to provide in-time protection, some customers have to use external hardware circuits, such as FPGA or CPLD, to achieve such protection logic, which increases the system cost and also the development effort.

To address this challenge, the previous application report *Achieve delayed protection for three-level inverter with CLB* introduced a single chip design by leveraging configurable logic block (CLB) of C2000 devices to design the additional delayed protection logic for PWM signals, but when extending from single phase to three phase inverter, no enough CLB tiles for most of C2000 devices, and extra workaround was proposed by occupying additional GPIOs.

Another application report *Achieve delayed protection for three-level inverter with Type 4 EPWM* proposed a creative configuration to leverage existed EPWM features instead, but similarly, when extending to a three phase inverter, additional EPWM modules are required, which is not desirable for high power systems with more EPWM modules required.

Additionally, both application reports assumed the fault events were reflected in hardware (from GPIOs or internal comparator outputs), but in actual applications, the fault event is from multiple sources, and from manual shut down command. A more flexible design is expected with less limitation on the fault events.

This application report discusses how to optimize the CLB logic to achieve the same performance but with less CLB resources. Meanwhile, this can simplify the software design and users can keep the original fault response actions regardless of different fault events. With the upgraded design, any C2000 devices with at least three CLB tiles can be used for three phase three-level inverter, including F2838xD/S, F28379D/S, F28076, F28004xC, F28003x and F28P55X.

2 Design Overview

Figure 2-1 shows the expected EPWM protection behaviors with CLB during positive cycle and negative operation for one phase. The CLB output diagram looks similar to the previous application report, but the way to generate and leverage the CLB output is different.

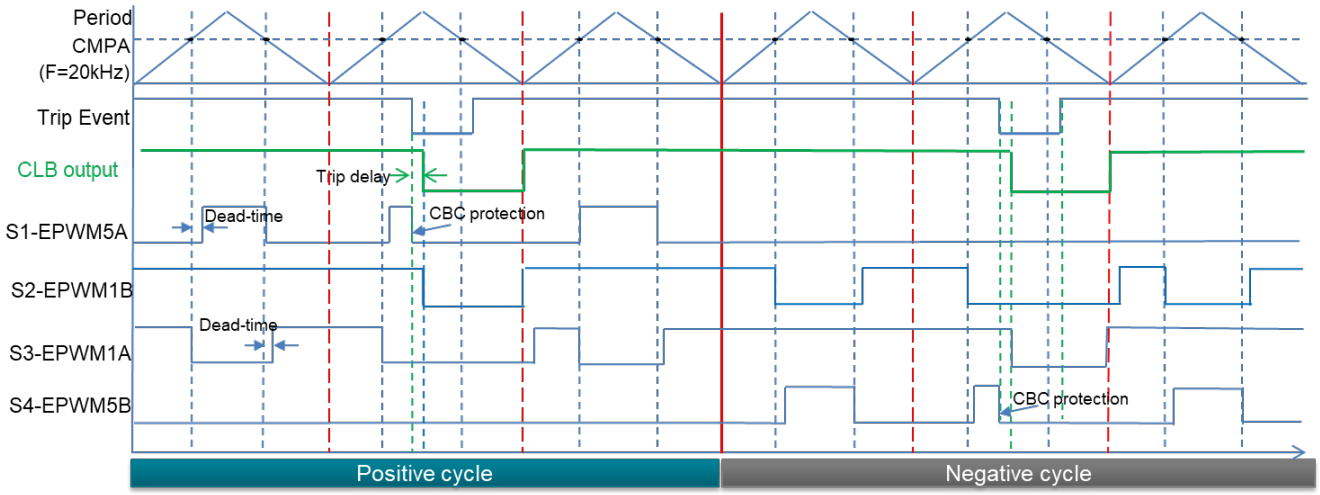

Figure 2-1. Expected EPWM Protection Logic With CLB

Table 2-1 lists the EPWM module and CLB tile assignments for each phase. Since only EPWM1-EPWM4 output can be replaced with the corresponding CLB output due to the peripheral signal multiplexer relationship for CLB for most of C2000 devices, EPWM1,2 and 3 are used for inner switches of three phase respectively.

Table 2-1. EPWM Module and CLB Tile Assignments

Switches	Phase 1	Phase 2	Phase 3
S1	EPWM5A	EPWM6A	EPWM7A
S2	EPWM1B	EPWM2B	EPWM3B
S3	EPWM1A	EPWM2A	EPWM3A
S4	EPWM5B	EPWM6B	EPWM7B
CLB	CLB1	CLB2	CLB3

3 CLB Implementation

Figure 3-1 shows the completed CLB block diagram for each phase.

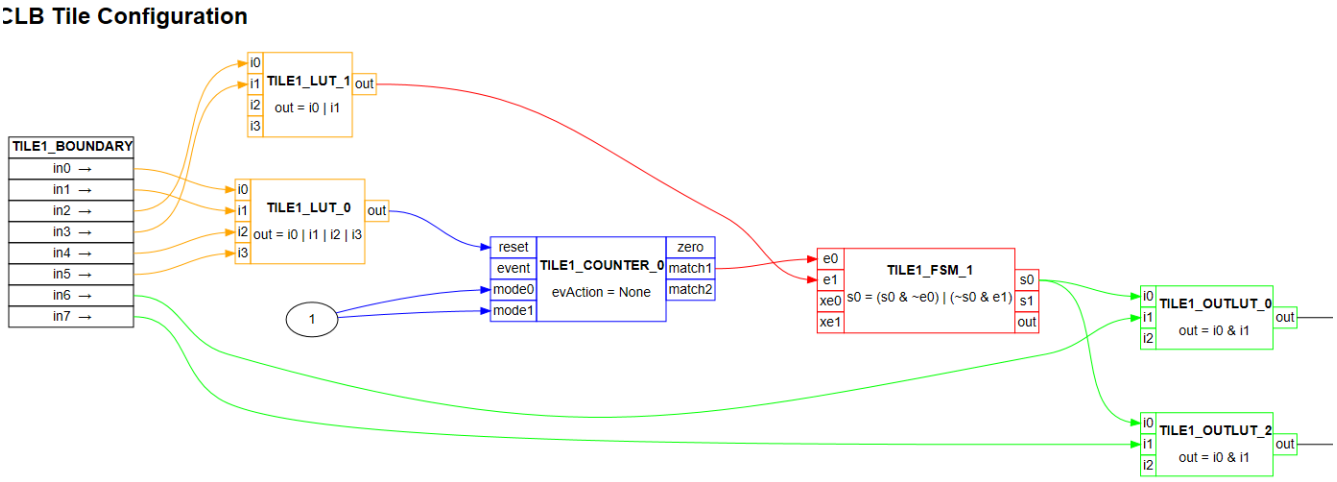

Figure 3-1. Completed CLB Block Diagram

3.1 CLB Input Selection

Total 8 CLB input are required for this design, including the input signals (take Phase 1 as example) shown in Table 3-1 .

Table 3-1. CLB Input Signal Selection

in0	in1	in2	in3	in4	in5	in6	in7
S2-EPWM1B	S3-EPWM1A	S2-EPWM1B (rising edge)	S3-EPWM1A (rising edge)	S1-EPWM5A	S4-EPWM5B	S3 EPWM1A_DB	S2 EPWM1B_DB

In the design, traditional protection response is kept for all EPWM modules, which means all the PWM outputs shut down immediately no matter if there are one-shot or cycle by cycle configurations, triggered by any hardware fault events, or manual shut down (such as software forced trip).

3.2 Counter and FSM Configuration

The counter block is used to achieve the customized delay. An additional LUT_0 is used to combine all the 4 PWM output signals with OR logic, and then the output of LUT_0 is designed as the Reset input of Counter_0. Together with both mode0 and mode1 set to 1, this means Counter_0 does not start to count until all PWM output signals shut down. MATCH1 is set with the expected delay value.

The state machine has been implemented with the FSM block as shown in Figure 3-2. Two inputs are used to identify state of S0, where S0 goes down at E0 and rise at E1. E0 is referred to the Counter_0 match1 event, while E1 is from the output of LUT_1, which combines the rising edges of two inner switch PWM signals (PWM1A and PWM1B), which means the CLB output recovers to high state when either of inner PWM signals turn on. Thus, the Karnaugh map can be created for S0 state, as listed in Table 3-2

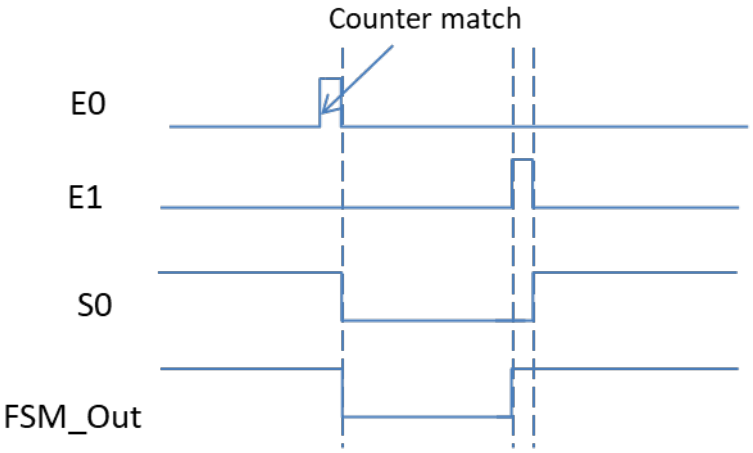

Figure 3-2. State Machine in the FSW Block

Table 3-2. FSM S0 K-Map

S0 E0E1	00	01	11	10
0	0	1	1	0
1	1	1	0	0

Based on the Karnaugh map, the FSM equations for S0 can be deduced as

S0=(S0 & ~E0) | (~S0 & E1)

3.3 CLB Output

The magic of CLB output is the ability to override the original peripheral signals with the signals generated by CLB. In this case, the output LUT is used to combine the FSM_S0 and original EPWM1A/B dead-band output with AND logic. OUTPUT LUT_0 and LUT_2 is selected to enabled the AND logic output as the final EPWM1A/ EPWM1B output, as listed in Figure 3-3.

Table 32-4. CLB Output Signal Multiplexer Table

CLB Output	CLB OUTLUT	CLB1 Destination	CLB2 Destination	CLB3 Destination	CLB4 Destination
0	OUTLUT0	EPWM1A	EPWM2A	EPWM3A	EPWM4A
1	OUTLUT1	EPWM1A_OE	EPWM2A_OE	EPWM3A_OE	EPWM4A_OE
2	OUTLUT2	EPWM1B	EPWM2B	EPWM3B	EPWM4B
3	OUTLUT3	EPWM1B_OE	EPWM2B_OE	EPWM3B_OE	EPWM4B_OE
4	OUTLUT4	EPWM1A_AQ	EPWM2A_AQ	EPWM3A_AQ	EPWM4A_AQ
5	OUTLUT5	EPWM1B_AQ	EPWM2B_AQ	EPWM3B_AQ	EPWM4B_AQ
6	OUTLUT6	EPWM1A_DB	EPWM2A_DB	EPWM3A_DB	EPWM4A_DB
7	OUTLUT7	EPWM1B_DB	EPWM2B_DB	EPWM3B_DB	EPWM4B_DB

Figure 3-3. CLB Output and Peripheral Signal Multiplexer Table

Figure 3-4 shows the relationship of the EPWM submodule signals and CLB logic.

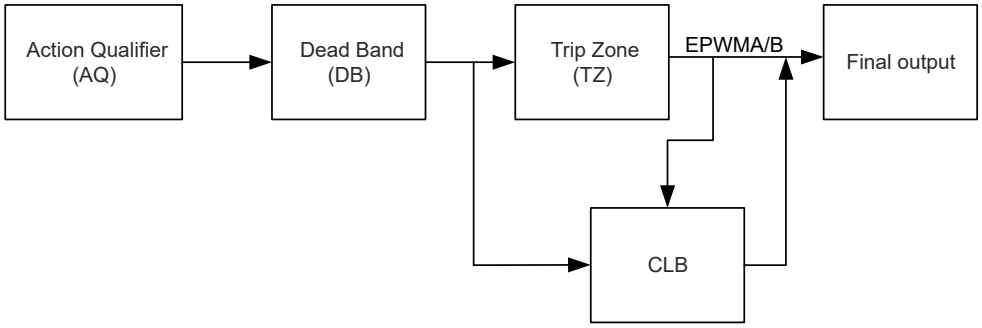

Figure 3-4. Relationship of EPWM Submodule Signals and CLB Logic

4 EPWM Configurations

Table 4-1 lists the different EPWM settings for positive and negative cycles. Different from traditional EPWM configurations, which use dead-band submodule to generate two complementary PWM outputs of the same EPWM module, the complementary behaviors are verified by the inverted action-qualifier actions of two EPWM modules in the present design. Since two EPWM modules shared the same CMPA value, the link register EPWMXLINK can be used to make sure the CMPA value is always updated simultaneously for two EPWM modules.

Grid-tied inverter must take care of the control during both positive and negative cycles. With the present EPWM configurations, swapping EPWMxA and EPWMxB output with the DBCTL[OUT_MODE] register in the dead-band submodule during the zero crossing point is simple.

Table 4-1. EPWM Settings for Positive and Negative Cycles

EPWM Signals	Basic Setting for Position Cycle	Negative Cycle
S1-EPWM5A	↑ CAU ↓ CAD With rising edge delay enabled	Swap EPWMxA and EPWMxB output
S2-EPWM1B	Forced high	
S3-EPWM1A	↑ CAD ↓ CAU With rising edge delay enabled	
S4-EPWM5B	Forced low	

The below codes show the example to swap EPWM outputs.

```
        if(positive_cycle==1)
        {
//Default setting is for positive cycle
             EPWM_setDeadBandOutputSwapMode(EPWM1_BASE, EPWM_DB_OUTPUT_A,false);
             EPWM_setDeadBandOutputSwapMode(EPWM1_BASE, EPWM_DB_OUTPUT_B,false);
             EPWM_setDeadBandOutputSwapMode(EPWM5_BASE, EPWM_DB_OUTPUT_A,false);
             EPWM_setDeadBandOutputSwapMode(EPWM5_BASE, EPWM_DB_OUTPUT_B,false);
        }
        else
        {
// for negative cycle
EPWM_setDeadBandOutputSwapMode(EPWM1_BASE, EPWM_DB_OUTPUT_A, true);
EPWM_setDeadBandOutputSwapMode(EPWM1_BASE, EPWM_DB_OUTPUT_B, true);
EPWM_setDeadBandOutputSwapMode(EPWM5_BASE, EPWM_DB_OUTPUT_A, true);
EPWM_setDeadBandOutputSwapMode(EPWM5_BASE, EPWM_DB_OUTPUT_B, true);
        }
```

4.1 Test Results

The design has been validated with the LaunchPad LAUNCHXL-F280039C, and Kingst Logic Analyzer, as shown in Figure 4-1.

Figure 4-1. Test Platform Setup

Figure 4-2 shows the test results during positive cycle, where EPWM5A starts CBC protection right at the fault event, while EPWM1B turns low after a delay of 2.098us measured, with 2us setting in CLB. The actual delay is a bit longer than the defined value due to the inherent delay with CLB hardware logic circuits. Figure 4-3 shows the fault event during a negative cycle, where the delayed protection logic also works as expected.

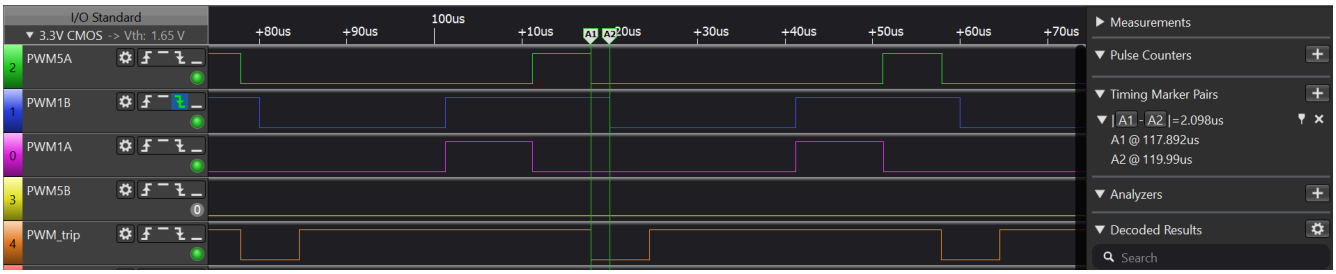

Figure 4-2. Fault Active Low During Positive Cycle

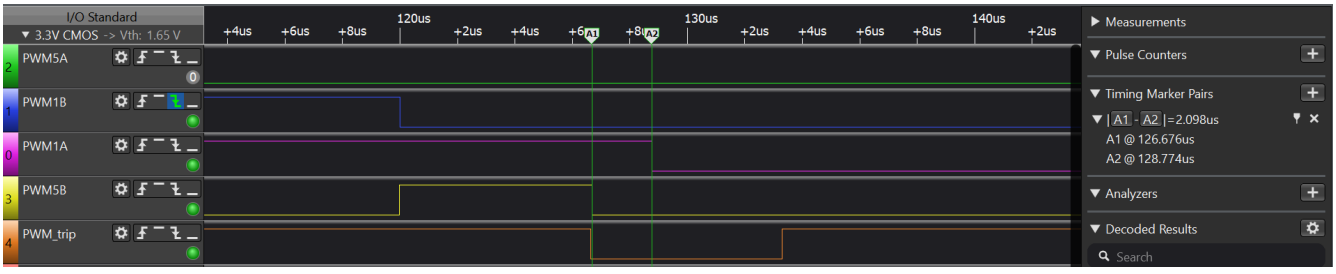

Figure 4-3. Fault Active Low During Negative Cycle

5 Summary

This application report introduces an upgraded design to achieved delayed protection for three phase inverter with minimum of CLB resources. Meanwhile, this can simplify the software design with less software overhead during the zero crossing point in every AC cycle. The design is also validated and adopted in actual applications.

6 References

1. Texas Instruments, *Achieve delayed protection for three-level inverter with CLB*, application note.
2. Texas Instruments, *Achieve delayed protection for three-level inverter with Type 4 EPWM*, application note.

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