Application Note

Clocking TI Clock Buffers with the LMK6Bx BAW Oscillator

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ABSTRACT

This application note shows how TI's LMK6Bx BAW oscillator provides ultra-low jitter reference clocking for LMKDB1x LP-HCSL and LMK1Dx LVDS clock buffers. The LMK6Bx delivers 9.3fs of RMS jitter at 625MHz HS-LVDS, enabling multiple clean clock outputs for telecommunications, networking, and data center applications. The document includes termination schemes, performance data, and phase noise analysis for oscillator-buffer combinations, supporting PCIe Gen 7 and other high-speed digital requirements.

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Trademarks

1 Introduction

The LMK6Bx BAW oscillator can be used to clock any of TI's clock buffers such as the LMKDB1x LP-HCSL buffer and the LMK1D1x LVDS buffer. The LMK6B has a maximum jitter performance of 30fs at 625MHz. This ultra-low jitter performance serves as an ideal reference clock for a buffer, enabling the generation of multiple ultra-low jitter clock signals. Different setups are used with each buffer to demonstrate the total performance of the LMK6Bx with the LMKDB1x or LMK1Dx.

2 The LMK6Bx BAW Oscillator

The LMK6Bx BAW oscillator is a fixed-frequency, factory-programmed, ultra-low jitter oscillator with AC-LVPECL, LVDS, HS-LVDS, Custom Swing (50MHz to 2500MHz), and LP-HCSL (50MHz to 625MHz) differential otuput type options and supports 2.5V and 3.3V. Both the HS-LVDS and Custom Swing output types swing can be programmed in 50mVppd steps from 350mVppd up to 2Vppd for 3.3V supply and for 2.5V supply up to 1.5Vppd for Custom Swing and 1.6Vppd for LVDS. The LMK6Bx also has two function pins. Pin 1 has output enable (OE) or standby (ST) control and pin 2 offers and optional output frequency selection (FSEL), where the frequency specified in the OPN can be divided by 2 or 4. Figure 2-1 shows a block diagram of the LMK6Bx.

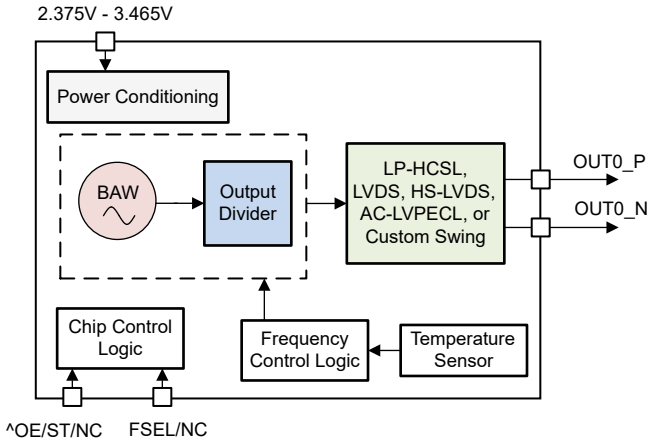

Figure 2-1. LMK6Bx Simplfied Block Diagram

Table 2-1 summarizes the LMK6Bx's ultra-low jitter and industry-leading performance for different output types and selected frequencies, including 4MHz high-pass filter (HPF) measurements.

Table 2-1. LMK6B Jitter Specifications

Output Type	Output Frequency (MHz)	Typical RMS Jitter (fs, 12kHz to 20MHz)(1)	Typical 4MHz HPF RMS Jitter (fs, 12kHz to 20MHz)(1)
AC-LVPECL(1)	156.25	45	31
	312.5	28	19.7
	625	18	9.6
	1250	17	6.3
	2500	16	3.4
LVDS	156.25	58	47.6
	312.5	36	26.3
	625	25	11.6
	1250	22	7.8
	2500	21	4.7
HS-LVDS (1.2Vppd swing)	156.25	50	40.2
	312.5	35	25.1
	625	20	9.3
	1250	19	6.9
	2500	17	3.8
LP-HCSL (V_{OH} = 850mV)	156.25	44	34.8
	312.5	33	20.0
	625	25	12.2

(1) The AC-LVPECL driver uses the Custom Swing driver, AC-LVPECL means the swing is set to 1.6Vppd.

For more information about the LMK6Bx, please refer to the LMK6Bx datasheet.

3 TI Clock Buffers

The LMK6Bx can be used to clock any of TI's clock buffers. In this application note, the two most-commonly used buffers (LMKDB1x and LMK1D1x) are used to demonstrate the oscillator and buffer performance. When looking for a LP-HCSL buffer, refer to Figure 3-2. When looking for a LVDS buffer, refer to Section 3.2.

3.1 The LMKDB1x LP-HCSL Buffer Family

The LMKDB1x LP-HCSL buffer family has extremely low additive jitter and can have two, four, eight, 12, 13, 16 or 20 outputs. The LMKDB12x buffers also work as a MUX and has two inputs that can fan-out to two, four, eigth, or 16 outputs. Figure 3-1 and Figure 3-2 demonstrate the block diagram for these two setups. This buffer supports 1.8V and 3.3V. At the input, the LMKDB1x can accept LP-HCSL input, DC coupled HCSL input, DC coupled LVDS input with external 100Ω termination resistor, and AC coupled inputs with internal self-bias. This buffer has the option to activate internal 50Ω to ground input terminations. At 156.25MHz, the typical additive jitter is 21.9fs and at 312.5MHz, the typical additive jitter is 19.3fs, making this LP-HCSL buffer PCIe Gen 7 compliant.

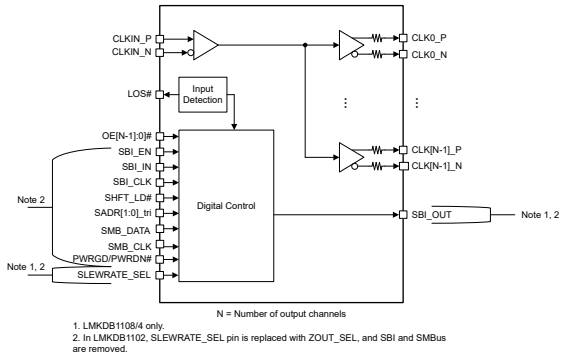

Figure 3-1. LMKDB11x Functional Block Diagram

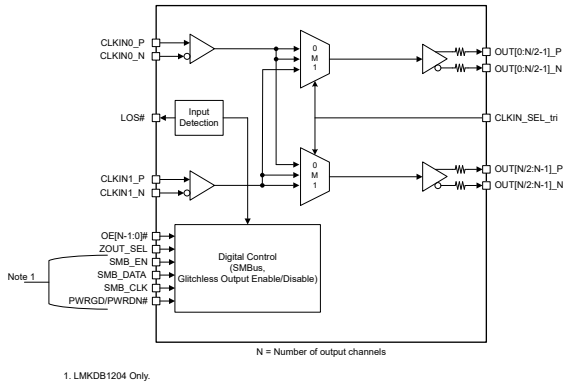

Figure 3-2. LMKDB12x Functional Block Diagram

For more information about the LMKDB1x, please refer to the LMKDB1x datasheet.

3.2 The LMK1Dx LVDS Buffer Family

The high-performance LMK1Dx LVDS buffer family can be used as a MUX and has either one set of 2 inputs to four, eight, 12, or 16 outputs or two sets of one input to two, four, six, or eight outputs. This device can support 1.8V, 2.5V, and 3.3V. Figure 3-3 and Figure 3-4 illustrate these different input to output terminations. The LMK1Dx inputs can be interfaced with LVDS, LVPECL, HCSL or LVCMOS drivers. At 156.25MHz, the typical additive jitter is 50fs and at 312.5MHz the typical additive jitter is 31fs. The LMK1Dx has a high-swing LVDS option (HS-LVDS) with 500mV V_{OD} typical to provide a higher slew rate at the outputs.

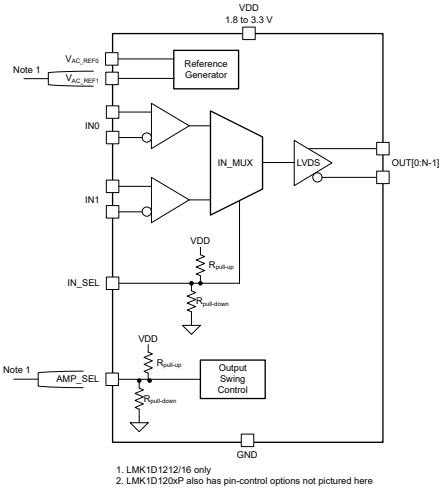

Figure 3-3. LMK1D12x Simplified Block Diagram

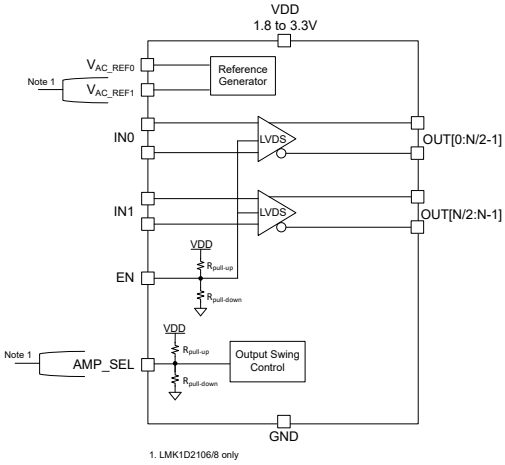

Figure 3-4. LMK1D21x Simplified Block Diagram

For more information about the LMK1D12x, see the LMK1D12x datasheet and for more information about the LMK1D21x, refer to LMK1D21x datasheet.

4 Clocking LMKDB1x with LMK6Bx

When clocking the LMKDB1x LP-HCSL buffer with the LMK6Bx, the LMKDB1x achieves best performance when using the LMK6BGx. The *G* in the OPN refers to HS-LVDS output type (V_{CM} = 1.2V) with a custom swing of 1.6Vppd. Figure 4-1 demonstrates the correct termination to clock the LMKDB1x with the LMK6BGx. The LMK6BGx can replace any LVDS-type oscillator already on the board without any required changes.

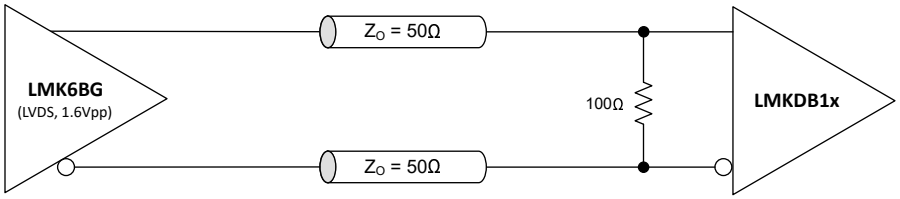

Figure 4-1. LMK6BGx Termination Required to Drive the LMKDB1x LP-HCSL Buffer

When clocking the LMKDB1x with the LMK6BGx, the total jitter of the clock tree results in 32.4fs at 312.5MHz and 22.4fs when using a 4MHz HPF. Table 4-1 summarizes the jitter of the LMK6BGx, the total jitter of the LMK6BGx clocking the LMKDB1x, and respective 4MHz high-pass filter (HPF) jitter. Figure 4-2 and Figure 4-3 showcase the respective phase noise curves.

Table 4-1. LMK6BGx and LMKDB1x Performance Summary (3.3V Supply)

Output Frequency (MHz)	LMK6BGx RMS Jitter (fs) (1)	LMK6BGx + LMKDB1x RMS Jitter (fs)(1)	LMK6BGx 4MHz HPF RMS Jitter (fs)(1)	LMK6BGx + LMKDB1x RMS Jitter (fs)(1)
156.25	39.7	49.7	30.5	37.0
312.5	25.3	32.4	16.0	22.4

(1) RMS jitter calculated from 12kHz to 20MHz integrated bandwidth.

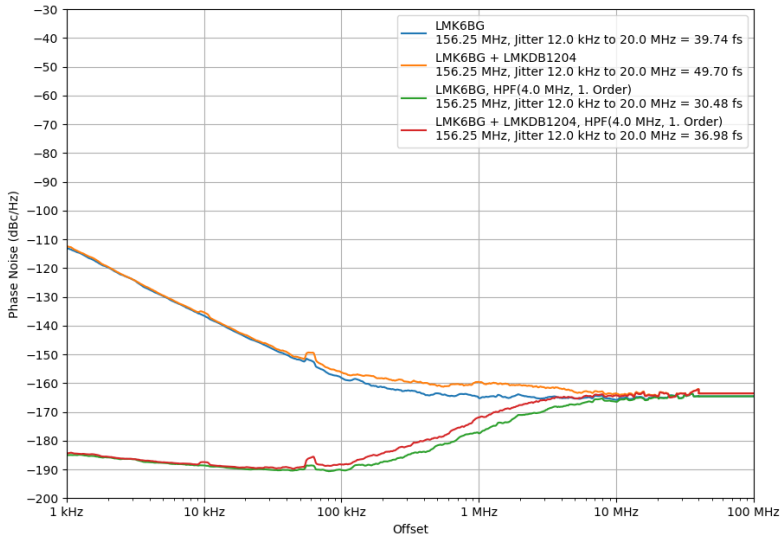

Figure 4-2. LMK6BGx and LMK6BGx + LMKDB1x Phase Noise Curves at 156.25MHz and 3.3V

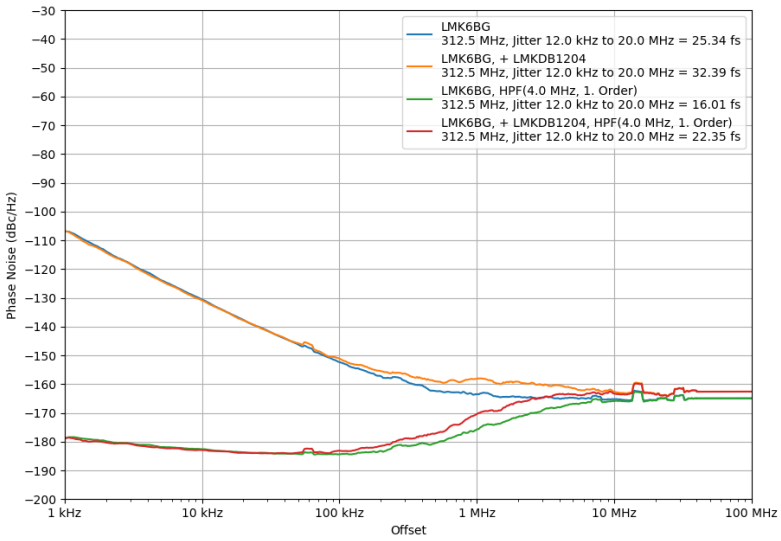

Figure 4-3. LMK6BGx and LMK6BGx + LMKDB1x Phase Noise Curves at 312.5MHz and 3.3V

4.1 Clocking LMKDB1x Buffer with a LP-HCSL Oscillator

The LMK6BIx (LP-HCSL output type with V_{OH} = 850mV) can replace any LP-HCSL oscillator clocking the LMKDB1x. Figure 4-4 demonstrates the required biasing to clock the LMKDB1x with a LP-HCSL oscillator. Make sure the 50Ω internal termination of the LMKDB1x is turned off. For any other oscillator replacement guidance, see the LMK6Bx datasheet.

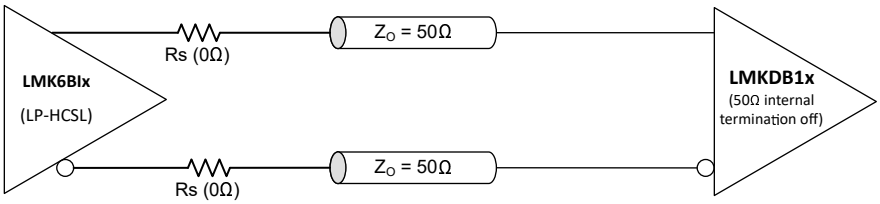

Figure 4-4. LMK6BIx Oscillator Termination Required to Drive the LMKDB1x LP-HCSL Buffer

Table 4-2 summarizes the RMS jitter (with and without a 4MHz HPF) of the LMKDB1x when clocked by the LMK6BIx and Figure 4-5 and Figure 4-6 showcase each corresponding phase noise plots.

Table 4-2. LMK6BIx and LMKDB1x Performance Summary (3.3V Supply)

Output Frequency (MHz)	LMK6BIx RMS Jitter (fs) (1)	LMK6BIx + LMKDB1x RMS Jitter (fs)(1)	LMK6BIx 4MHz HPF RMS Jitter (fs)(1)	LMK6BIx + LMKDB1x 4MHz HPF RMS Jitter (fs)(1)
156.25	46.5	49.6	34.8	37.1
312.5	30.2	31.2	20.0	21.2

(1) RMS jitter calculated from 12kHz to 20MHz integrated bandwidth.

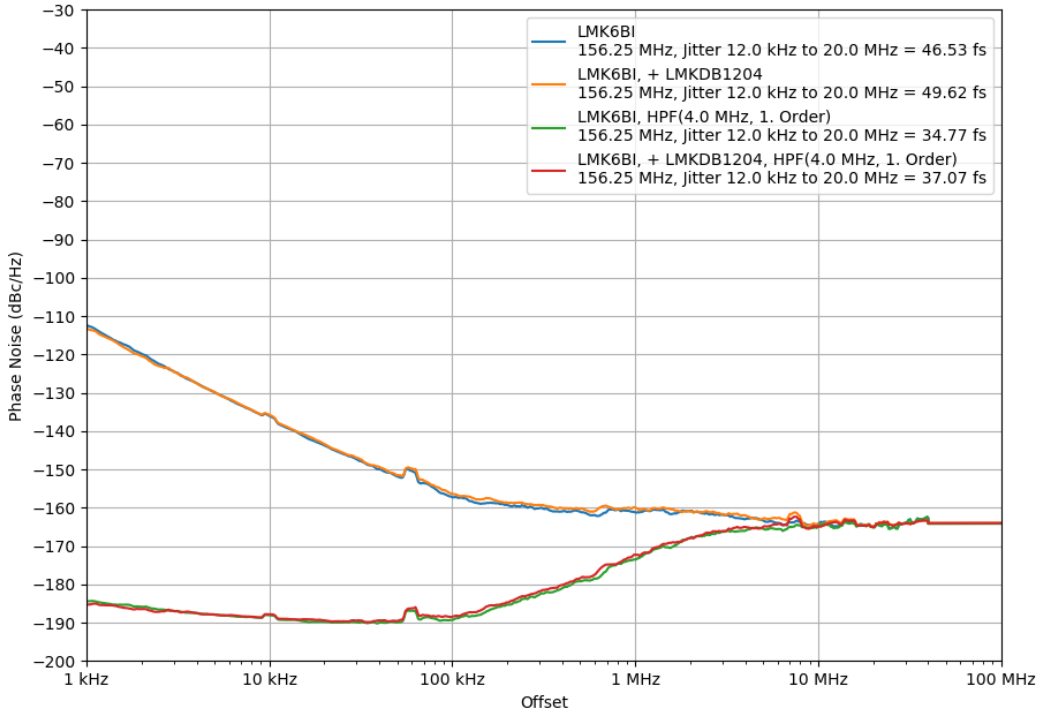

Figure 4-5. LMK6BIx and LMK6BIx + LMKDB1x Phase Noise Curves at 156.25MHz and 3.3V

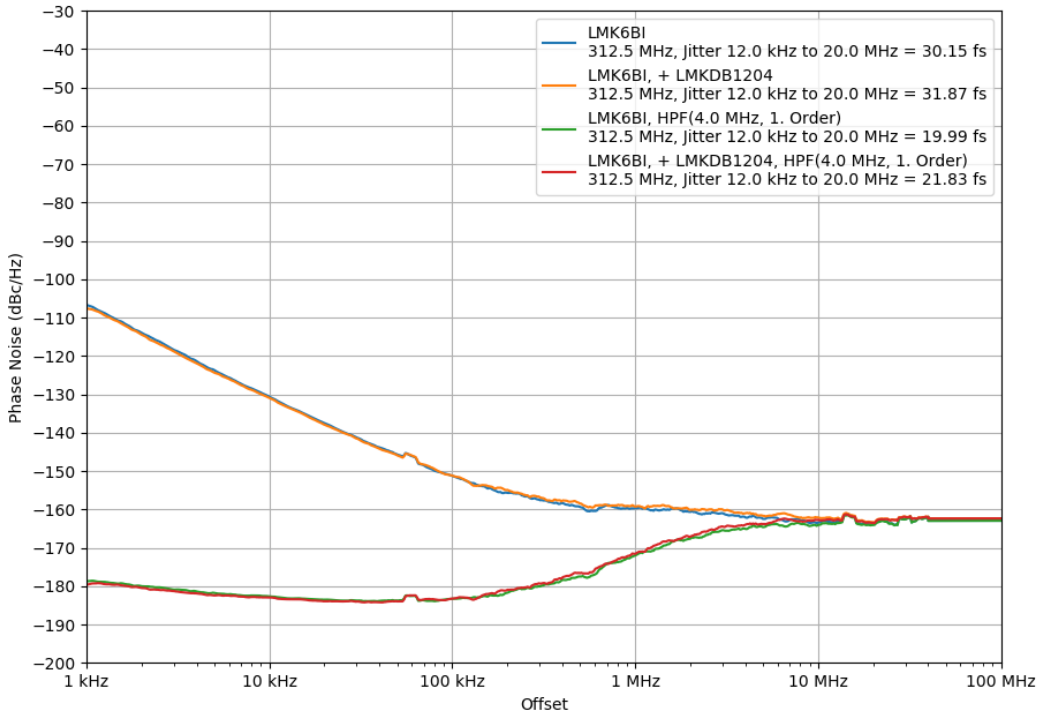

Figure 4-6. LMK6BIx and LMK6BIx + LMKDB1x Phase Noise Curves at 312.5MHz and 3.3V

5 Clocking the LMK1Dx with the LMK6Bx

When clocking the LMK1Dx LVDS buffer with the LMK6Bx, the LMK1Dx achieves best performance when using the LMK6BPx or LMK6BKx. The *P* in the OPN refers to AC-LVPECL output type which has a V_{CM} = VDD/2 with and a swing of 1.6Vppd. The *K* refers to a swing of 2Vppd with V_{CM} = VDD/2V. Figure 5-1 demonstrates the correct termination to clock the LMK1Dx with the LMK6BPx or LMK6BKx. The LMK6BPx or LMK6Bx can replace any LVDS-type oscillator already clocking the LMK1Dx without any required board changes.

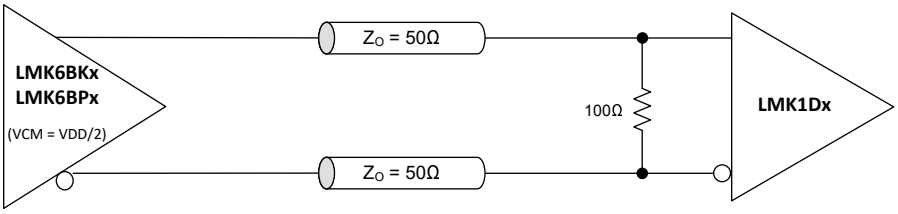

Figure 5-1. LMK6BKx or LMK6BPx Termination to Drive the LMK1Dx or LMK1Dx LVDS Buffer

When clocking the LMK6BPx with the LMK1Dx, the total jitter of the clock tree results in 28.1fs at 625MHz and the LMK6BKx with the LMK1Dx results in 28.0fs at 625MHz (both at 3.3V supply). With a 4MHz HPF, the total jitter is 16.6fs at 625MHz with an AC-LVPECL output. As seen from these values, either LMK6B configuration achieves very similar jitter. For the purpose of this application note, data is shown for LMK6BPx. Table 4-1 summarizes the jitter of the LMK6BPx when clocked with the LMK1Dx (and respective 4MHz HPF values). Figure 4-2 showcase the respective phase noise curves.

Table 5-1. LMK6BPx and LMK1Dx Performance Summary (3.3V Supply)

Output Frequency (MHz)	LMK6BPx RMS Jitter (fs) (1)	LMK6BPx + LMK1Dx RMS Jitter (fs)(1)	LMK6BPx 4MHz HPF RMS Jitter (fs)(1)	LMK6BPx + LMK1Dx 4MHz HPF RMS Jitter (fs)(1)
156.25	49.9	30.7	34.8	45.1
312.5	30.8	40.4	16.2	28.4
625	19.8	28.1	8.2	16.6

(1) RMS jitter calculated from 12kHz to 20MHz integrated bandwidth

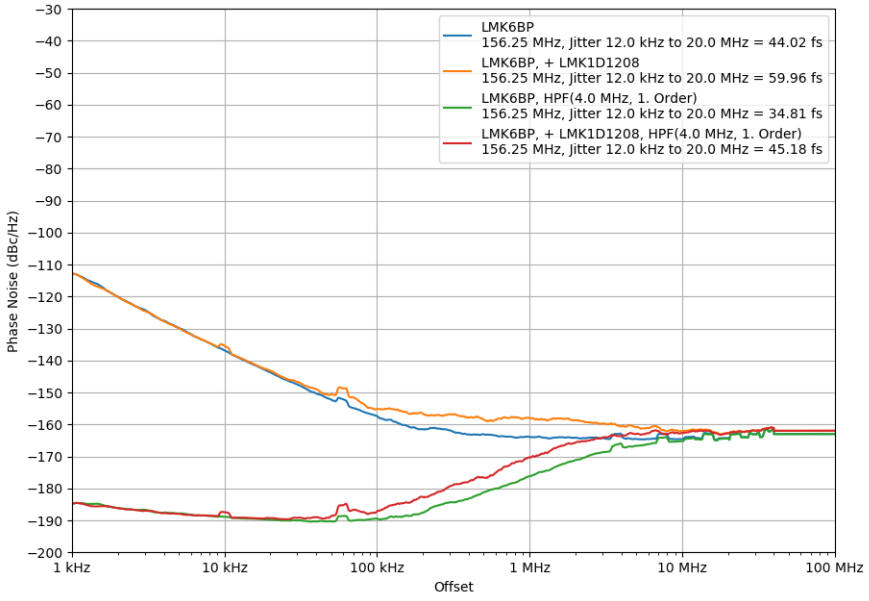

Figure 5-2. LMK6BP and LMK6BPx + LMK1Dx Phase Noise Curves at 156.25MHz and 3.3V

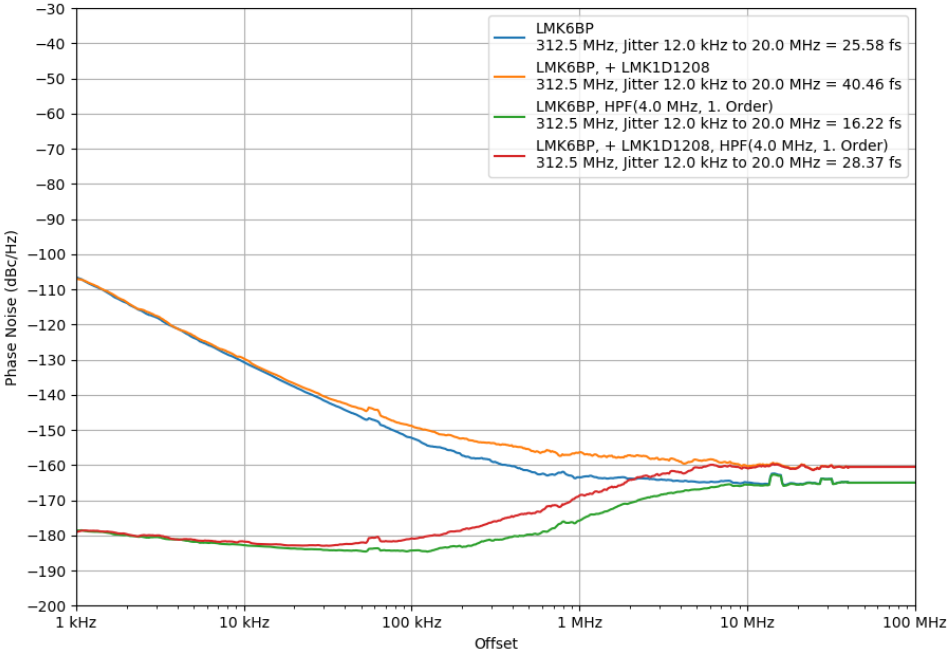

Figure 5-3. MK6BPx + LMK1Dx Phase Noise Curves at 312.5MHz and 3.3V

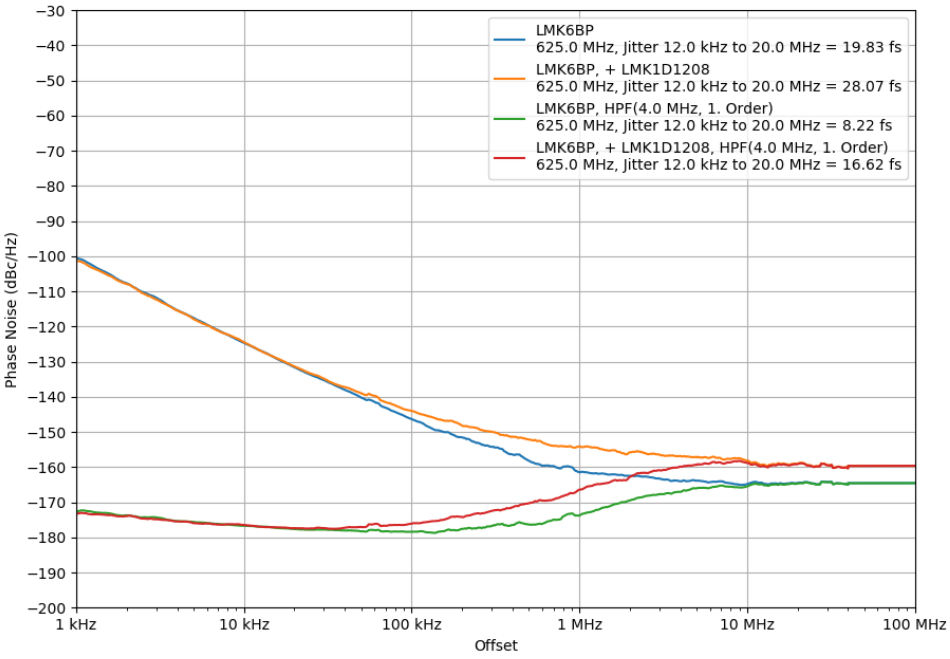

Figure 5-4. LMK6BPx and LMK6BPx + LMK1Dx Phase Noise Curves at 625MHz and 3.3V

5.1 Clocking LMK1Dx Buffer with a LP-HCSL Oscillator

The LMK6BIx (LP-HCSL output type with V_{OH} = 850mV) can replace any LP-HCSL oscillator clocking the LMK1Dx. Figure 5-5 demonstrates the required biasing to clock the LMK1Dx with a LP-HCSL oscillator. For any other oscillator replacement guidance, see the LMK6Bx datasheet.

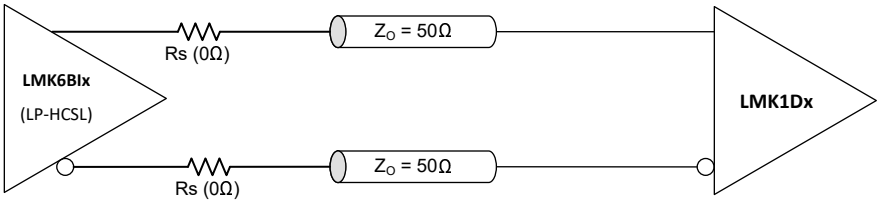

Figure 5-5. LMK6BIx Oscillator Termination Required to Drive the LMK1Dx LP-HCSL Buffer

Table 5-2 demonstrates the RMS jitter of the LMK1Dx when clocked by the LMK6BIx (and the respective 4MHz HPF jitter). Figure 5-6 through Figure 5-8 showcase each corresponding phase noise plots.

Table 5-2. LMK6BIx and LMK1Dx Performance Summary (3.3V Supply)

Output Frequency (MHz)	LMK6BIx RMS Jitter (fs) (1)	LMK6BIx + LMK1Dx RMS Jitter (fs)(1)	LMK6BIx 4MHz HPF RMS Jitter (fs)(1)	LMK6BIx + LMK1Dx 4MHz HPF RMS Jitter (fs)(1)
156.25	46.5	63.3	34.8	48.2
312.5	30.2	45.1	20.0	32.9
625	22.7	34.0	12.2	22.8

(1) RMS jitter calculated from 12kHz to 20MHz integrated bandwidth.

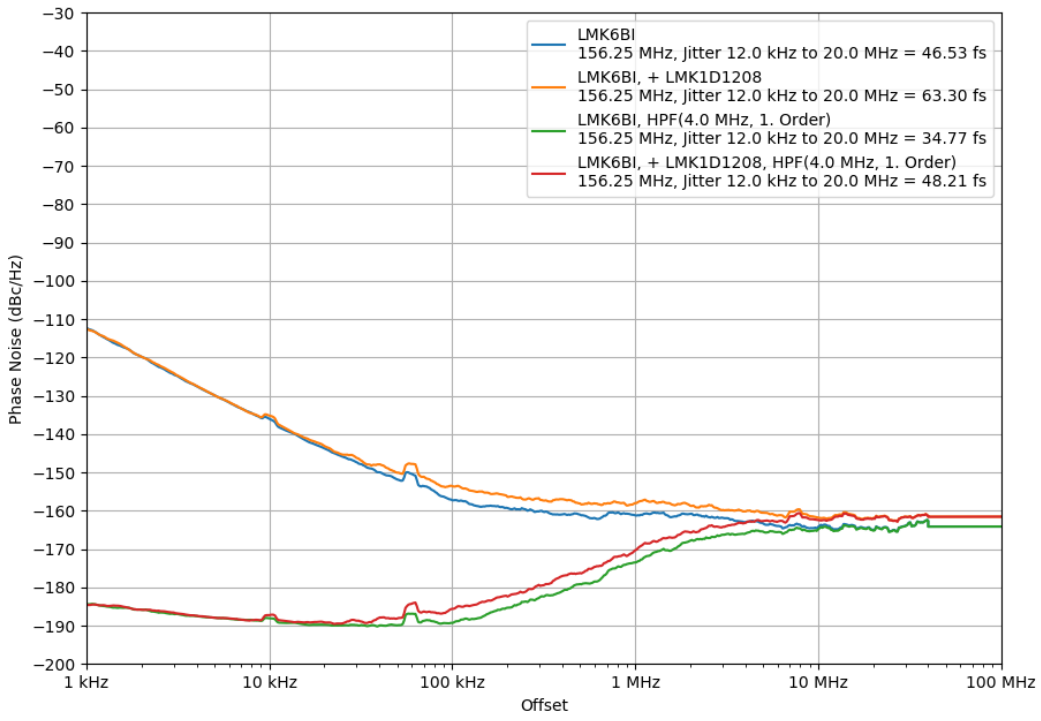

Figure 5-6. LMK6BIx and LMK6BIx + LMK1Dx Phase Noise Curves at 156.25MHz and 3.3V

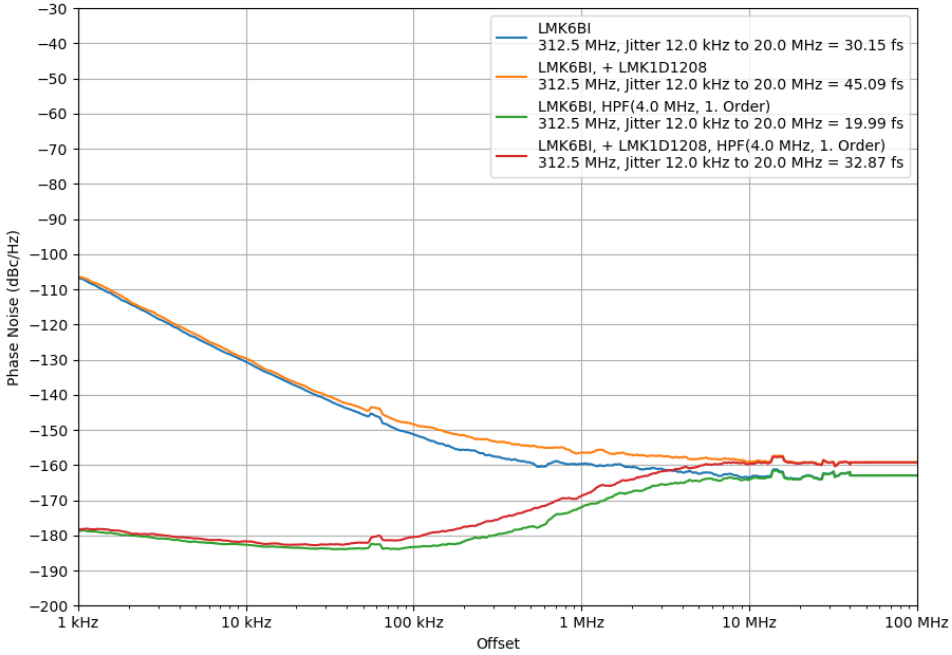

Figure 5-7. LMK6BIx and LMK6BIx + LMK1Dx Phase Noise Curves at 312.5MHz and 3.3V

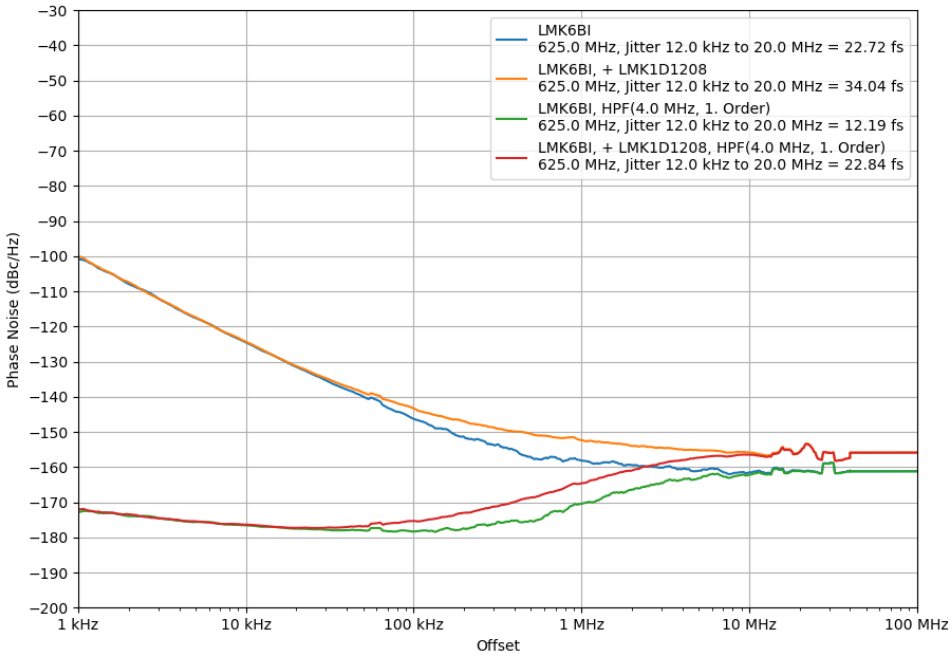

Figure 5-8. LMK6BIx and LMK6BIx + LMK1Dx Phase Noise Curves at 625MHz and 3.3V

6 Summary

To achieve best performance, combine both the LMK1Dx and LMKDB1x buffers with the LMK6Bx. In either combination, the jitter is < 41.2fs at 312.5MHz of jitter from either clock tree. The LMK1Dx and LMKDB1x are preferred buffers to replicate the ultra-low jitter performance of the LMK6Bx. Make sure to properly terminate the LMK6Bx to each buffer to achieve the performance demonstrated on this application note.

7 References

- Texas Instruments, *LMK6Bx datasheet*, datasheet.
- Texas Instruments, *LMK1D120x datasheet*, datasheet.
- Texas Instruments, *LMK1D210x datasheet*, datasheet.
- Texas Instruments, *LMKDB1x datasheet*, datasheet.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2026) to Revision A (May 2026)	Page
• Corrected the device from LMK1D12x to LMK1D21x	5

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