Application Note

TPS257xx-Q1 System Telemetry

ABSTRACT

The TPS257xx-Q1 is an automotive-qualified USB Type-C® Power Delivery (PD) controller designed to enable robust, standards-compliant power negotiation and system monitoring in modern vehicle architectures. As USB-C ports evolve to support higher power levels and expanded functionality, system designers require reliable power control, fault protection, and real-time telemetry to verify safe and efficient operation. The TPS257xx-Q1 address these challenges by integrating USB PD policy management, power path control, protection features, and I2C-accessible telemetry into a single design. The device provides operational status and fault reporting that allows a host MCU or HUB to monitor, diagnose, and dynamically manage charging ports. This reduces system complexity while improving safety and reliability.

Table of Contents

Trademarks

1 Introduction

Telemetry refers to the measurement and reporting of device operating parameters through a digital interface such as I2C. Many systems require real-time monitoring of voltage, current, temperature, power, and fault status, and may also adjust operating conditions dynamically based on this information. The TPS257xx-Q1 USB Type-C® Power Delivery (PD) controller provides system telemetry through its I2C interface. When used in conjunction with a host MCU or HUB, the device allows the host to read operational status and fault information for each charging port.

2 PD Controller Host Interface Description

2.1 TPS257xx-Q1 I2C Target Addresses

The TPS257xx-Q1 internal registers are accessed through the I2C interface. The device provides two I2C target addresses, one per port. To read or write internal registers, the I2C controller must address the appropriate target address corresponding to the desired port. The assigned target address depends on the boot mode detected at power-up. Boot mode selection is determined by the R_{TVSP} resistance between the TVSP pin and PGND. Each port is assigned a unique I2C target address based on the detected boot configuration. Refer to the device data sheet for detailed boot mode descriptions and the corresponding target address mappings (see Table 2-1).

Table 2-1. I2C Target Address by TVSP Configuration (TPS2576xxQRQLRQ1 and TPS25772xQRQLRQ1)

TVSP Index	Port A Target Address	Port B Target Address
0, 2, 5, 7, and 8	0x22	0x26
1, 3, 4, and 6	0x23	0x27

2.2 Host Interface Protocol

The Host Interface allows for complex interactions between an I2C controller and a PD Controller. The I2C Target unique address is used to receive or respond to Host Interface protocol commands. Figure 2-1 and Figure 2-2 show the write and read protocols, respectively.

When writing a register that has a defined length of N bytes, if the I2C transaction only contains n bytes then the final (N - n) bytes of the register remain unchanged.

When reading a register that has a defined length of N bytes, the I2C controller may terminate the I2C read transaction after the first n bytes (n < N).

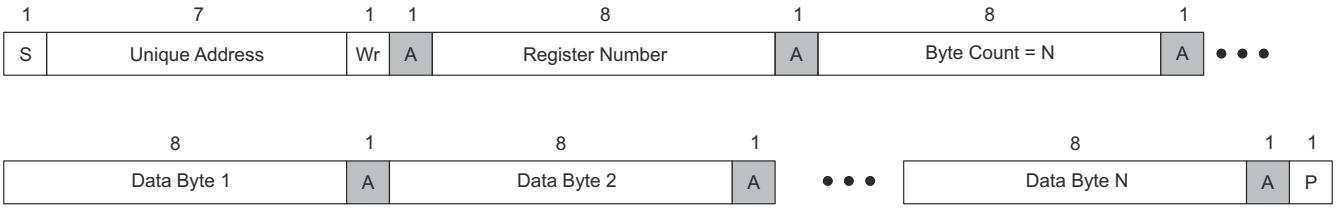

Figure 2-1. I2C Host Interface Write Register Protocol

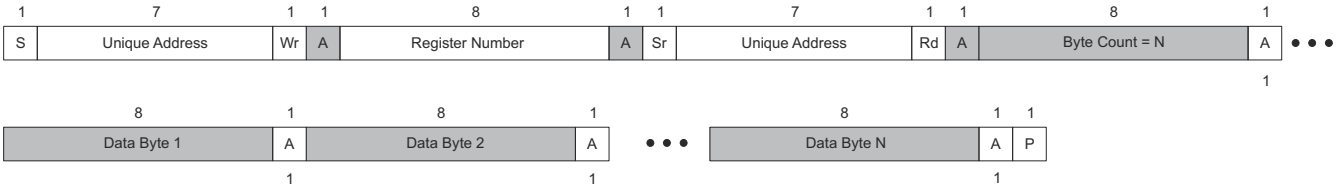

Figure 2-2. I2C Host Interface Read Register Protocol

3 TPS257xx-Q1 Telemetry Registers

3.1 STATUS Register (Address = 1Ah)

This read-only (RO) register returns port status parameters. When the host reads from the Port A target address (0x22 or 0x23), the register returns the status associated with Port A. When the host reads from the Port B target address (0x26 or 0x27), the register returns the status associated with Port B.

Table 3-1. STATUS Register Bit Field Descriptions

Bits	Name	Description	
Bytes 6-12: Telemetry			
55:48	Vntc Voltage	VNTC voltage ADC reading (14mV per LSB)	
47:40	Vbus Current	VBUS current ADC reading (23mA per LSB)	
39:32	Vbus Voltage	VBUS voltage ADC reading (98mV per LSB)	
31:24	Vin Voltage	VIN voltage ADC reading (80mV per LSB)	
23:16	DCDC1CurrCode	DCDC1 Current code reading (25mA per LSB). Valid only on Port A reading.	
15:0	DCDC1VCode	DCDC1 Voltage code reading (10mV per LSB). Lower 12bits + 4 pad bits. Valid only on Port A reading.	
Bytes 2-5: Reserved			
31:0	Reserved	Reserved	
Byte 1: Port Status			
7	Reserved	Reserved	
6	Data Role	PD controller data role. This is only valid once there is a connection.	
		0b	Upstream Facing Port (UFP)
		1b	Downstream Facing Port (DFP)
5	Port Role	Current state of PD Controller CCx terminations. This also indicates the PD Controller's Power Role once connected.	
		0b	PD Controller is in the Sink role. This means the CCx pull-down is active or the port is disabled/disconnected.
		1b	PD Controller is Source (CCx pull-up active).
4	Plug Orientation	0b	Upside-up orientation (plug CC on CC1)
		1b	Upside-down orientation (plug CC on CC2)
3:1	Connection State	Details of a connected plug.	
		000b	No connection.
		001b	Port is disabled.
		010b	Reserved
		011b	Reserved
		100b	No connection, Ra detected (Ra, but no Rd).
		101b	Reserved
		110b	Connection present, no Ra detected.
		111b	Connection present. Ra detected.
0	Plug Present	Status of the plug.	
		0b	No plug is connected.
		1b	A plug is connected.

3.2 POWER PATH STATUS Register (Address = 26h)

This RO register returns power path status and fault status parameters. When the host reads from the Port A target address (0x22 or 0x23), the register returns the status associated with Port A. When the host reads from the Port B target address (0x26 or 0x27), the register returns the status associated with Port B.

Table 3-2. POWER PATH STATUS Register Bit Field Descriptions

Bits	Name	Description
Byte 5: Power Path Common Status		
7:4	Reserved	Reserved
3	VIN Good FE	VIN Good falling edge. Asserted if a UVLO condition is detected on VIN (Falling edge below VIN Good threshold).
2	VIN Ovp	VIN OVP. Asserted if an OVP condition exists on VIN.
1:0	Reserved	Reserved
Byte 4: VBUS, VCONN, DPDM Fault Status		
7:6	Reserved	Reserved
5	DPDM Ovp	DPDM OVP. Asserted if an OVP condition exists on DP DM.
4	Vconn Ovp	VCONN OVP. Asserted if an OVP condition exists on VCONN.
3	Vconn Ocp	VCONN OCP. Asserted if an OCP condition exists on VCONN.
2	Vconn Tsd	VCONN TSD. Asserted if a TSD condition exists on VCONN.
1	VBUS Uvp	VBUS UVP. Asserted if a UVP condition exists on VBUS.
0	VBUS Ovp	VBUS OVP. Asserted if an OVP condition exists on VBUS.
Bytes 1-3: Reserved		
23:0	Reserved	Reserved

3.3 THERMAL ENG PWR STATUS Register (Address = 96h)

This RO register returns Thermal Foldback and VIN Engine Foldback status parameters. Please see Section 4.3 and Section 4.4 in the *TPS257XX-Q1-GUI Configuration Guide* for guidance on how to configure Thermal Foldback and VIN Engine Foldback parameters using the GUI. This register is global and is not specific to any individual port.

Table 3-3. THERMAL ENGPWR STAT Register Bit Field Descriptions

Bits	Name	Description	
15:11	Reserved	Reserved	
10:8	ENG Pwr Phase Status	000b	RANGE 1 - No VBUS Power.
		001b	RANGE 2 - User Defined VBUS Power. Grace Period starts.
		010b	RANGE 3 - User Defined VBUS Power. After Grace Period timer expiration
		011b	RANGE 4 - Full VBUS Power
		1xxb	Reserved
7:3	Reserved	Reserved	
2:0	Thermal Phase Status	000b	Normal operation
		001b	Thermal Foldback Phase 1
		010b	Thermal Foldback Phase 2
		011b	Thermal Foldback Phase 3
		100b	Thermal Foldback Phase 4
		101b	Thermal Foldback Phase 5
		110b	Thermal Foldback Phase 6

3.4 DEVICE INFO Register (Address = 2Fh)

This RO register returns identification and version information for the TPS257xx-Q1 device and can be used for device identifcation, firmware validation, and diagnostic purposes. This register is global and is not specific to any individual port.

Table 3-4. DEVICE INFO Register Bit Field Descriptions

Bits	Name	Description
271:224	FW Build Version	example) "_0005"
223:128	FW Version	example) "FWF411.04.01"
127:72	HW Version	example) "HW00D0"
71:0	Device Name	example) "TPS25772"

3.5 CUSTOM ID (Version Control) Register (Address = 06h)

This RO register allows system designers to store a user-defined identifier associated with a specific firmware patch. Storing a custom patch ID enables clear version tracking across production units, service updates, and validation builds. Please see Appendix A in the *TPS257XX-Q1-GUI Configuration Guide* for detailed instructions on how to program a CUSTOM ID in the FW patch. When the host reads from the Port A target address (0x22 or 0x23), the register returns CUSTOM ID A. When the host reads from the Port B target address (0x26 or 0x27), the register returns CUSTOM ID B.

Table 3-5. Custom ID Register Bit Field Descriptions

Bits	Name	Description
63:0	CUSTOM ID	User-defined version control

4 Summary

By combining system telemetry with PD policy management and power path control into a single device, the TPS257xx-Q1 reduces design complexity while improving system reliability, diagnostics capability, and compliance with USB standards. Proper use of the telemetry registers described in this document allows designers to enhance safety, optimize performance, and simplify system-level validation.

5 References

1. Texas Instruments, *TPS25772-Q1 Automotive Dual USB Type-C® Power Delivery Controller with Buck-Boost Regulator* data sheet.
2. Texas Instruments, *TPS25763-Q1 Automotive Dual USB Type-C® Power Delivery Controller with Buck-Boost Regulator and DisplayPort Alt Mode* data sheet.
3. Texas Instruments, *TPS25762-Q1 Automotive USB Type-C® Power Delivery Controller with Buck-Boost Regulator* data sheet.
4. Texas Instruments, *TPS257XX-Q1-GUI Configuration Guide* user's guide.

6 Revision History

Changes from Revision * (March 2026) to Revision A (June 2026)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	2
• Revised UFP/DFP terminology to "Upstream Facing Port" and "Downstream Facing Port."	3
• Updated terminology for ENG Pwr Phase Status	4
• Added reference link to GUI configuration guide	6

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025