Application Note

Optimizing EMC in Isolated Designs: 10 PCB Techniques for CISPR and IEC Compliance

Ayush Mangla, Himalaya Pramanick, Varun Kumar

ABSTRACT

This application note outlines techniques to minimize emission and maximize immunity through the top ten PCB improvements, including capacitor placement, ferrite bead filters, and careful PCB grounding. This application note is designed using TI's signal isolators with integrated power, the ISOW64xx, ISOW308x, and ISOW1050 devices, but these techniques can be used in all other isolator designs for better EMC performance.

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1 Introduction

To achieve better EMC performance on the first design iteration—without potentially costly board re-spins—this application note presents multiple proven system-level techniques that reduce radiated and conducted emissions while improving immunity margins.

The techniques are referenced to the ISOW6441DWEEVM, ISOW3080DWEEVM, and ISOW1050DWEEVM EVMs and applicable across the ISOW6441, ISOW3080, and ISOW1050 family of devices. Some of these techniques address the fundamental root causes of switching noise and must be implemented in every design, whereas other techniques are good to have to enhance the performance further. These techniques can be used in any design with isolators for better EMC performance.

- HF decoupling capacitor on pin 1 and pin 16
- Capacitor bank and relative placement
- Ferrite bead π-filter on supply rails
- Isolated copper island (KOZ) under ferrite beads
- Common-mode choke on communication bus (for example, CAN/RS-485)
- Post island capacitor
- Series resistors or low-pass filter on I/O traces
- Y-capacitor between GND1 and GND2 (safety-critical)
- Interlayer capacitor (substrate capacitor in isolation region)
- 100μF bulk capacitor at VDD input rail

2 Enhancing EMC Performance Through Board Design Techniques

2.1 HF Decoupling Capacitor on Pin 1 and Pin 16

The integrated DC-DC converter switches at ≅60MHz. This frequency (60MHz) along with all harmonic frequencies appear in both radiated and conducted emissions spectrum. A 100nF X7R ceramic capacitor placed directly at VDD (pin 1) and VISO (pin 16) provides a low-impedance shunt path at the fundamental frequency. The capacitor must be placed symmetrically between the supply and ground pin on both sides so that effective inductance from the device supply pin to the capacitance terminal is the same as the device ground pin to the capacitance terminal. (Refer to C27 and C28 placement in the ISOW1050DWEEVM evaluation module).

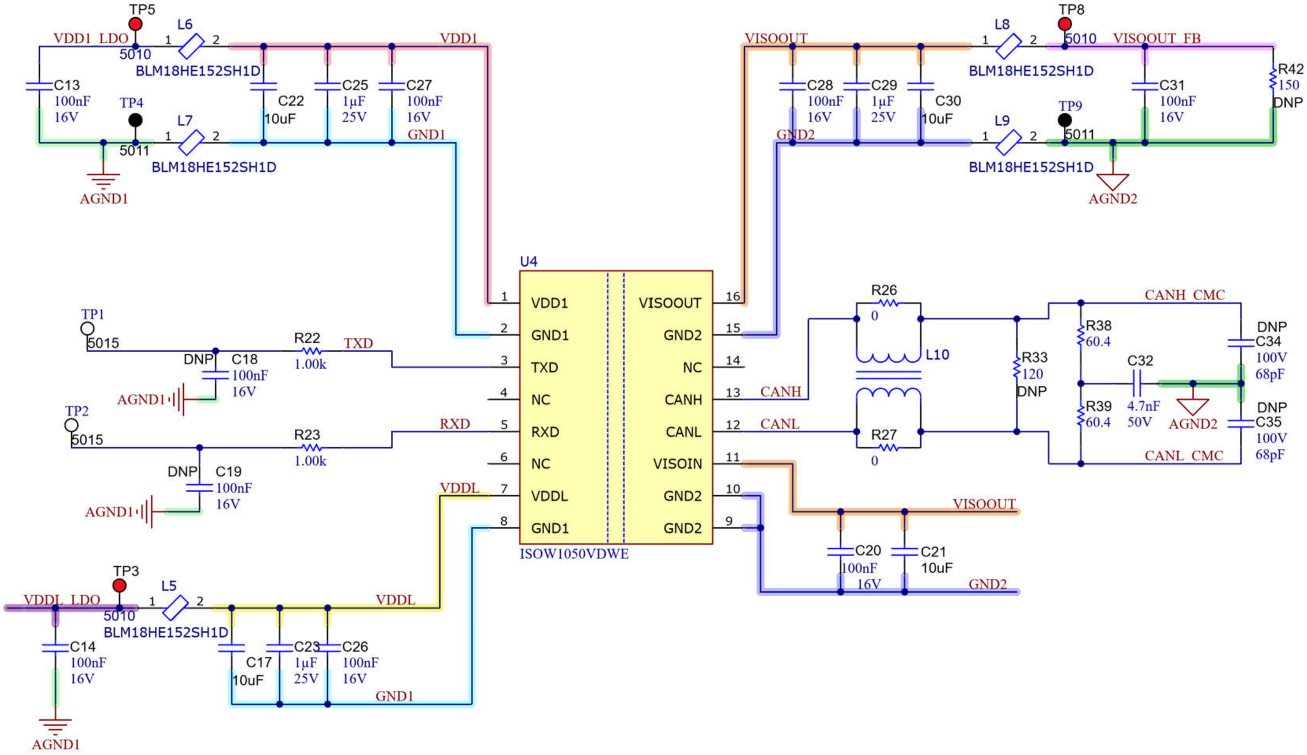

Figure 2-1. Schematic Reference From the ISOW1050DWEEVM Evaluation Module for the Mentioned Techniques

EMC performance can be further enhanced by using a reverse geometry capacitance (for example 0306YD104KAT2A, see references) or 10nF capacitance (for example GCM155L81E103KA37D, see references) which has much higher series resonant frequency (SRF) and lower equivalent series resistance and equivalent series inductance (ESL/ESR).

2.2 Capacitor Bank and Relative Placement

Proper capacitor stacking maintains low impedance across wide frequency bands:

- 60MHz (switching fundamental): 100nF handles this
- 1–30MHz (harmonics and common mode): 1µF provides the impedance floor
- < 1MHz (low-frequency transients): 10µF absorbs load step current

The correct order: Smallest → Largest, Closest → Farthest from the device under test (DUT):

Refer to capacitance banks [(C27, C25, C22) and (C28, C29, C30)] placement in Figure 2-1. The order is crucial because each mm of PCB trace between capacitor and IC adds ≅1nH of series inductance. By placing large 10µF capacitors closest to the IC and small 100nF capacitors farthest from the IC, this inverts the impedance profile and results in poor HF noise shunting. For applications targeting lower supply ripple, increasing the bulk capacitor from the standard 10µF to 22µF or 47µF helps to improve supply ripple.

2.3 Ferrite Bead π-Filter on Supply Rails

Without filtering the switching noise, the noise directly propagates into the VDD supply planes and the PCB ground planes. This action results in conducted emissions on the input terminal, and noise in the ground planes leads to radiated emissions. A ferrite bead π-filter blocks all noise above the cutoff frequency, preventing the fundamental frequency and all harmonic frequencies from reaching the main board copper planes. Use of a ferrite bead (FB) (for example, BLM18HE152SH1D, see references) is vital in minimizing radiated emissions due to common-mode current loops. FBs can be inserted between the DUT DC-DC converter and the rest of the system, as placed in Figure 2-1, thereby breaking the path of larger common-mode current loops and limiting formation of only shorter current loops. The cutoff frequency is calculated as:

$$\mathrm{Fc} = 1 \div (2\pi \times \sqrt{(\mathrm{L} \times \mathrm{C\_eff})}) \tag{1}$$

Two ferrite beads per rail (one on the supply line, one on the return or GND) helps in balanced differential filtering, as shown in Figure 2-1. (L6, L7 on VDD and L8, L9 on VISO).

2.4 Isolated Copper Island (KOZ) Under Ferrite Beads

Ferrite beads attenuate and block formation of large common-mode current loops. While FBs separate out the device from the rest of the PCB, all the power and ground planes before and after FBs must stay separated all through the PCB. This prevents alternate common-mode current loops from forming, which are created through capacitive coupling between the planes, bypassing FBs. Even 0.1pF of parasitic capacitance between copper pours on opposite sides defeats the purpose of a ferrite bead. Figure 2-2 highlights the keep-out zones that separate the inner and outer planes with a good amount of space between them.

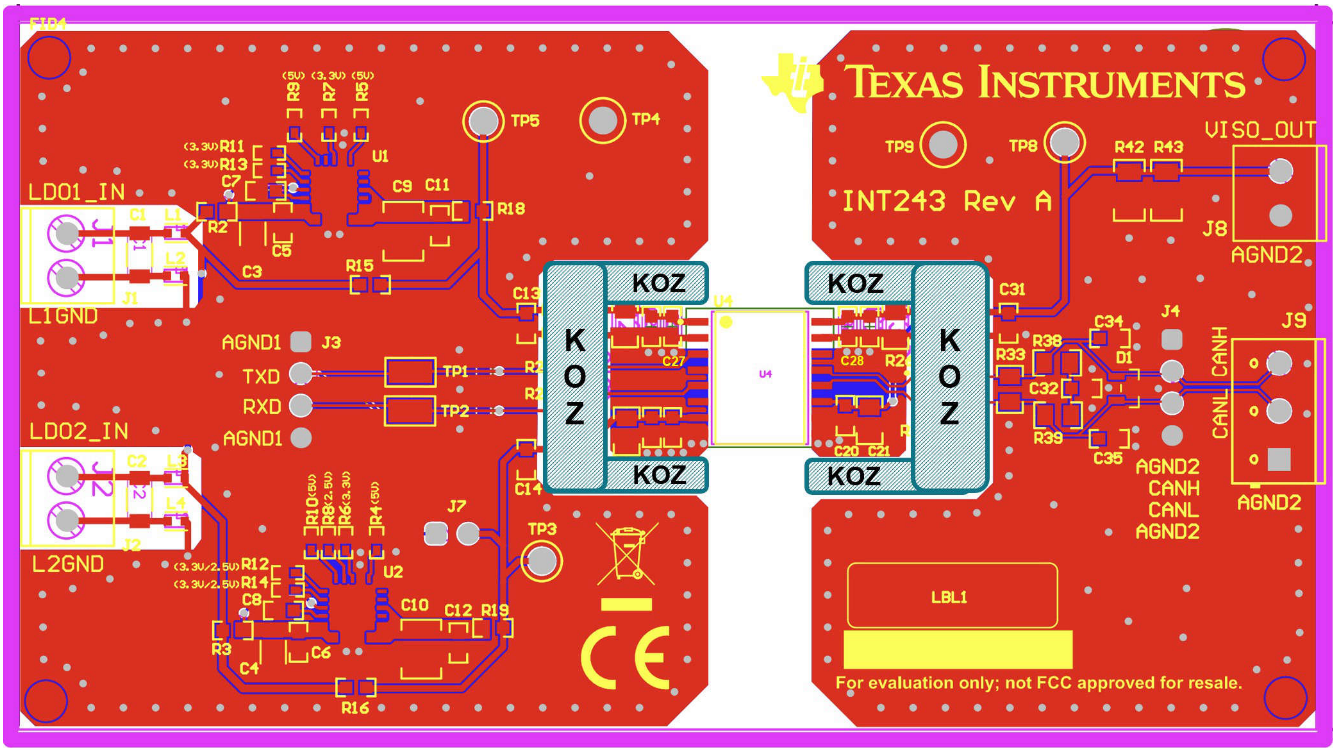

Figure 2-2. Layout Reference From the ISOW1050DWEEVM Board Showcasing KOZ

The ISOW6441, ISOW3080, ISOW1050 evaluation board shows deliberate gaps in the copper pour on both the top and bottom layers. This is an intentional keep-out zone to avoid parasitic capacitance.

2.5 Common-Mode Choke on the CAN/RS-485 Cable (ISOW3080 and ISOW1050 Device)

Isolated transceivers (ISOWRS485 – ISOW3080 and ISOWCAN – ISOW1050) have isolated output buses that connect through cables to external devices. The cables or wires connected to the system can pick up high-frequency switching noise from the converter and act as transmitter antennas; longer cables result in higher radiation levels. The answer to this outcome is to keep the common-mode current loop as small as possible by using common-mode chokes (CMC), which can be used for attenuating the common-mode noise. A CMC (for example, the ACT45B-101-2P-TL003, see references, and L10 in Figure 2-1) offers high impedance to common-mode currents while passing differential signals with minimal insertion loss. As a result, common mode noise from the ISOW output is blocked before reaching the cable; the differential data signal passes unaffected.

Position of the CMC is crucial—if the CMC is placed far from the connector, common mode noise gets coupled into PCB traces which defeats the purpose of the choke. For layout guidelines to follow for minimizing stray fringe capacitance between the choke terminals, refer to Figure 2-2. Refer to the ISOW1050DWEEVM evaluation module for a detailed layout.

2.6 Post Island Capacitor

Despite the isolated island (Section 2.4), some residual HF noise still crosses the ferrite bead region. Parasitic capacitance through the PCB substrate is unavoidable—meaning, small but non-zero. Capacitors (C13 and C31 in Figure 2-1 and Figure 2-2) are placed on the main-board GND side (after the ferrite output) to shunt this residual noise to local ground before the noise reaches the PCB ground planes. These capacitors directly improve both conducted emissions (CE) at the input terminals and radiated emissions (RE) from the PCB plane acting as an antenna. Placing capacitors on the main-board GND side also improves immunity to external conducted disturbances (radiated coupling into power input)

2.7 Series Resistors or Low-Pass Filter on I/O Traces

Fast digital edges on I/O traces carry significant harmonic energy up to several hundred MHz, depending on the data rate. When these lines route to off-board connectors or cables, the lines radiate directly. Series resistors limit edge slew rate, reducing harmonic amplitude. A resistor-capacitor (RC) or inductor-capacitor (LC) low-pass filter provides a defined cutoff frequency. There are many ways to control emissions through traces.

- Series resistor (≅1KΩ | R22, R23 in Figure 2-1): Slows edge rise time; reduces harmonic amplitude above signal frequency. As there is no dedicated capacitance in parallel, this option does not have any defined cutoff frequency.
- RC low pass filter: Adding a small capacitor (≅100pF) from the signal line to GND after the 1kΩ resistor creates a low pass filter. In cases where operation occurs at much lower data rates, the capacitor value can be increased further.
  - $F_C = 1 / (2\pi \times R \times C)$
- Ferrite bead + Capacitor: Replacing the series resistor with a ferrite bead paired with a capacitor to ground can be used to provide a complete high-rejection low-pass filter on every I/O line.
  - At signal frequencies (≤10Mbps): Ferrite looks like a small resistor (≅0.5Ω DC)
  - At switching convertor frequencies (≅60MHz): Ferrite presents > 1kΩ impedance—far better than a fixed resistor

2.8 Y-Capacitor Between GND1 and GND2 (Safety-Critical)

The ISOW DC-DC converter generates common-mode (CM) switching current that flows across the isolation barrier through parasitic capacitance (≅2pF). Without a controlled return path, this CM current:

- Flows from GND1 → PCB supply planes → cables and connectors → radiates (poor emissions)
- Couples into off-board circuits, causing immunity failures (poor immunity)

A safety-rated Y-capacitor bridges GND1 and GND2, providing a short, controlled local return path for CM current. The Y-capacitor bridges the isolation barrier. The Y-capacitor must be a safety-rated component certified to the IEC 60384-14 standard. Never use standard multilayer ceramic capacitors (MLCCs) across the isolation barrier as these capacitors are not safety-rated. Some examples of Y-capacitors are P101AA102M250 (1nF) and P101AA102M250 (4.7nF) (see references).

2.9 Interlayer Capacitor (Substrate Capacitor in the Isolation Region)

Using Y-capacitors on the printed circuit board (PCB) introduces lead inductance on both sides of the capacitor, in addition to the parasitic inductance of the capacitor, making the capacitor ineffective at frequencies higher than 200MHz. One way to create a low-inductance capacitance is by overlapping the internal PCB layers. This can be possible by a multilayer PCB layout. Extending the internal reference layers (GND and VCC) on either side of the isolation barrier (as shown in Figure 2-3) creates an overlap of internal layers. This overlap area, formed by the extension of the GND1 and VCC2 layers with FR4 material between the layers acting as a dielectric, creates a stitching capacitance between GND1 and VCC2.

Depending on whether the isolation requirement is functional, basic, or reinforced and depending on the working voltage, the spacing between the layers can be adjusted to achieve the capacitance value. Refer to the *Low-Emission Designs With ISOW7841 Integrated Signal* application report for an interlayer capacitance design example.

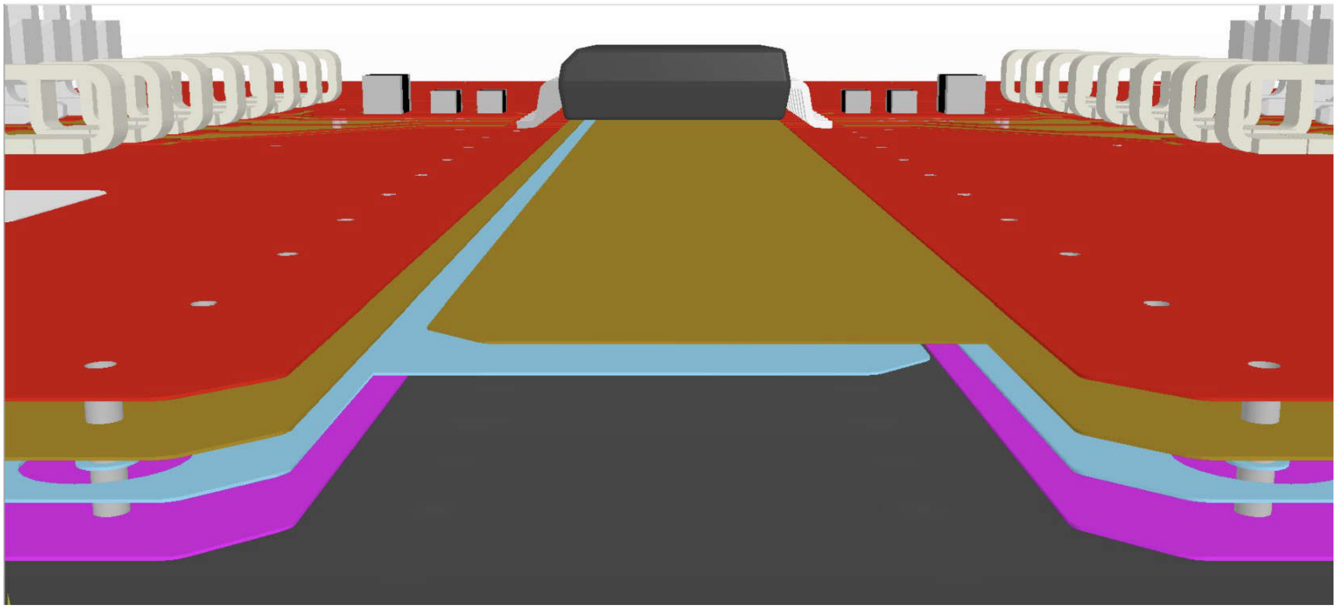

Figure 2-3. Diagram Showing Interlayer Capacitance Using PCB Layers

Extra care must be given at the edges of the PCB. At the edges, the planes can be exposed to air. Since opposite voltages come close to the edge of the board, these opposing voltages can potentially lead to electric field stress and then air breakdown along the edge.

2.10 100µF Bulk Capacitor at VDD Input Rail

The ISOW DC-DC converter draws pulsed current from the VDD rail. Without sufficient bulk capacitance, this draw creates voltage ripple on VDD that propagates upstream to other circuits sharing the same rail. This results in conducted emissions which measure input terminal voltage disturbance. Low frequency disturbances can be minimized by placing a 100µF capacitor (for example, T491X107K010AT, see references) at the VDD supply entry point—before the ferrite bead π-filter. This acts as a local charge reservoir, supplying pulsed current onboard so the disturbance does not propagate upstream.

A good practice is to try to avoid sharing the VDD supply rail with sensitive analog circuits (ADCs, op-amps, or PLLs). Even with 100µF, a residual switching ripple can potentially degrade analog performance. TI also advises to use a separate LDO (low-dropout regulator) or ferrite + capacitor filter for each sensitive circuit.

3 Summary

This application note suggested a comprehensive set of techniques to minimize radiated and conducted emissions, while maximizing immunity to external electromagnetic interference. These techniques include strategic placement of decoupling capacitors, ferrite bead π-filters, isolated copper islands, common-mode chokes, and Y-capacitors. These techniques emphasized the importance of PCB layout, referencing the ISOW6441DWEEVM, ISOW3080DWEEVM, and ISOW1050DWEEVM evaluation module designs as examples. These techniques can be applied to any design with isolators for achieving better EMC performance. Table 3-1 summarizes the EMC performance achieved with the ISOW64xx device using the techniques mentioned in this application note.

For more details on the EMC performance of this family of devices, refer to the *EMC Compliance Report: CISPR/IEC Test Results for Isolators With Integrated Power* application note.

Table 3-1. EMC Results for ISOW64xx

Test Type	Standard	Parameter	Level | Class	Result
Radiated Emission	CISPR 32	Industrial Radiated Emissions	Class B	PASS
	CISPR 25	Automotive Radiated Emissions	Class 5	PASS
Radiated Immunity	IEC 61000-4-3	Industrial Radiated Immunity	20V/m	PASS
	ISO11452-2	Automotive Radiated Immunity	100V/m	PASS
Conducted Immunity	IEC 61000-4-6	Conducted Immunity	15Vrms	PASS
Conducted Emission	CISPR 32	Conducted Emission	Class B	PASS
Magnetic Immunity	IEC 61000-4-8	Magnetic Field	100A/m (Level 5)	PASS
ESD	AEC Q100-002	HBM ESD	2kV	PASS
	AEC Q100-011	CDM ESD	1.5kV	PASS
	IEC 62368-1	Surge Isolation	10.4kV	PASS
CMTI	VDE 0884-17	Common Mode Transient Immunity	100kV/µs (Minimum); 200kV/µs (Typical)	PASS

4 References

1. Kemet, *P101AA102M250, Y-Capacitors*, datasheet.
2. Kemet, *T491X107K010AT, Tantalum Capacitors* , datasheet.
3. Kyocera, *0306YD104KAT2A, Reverse Geometry Capacitor*, datasheet.
4. Kyocera, *GCM155L81E103KA37D, 10nF Capacitor*, datasheet.
5. Murata, *BLM18HE152SH1D, Ferrite Bead*, product page.
6. TDK, *ACT45B-101-2P-TL003, Common mode Chokes*, datasheet.
7. Texas Instruments, *EMC Compliance Report: CISPR/IEC Test Results for Isolators With Integrated Power*, application note.
8. Texas Instruments, *Enhance Design Performance Using Integrated Power and Digital Isolation Design*, application brief.
9. Texas Instruments, *How to Meet CISPR 32 Radiated Emissions Limits With ISOW7741*, application brief.
10. Texas Instruments, *ISOW644x Robust-EMC, Reinforced, Quad-Channel Digital Isolator With Integrated DCDC Converter*, datasheet.
11. Texas Instruments, *ISOW308x Robust-EMC, Isolated RS-485/RS-422 Transceiver With Integrated DC-DC Converter*, datasheet.
12. Texas Instruments, *ISOW1050 Robust-EMC, Isolated CAN FD Transceiver With Integrated DC-DC Converter*, datasheet.
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15. Texas Instruments, *ISOW1050 EVM Datasheet for Layout Guidance*, evaluation module.
16. Texas Instruments, Low-Emission Designs With ISOW7841 Integrated Signal and Power Isolator, application note.
17. Texas Instruments, *Passing CISPR 25 Class-5 Automotive Radiated Emissions Using ISOW6441*, application note.
18. Texas Instruments, *Passing CISPR 32 Class-B Radiated Emissions With Ease Using ISOW6441*, application note.

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