Functional Safety Information

DRV8144-Q1 Half Bridge Driver Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for DRV8144-Q1 to aid in a functional safety system design. This document covers all the device package and interface variants as listed below:

1. HW variant in VQFN-HR package
2. SPI "S" variant in VQFN-HR package

Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA) for all the package and interface variants

Figure 1-1 shows the HW device variant's functional block diagram for reference.

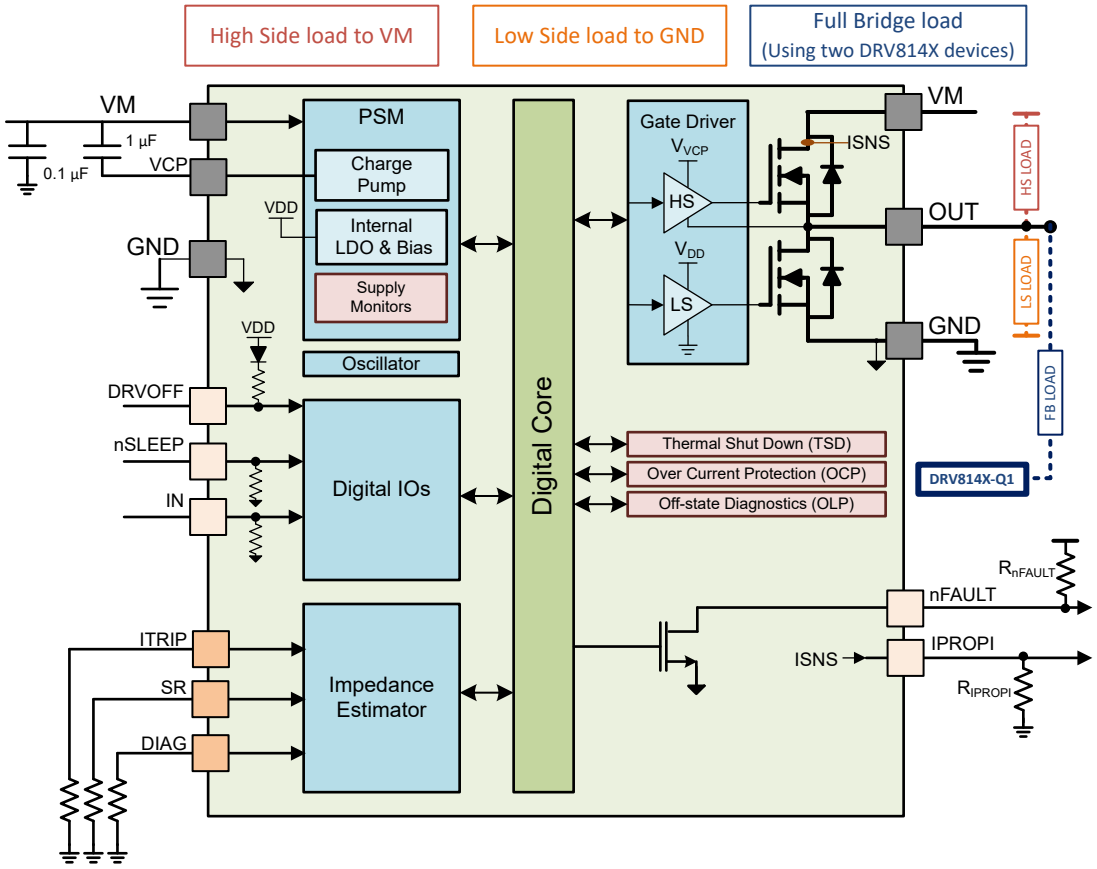

Figure 1-1. Functional Block Diagram for HW variant

Figure 1-2 shows the SPI "S" device variant's functional block diagram for reference.

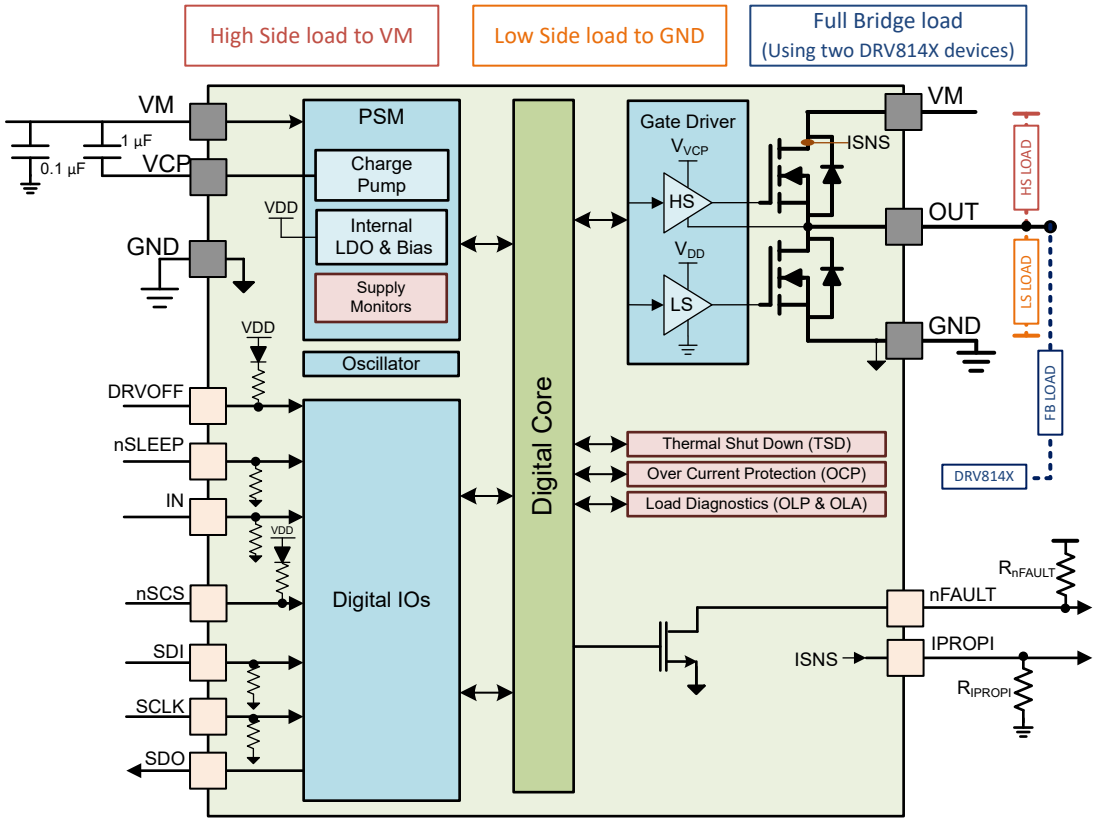

Figure 1-2. Functional Block Diagram for SPI "S" variant

Figure 1-3 shows the SPI "P" device variant's functional block diagram for reference.

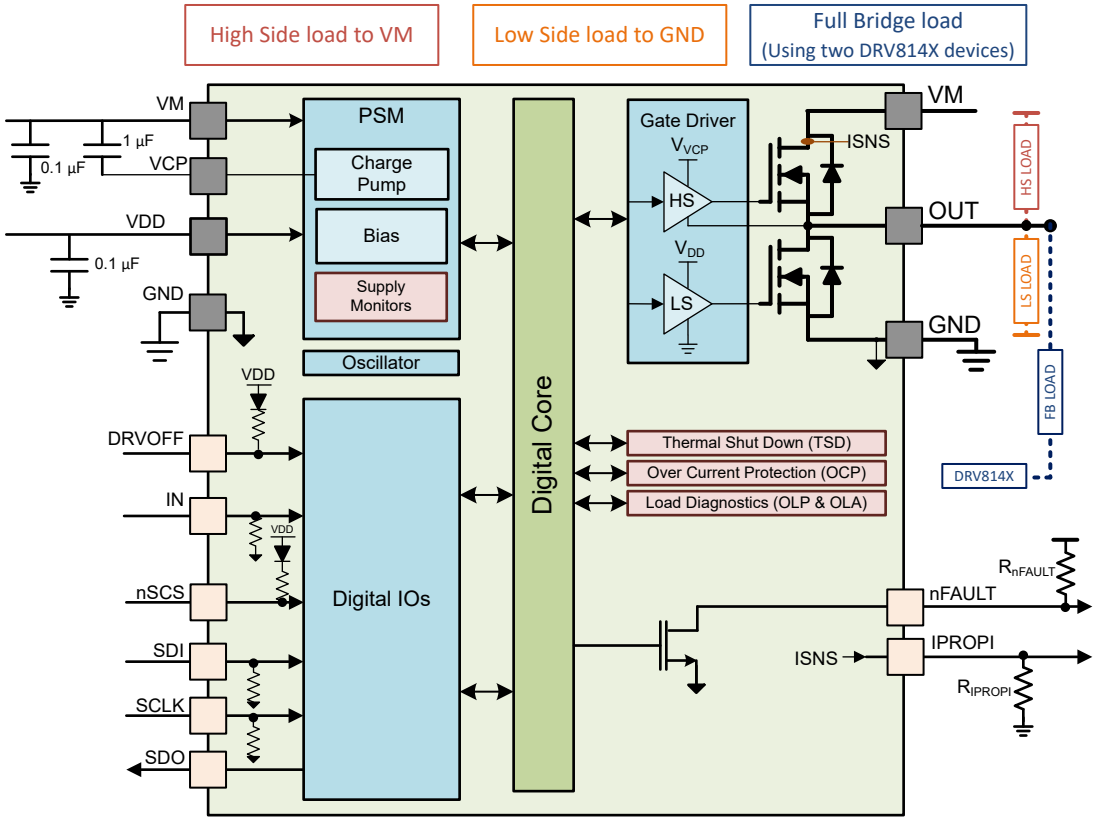

Figure 1-3. Functional Block Diagram for SPI "P" variant

DRV8144-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

ADVANCE INFORMATION for preproduction products; subject to change without notice.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for DRV8144-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)	
	HW variant in VQFN-HR package	SPI "S" variant in VQFN-HR package
Total Component FIT Rate	**25**	**25**
Die FIT Rate	**13**	**13**
Package FIT Rate	**12**	**12**

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 1150 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS,BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for DRV8144-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Output is stuck LOW when commanded OFF (GND short)	14%
Output is stuck HIGH when commanded OFF (VM short)	14%
Output is stuck OFF when commanded LOW (Open)	8%
Output is stuck OFF when commanded HIGH (Open)	8%
Output ON resistance too high when commanded LOW	12%
Output ON resistance too high when commanded HIGH	19%
Low side slew rate too fast or too slow (high-side recirculation)	5%
High side slew rate too fast or too slow (low-side recirculation)	5%
Dead-time is too short	1%
Current sense feedback incorrect	3%
ITRIP current regulation incorrect	3%
Incorrect communication (SPI variant)/ configuration interpretation (HW variant)	4%(1)
Incorrect input interpretation (nSLEEP, DRVOFF, IN)	3%(1)
Incorrect nFAULT assertion	1%

(1) 1% for each pin function

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) of the pins for each of the device variants of DRV8144-Q1 as listed below.

1. HW variant in VQFN-HR package
2. SPI "S" variant in VQFN-HR package

The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground
- Pin open-circuited
- Pin short-circuited to an adjacent pin
- Pin short-circuited to supply

The analysis also indicates how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

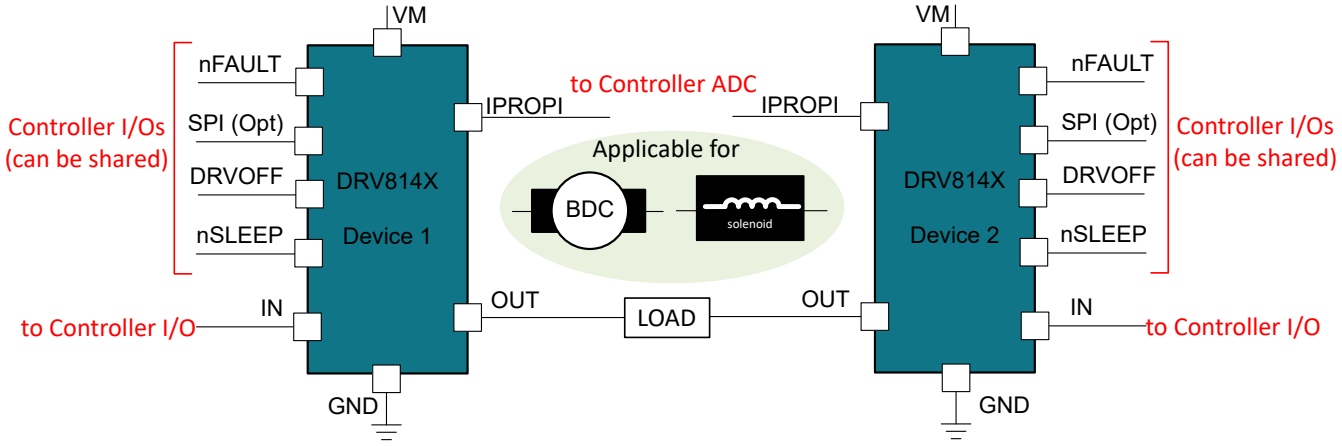

Figure 4-1. Using dual DRV814x-Q1 as a Full Bridge configuration with low-side recirculation

- Test conditions:
  - V_{VM} = 13.5 V, $T_{Ambient}$ = 25°C , SPI "P" variant: V_{VDD} = 5 V
- SPI "S" variant:
  - DRVOFF (pins combined) and IN pins controlled by controller
  - IPROPI (pins combined) monitored by controller, nFAULT (pins combined) monitoring optional
  - Configurations: SPI_IN unlocked with
    - DRVOFF_SEL = 1'b0 (Pin and register control for redundant shutoff)
    - IN_SEL for switching half bridge device = 1'b1 (Pin only control for PWM)
    - IN_SEL for non-switching half bridge device = 1'b0 (Register only control)
- HW variant:
- – nSLEEP, DRVOFF, EN/IN1, PH/IN2 pins controlled by controller
  - nFAULT and IPROPI pins monitored by controller
  - NC pin floating

4.1 SPI "S" variant in VQFN-HR package

Figure 4-2shows the pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the DRV8144-Q1 data sheet.

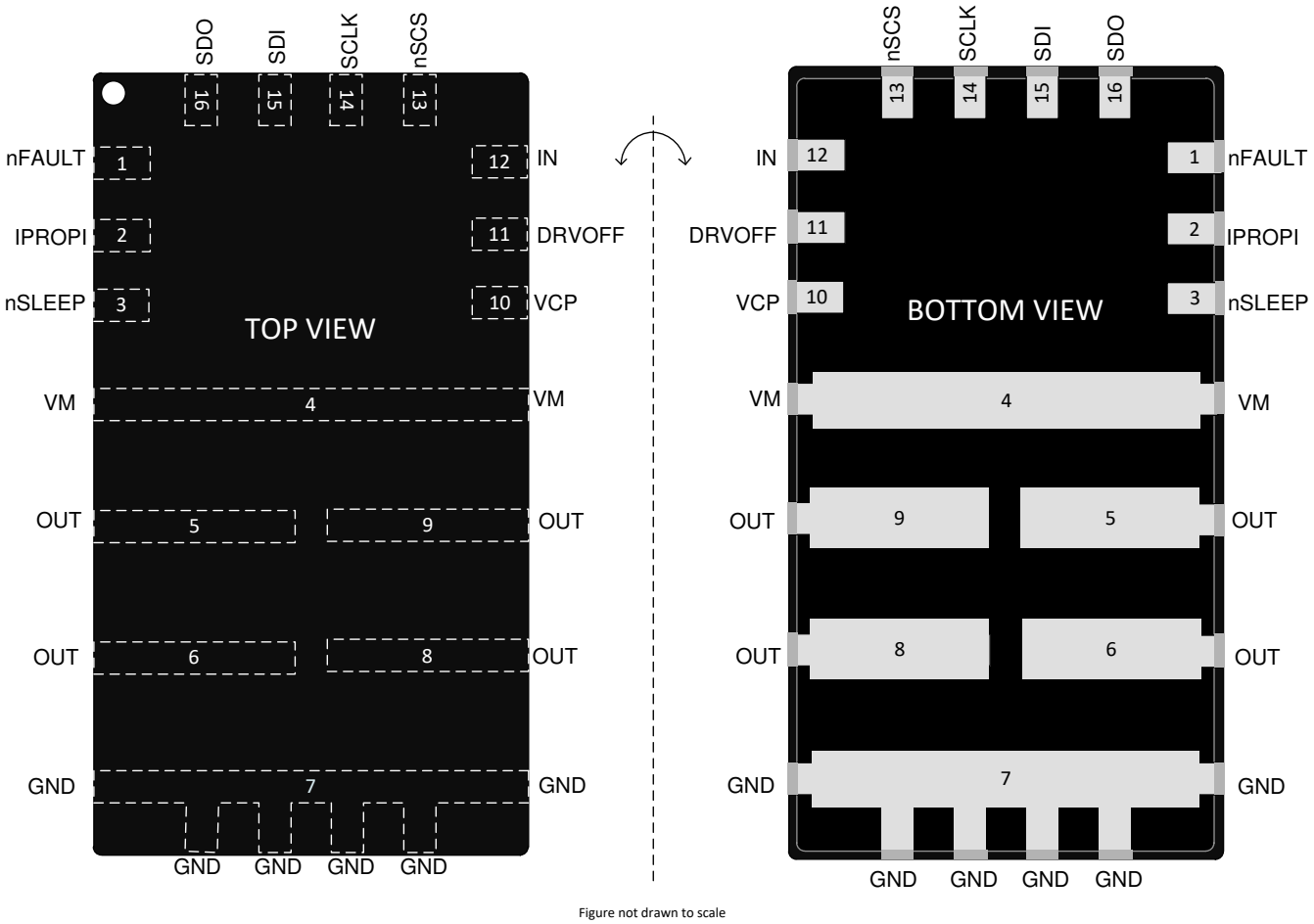

Figure 4-2. SPI "S" variant

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin		Description of Potential Failure Effect(s)	Failure Effect Class
No.	Name		
1	nFAULT	False fault signaling possible. Device will continue to operate as commanded.	B
2	IPROPI	IPROPI feedback is lost. ITRIP regulation, if enabled, is also lost.	B
3	nSLEEP	Device will be in SLEEP state and OUT is Hi-Z	B
4	VM	Device is powered off with driver Hi-Z.	B
5, 6	OUT	If OUT is commanded to be pulled high, short is detected and OUT is Hi-Z.	B
7	GND	Normal function.	D
8,9	OUT	If OUT is commanded to be pulled high, short is detected and OUT is Hi-Z.	B
10	**VCP**	**Device damage possible. Device behavior can not be guaranteed.**	**A**
11	DRVOFF	Pin based shutoff function is lost.	B
12	IN	External PWM control is lost. Internal ITRIP regulation is ok. No risk of spin direction reversal.	B
13	nSCS	SPI communication is lost.	B
14	SCLK	SPI communication is lost.	B
15	SDI	SPI communication is lost.	B

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin		Description of Potential Failure Effect(s)	Failure Effect Class
No.	Name		
16	SDO	SPI communication is lost.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin		Description of Potential Failure Effect(s)	Failure Effect Class
No.	Name		
1	nFAULT	False fault signaling possible. Device will continue to operate as commanded.	B
2	IPROPI	IPROPI feedback is lost. Load will be forced to recirculate if ITRIP regulation is enabled.	B
3	nSLEEP	Device will be in SLEEP state and OUT is Hi-Z.	B
4	VM	Device is powered off with driver Hi-Z.	B
5, 6	OUT	Load drive capability is lost.	B
7	GND	Normal function.	D
8,9	OUT	Load drive capability is lost.	B
10	VCP	The driver can't keep up with PWM frequency > 20 KHz	B
11	DRVOFF	Pin based shutoff is triggered and OUT is Hi-Z	B
12	IN	External PWM control is lost. Internal ITRIP regulation is OK. No risk of spin direction reversal.	B
13	nSCS	SPI communication is lost.	B
14	SCLK	SPI communication is lost.	B
15	SDI	SPI communication is lost.	B
16	SDO	SPI communication is lost.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Short between pins		Description of Potential Failure Effect(s)	Failure Effect Class
nFAULT	SDO	False fault signaling possible. SPI communication will be affected during fault assertion.	B
IPROPI	nFAULT	False fault signaling possible. IPROPI feedback is inaccurate. ITRIP regulation levels, if enabled, will be lower.	B
nSLEEP	IPROPI	ITRIP regulation levels, if enabled, will be lower.	B
VM	nSLEEP	SLEEP functionality is lost.	B
OUT	VM	If OUT is commanded to be pulled low, short is detected and OUT is Hi-Z.	B
GND	OUT	If OUT is commanded to be pulled high, short is detected and OUT is Hi-Z.	B
VCP	VM	Pull up path R_{ON} (High-side FET) will be much higher.	B
DRVOFF	**VCP**	**Device damage possible. Device behavior can not be guaranteed.**	**A**
IN	DRVOFF	Either OUT is Hi-Z or external PWM control is lost. Internal ITRIP regulation is ok. No risk of spin direction reversal.	B
nSCS	IN	SPI communication is affected. External PWM control is lost. Internal ITRIP regulation is OK. No risk of spin direction reversal.	B
SCLK	nSCS	SPI communication is lost.	B
SDI	SCLK	SPI communication is lost.	B
SDO	SDI	SPI communication is lost.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to VM

Pin		Description of Potential Failure Effect(s)	Failure Effect Class
No.	Name		
1	nFAULT	Device damage possible.	A
2	IPROPI	Device damage possible.	A
3	nSLEEP	SLEEP functionality is lost.	B
4	VM	Device is powered off with driver Hi-Z.	B
5, 6	OUT	If OUT is commanded to be pulled low, short is detected and OUT is Hi-Z.	B
7	GND	Normal function.	D
8,9	OUT	If OUT is commanded to be pulled low, short is detected and OUT is Hi-Z.	B
10	VCP	Pull up path R_{ON} (High-side FET) will be much higher.	B
11	DRVOFF	OUT is Hi-Z.	B
12	IN	Device damage possible.	A
13	nSCS	Device damage possible.	A
14	SCLK	Device damage possible.	A
15	SDI	Device damage possible.	A
16	SDO	Device damage possible.	A

4.2 HW variant in VQFN-HR package

Figure 4-3shows the pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the DRV8144-Q1 data sheet.

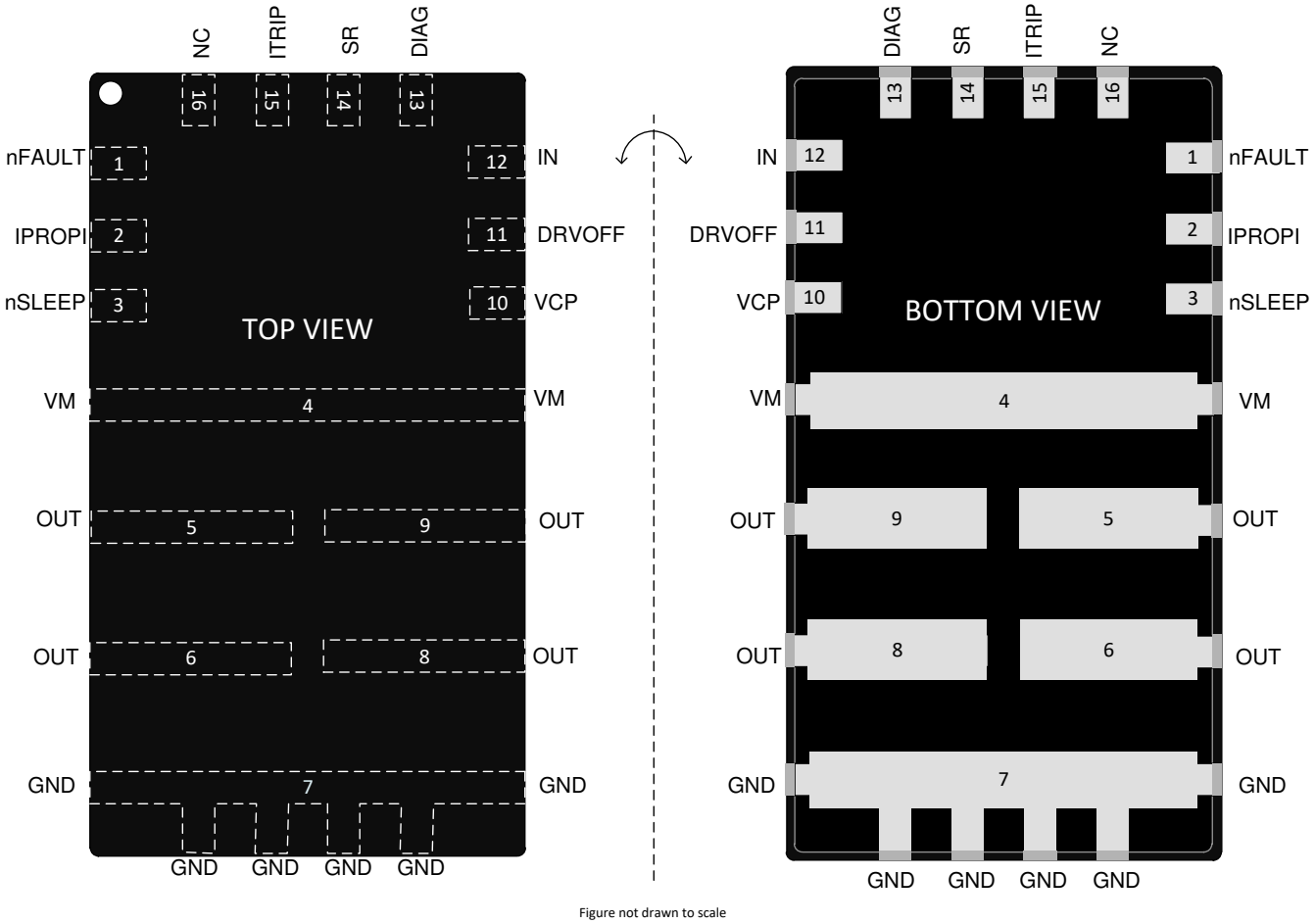

Figure 4-3. HW variant

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin		Description of Potential Failure Effect(s)	Failure Effect Class
No.	Name		
1	nFAULT	False fault signalling. Devie will continue to operate as commanded.	B
2	IPROPI	IPROPI feedback is lost. ITRIP regulation, if enabled, is also lost.	B
3	nSLEEP	Device will be in SLEEP state and outputs are Hi-Z	B
4	VM	Device is powered off with driver Hi-Z.	B
5, 6	OUT	If OUT is commanded to be pulled high, short is detected and OUT is Hi-Z.	B
7	GND	Normal function.	D
8, 9	OUT	If OUT is commanded to be pulled high, short is detected and OUT is Hi-Z.	B
10	**VCP**	**Device damage possible. Device behavior can not be guaranteed.**	**A**
11	DRVOFF	Shutoff function is lost.	B
12	IN	External PWM control is lost. Internal ITRIP regulation is ok. No risk of spin direction reversal.	B
13	DIAG	Wrong load and fault response configuration possible.	B
14	SR	Wrong SR configuration possible, EM performance may be affected.	B
15	ITRIP	Incorrect ITRIP level for current regulation possible.	B

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin		Description of Potential Failure Effect(s)	Failure Effect Class
No.	Name		
16	NC	Unused pin.	D

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin		Description of Potential Failure Effect(s)	Failure Effect Class
No.	Name		
1	nFAULT	False fault signalling. Devie will continue to operate as commanded.	B
2	IPROPI	IPROPI feedback is lost. Load will be forced to recirculte if ITRIP regulation is enabled.	B
3	nSLEEP	Device will be in SLEEP state and outputs are Hi-Z	B
4	VM	Device is powered off with driver Hi-Z.	B
5, 6	OUT	Load drive capability is lost.	B
7	GND	Normal function.	D
8, 9	OUT	Load drive capability is lost.	B
10	VCP	The driver can't keep up with PWM frequency > 20 KHz.	B
11	DRVOFF	Pin based shutoff is triggered and OUT is Hi-Z.	B
12	IN	External PWM control is lost. Internal ITRIP regulation is ok. No risk of spin direction reversal.	B
13	DIAG	Wrong load and fault response configuration possible.	B
14	SR	Wrong SR configuration possible, EM performance may be affected.	B
15	ITRIP	Incorrect ITRIP level for current regulation possible.	B
16	NC	Not used.	D

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Short between pins		Description of Potential Failure Effect(s)	Failure Effect Class
nFAULT	NC	Fault signaling function is unaffected.	D
IPROPI	nFAULT	False fault signaling possible. IPROPI feedback is inaccurate. ITRIP regulation levels, if enabled, will be lower.	B
nSLEEP	IPROPI	IPROPI feedback is inaccurate. ITRIP regulation levels, if enabled, will be lower.	B
VM	nSLEEP	SLEEP functionality is lost.	B
OUT	VM	If OUT is commanded to be pulled low, short is detected and OUT is Hi-Z.	B
GND	OUT	If OUT is commanded to be pulled high, short is detected and OUT is Hi-Z.	B
VCP	VM	Pull up path R_{ON} (High-side FET) will be much higher.	B
DRVOFF	**VCP**	**Device damage possible. Device behavior can not be guaranteed.**	**A**
IN	DRVOFF	Either OUT is Hi-Z or external PWM control is lost. Internal ITRIP regulation is ok. No risk of spin direction reversal.	B
DIAG	IN	Wrong load and fault response configuration possible. Internal ITRIP regulation is OK. No risk of spin direction reversal.	B
SR	DIAG	Wrong configuration - EM performance may be affected. Load and fault response may be incorrect.	B
ITRIP	SR	Wrong configuration - EM performance may be affected. Incorrect ITRIP level for current regulation possible.	B
NC	ITRIP	ITRIP setting is unaffected.	D

Table 4-9. Pin FMA for Device Pins Short-Circuited to VM

Pin		Description of Potential Failure Effect(s)	Failure Effect Class
No.	Name		
1	nFAULT	Device damage possible.	A

Table 4-9. Pin FMA for Device Pins Short-Circuited to VM (continued)

Pin		Description of Potential Failure Effect(s)	Failure Effect Class
No.	Name		
2	IPROPI	Device damage possible.	A
3	nSLEEP	SLEEP functionality is lost.	B
4	VM	Normal function.	D
5, 6	OUT	If OUT is commanded to be pulled low, short is detected and OUT is Hi-Z.	B
7	GND	Normal function.	D
8, 9	OUT	If OUT is commanded to be pulled low, short is detected and OUT is Hi-Z.	B
10	VCP	Pull up path R_{ON} (High-side FET) will be much higher.	B
11	DRVOFF	OUT is Hi-Z.	B
12	IN	Device damage possible.	A
13	DIAG	Device damage possible.	A
14	SR	Device damage possible.	A
15	ITRIP	Device damage possible.	A
16	NC	Device damage possible.	A

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