*Functional Safety Information*

# *TS5A23157-Q1*
# *Functional Safety FIT Rate, FMD and Pin FMA*

## Table of Contents

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# 1 Overview

This document contains information for TS5A23157-Q1 (VSSOP package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

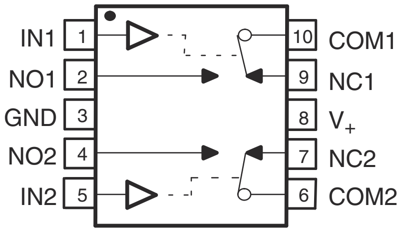

**Figure 1-1. Functional Block Diagram**

TS5A23157-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

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## 2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TS5A23157-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

**Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

| FIT IEC TR 62380 / ISO 26262 | FIT (Failures Per $10^9$ Hours) |
|---|---|
| Total Component FIT Rate | 7 |
| Die FIT Rate | 3 |
| Package FIT Rate | 4 |

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 100 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2**

| Table | Category | Reference FIT Rate | Reference Virtual $T_J$ |
|---|---|---|---|
| 5 | CMOS/BICMOS ASICs<br>Analog & Mixed = <50 V supply | 20 FIT | 55°C |

The Reference FIT Rate and Reference Virtual $T_J$ (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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# 3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TS5A23157-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

**Table 3-1. Die Failure Modes and Distribution**

| Die Failure Modes | Failure Mode Distribution (%) |
|---|---|
| NO or NC no output (Hi-Z) | 20% |
| NO or NC channel stuck on | 10% |
| NO or NC channel stuck off | 10% |
| NO or NC functional out of specification voltage or timing | 60% |

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

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# 4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TS5A23157-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

**Table 4-1. TI Classification of Failure Effects**

| Class | Failure Effects |
|---|---|
| A | Potential device damage that affects functionality |
| B | No device damage, but loss of functionality |
| C | No device damage, but performance degradation |
| D | No device damage, no impact to functionality or performance |

Figure 4-1 shows the TS5A23157-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TS5A23157-Q1 data sheet.

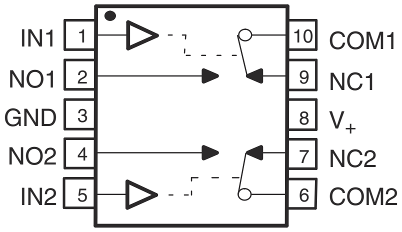

**Figure 4-1. Pin Diagram**

**Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| IN1 | 1 | IN stuck low. Cannot control switch states. | B |
| NO1 | 2 | Corruption of analog signal. If there is no limiting resistor in the switch path device damage is possible. | A |
| GND | 3 | No effect, normal operation. | D |
| NO2 | 4 | Corruption of analog signal. If there is no limiting resistor in the switch path device damage is possible. | A |
| IN2 | 5 | IN stuck low. Cannot control switch states. | B |
| COM2 | 6 | Corruption of analog signal. If there is no limiting resistor in the switch path device damage is possible. | A |
| NC2 | 7 | Corruption of analog signal. If there is no limiting resistor in the switch path device damage is possible. | A |
| V+ | 8 | Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible. | A |
| NC1 | 9 | Corruption of analog signal. If there is no limiting resistor in the switch path device damage is possible. | A |

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### Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| COM1 | 10 | Corruption of analog signal. If there is no limiting resistor in the switch path device damage is possible. | A |

### Table 4-3. Pin FMA for Device Pins Open-Circuited

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| IN1 | 1 | Loss of control of IN pin. Switch in undefined state. | B |
| NO1 | 2 | Corruption of analog signal. | B |
| GND | 3 | Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible. | A |
| NO2 | 4 | Corruption of analog signal. | B |
| IN2 | 5 | Loss of control of IN pin. Switch in undefined state. | B |
| COM2 | 6 | Corruption of analog signal. | B |
| NC2 | 7 | Corruption of analog signal. | B |
| V+ | 8 | Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible. | A |
| NC1 | 9 | Corruption of analog signal. | B |
| COM1 | 10 | Corruption of analog signal. | B |

### Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

| Pin Name | Pin No. | Shorted to | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|---|
| IN1 | 1 | NO1 | Loss of control of IN pin. Switch in undefined state. Possible corruption of analog signal. | B |
| NO1 | 2 | COM1 | Corruption of analog signal. If there is no limiting resistor in the switch path device damage is possible. | A |
| COM1 | 3 | NO2 | Corruption of analog signal. If there is no limiting resistor in the switch path device damage is possible. | A |
| NO2 | 4 | IN2 | Loss of control of IN pin. Switch in undefined state. Possible corruption of analog signal. | B |
| IN2 | 5 | COM2 | Not considered, Corner pin. | D |
| COM2 | 6 | NC2 | Corruption of analog signal. | B |
| NC2 | 7 | V+ | Corruption of analog signal. If there is no limiting resistor in the switch path device damage is possible. | A |
| V+ | 8 | NC1 | Corruption of analog signal. If there is no limiting resistor in the switch path device damage is possible. | A |
| NC1 | 9 | COM1 | Corruption of analog signal. | B |
| COM1 | 10 | IN1 | Not considered, Corner pin. | D |

### Table 4-5. Pin FMA for Device Pins Short-Circuited to VSSOP

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| IN1 | 1 | IN stuck to VDD. Cannot control switch states. | B |
| NO1 | 2 | Corruption of analog signal. If there is no limiting resistor in the switch path device damage is possible. | A |
| COM1 | 3 | Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible. | A |

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### Table 4-5. Pin FMA for Device Pins Short-Circuited to VSSOP (continued)

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| NO2 | 4 | Corruption of analog signal. If there is no limiting resistor in the switch path device damage is possible. | A |
| IN2 | 5 | IN stuck to VDD. Cannot control switch states. | B |
| COM2 | 6 | Corruption of analog signal. If there is no limiting resistor in the switch path device damage is possible. | A |
| NC2 | 7 | Corruption of analog signal. If there is no limiting resistor in the switch path device damage is possible. | A |
| V+ | 8 | No effect, normal operation | D |
| NC1 | 9 | Corruption of analog signal. If there is no limiting resistor in the switch path device damage is possible | A |
| COM1 | 10 | Corruption of analog signal. If there is no limiting resistor in the switch path device damage is possible | A |

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