Functional Safety Information

TLV1812, TLV1822 Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

All trademarks are the property of their respective owners.

1 Overview

This document contains information for TLV1812 and TLV1822 to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

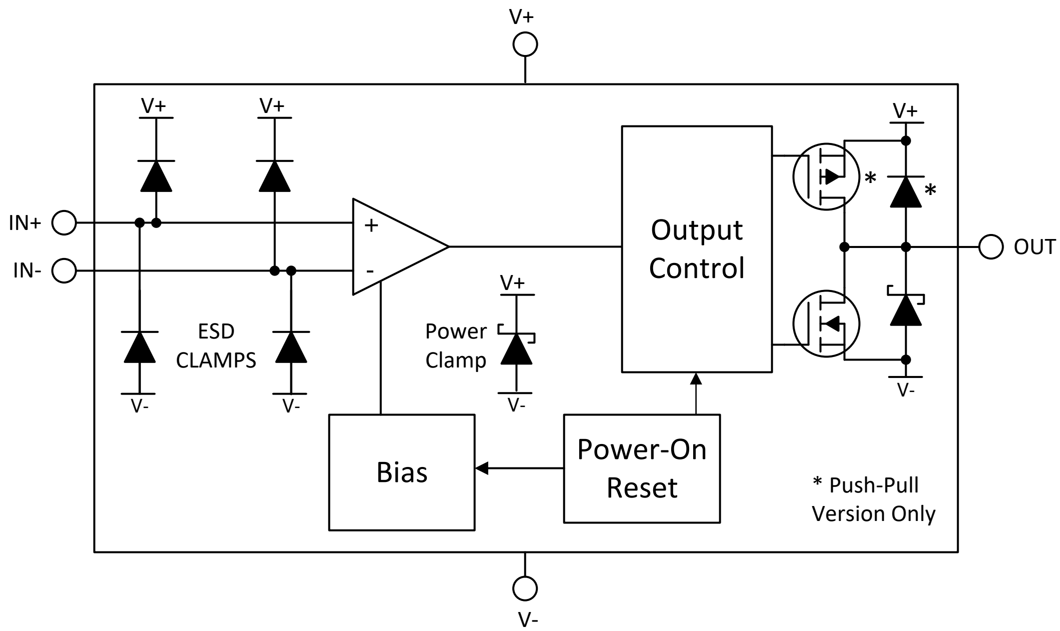

Figure 1-1. Functional Block Diagram

TLV1812 and TLV1822 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TLV1812 and TLV1822 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours) For SOIC (8) Package
Total Component FIT Rate5	10
Die FIT Rate	3
Package FIT Rate	7

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 0.25 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	CMOS, BICMOS Digital, analog / mixed	12	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TLV1812 and TLV1822 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUT Open (HIZ)	15%
OUT Saturate high	25%
OUT Saturate low	25%
OUT Functional not in specification	30%
Short Circuit any two pins	5%

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TLV1812 and TLV1822. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to V- (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply pin (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TLV1812 and TLV1822 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TLV1812 and TLV1822 data sheet.

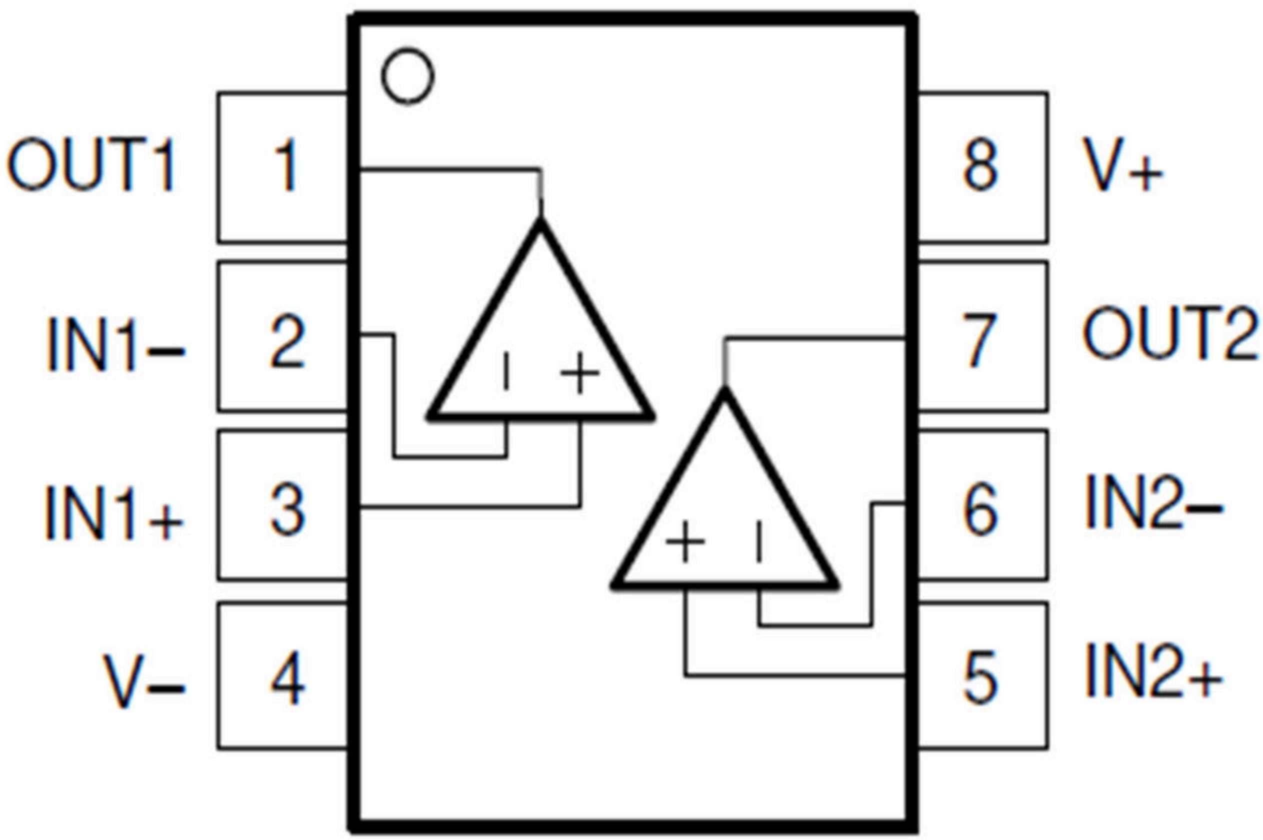

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Each pin is assessed individually
- All other pins are configured correctly for device functionality

Table 4-2. Pin FMA for Pins Short-Circuited to V-

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	Thermal stress due to high power dissipation (Push-Pull) No change if same node as V- (Open-Drain)	A B
IN1-	2	Output goes high, if other input is positive	B
IN1+	3	Output goes low, if other input is positive	B
V-	4	No change if same node as V-	D
IN2+	5	Output goes low, if other input is positive	B
IN2-	6	Output goes high, if other input is positive	B
OUT2	7	Thermal stress due to high power dissipation (Push-Pull) No change if same node as V- (Open-Drain)	A B
V+	8	Main supply shorted out (no power to device)	B

Table 4-3. Pin FMA for Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	Output can't drive application load	B
IN1-	2	Output may be low or high	B
IN1+	3	Output may be low or high	B
V-	4	Highest voltage pin will drive V- pin internally (via diode)	B
IN2+	5	Output may be low or high	B
IN2-	6	Output may be low or high	B
OUT2	7	Output can't drive application load	B
V+	8	Main supply open (no power to device)	B

Table 4-4. Pin FMA for Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1 to IN1-	1	2	Output may be low or high	B
IN1- to IN1+	2	3	Output may be low or high	B
IN1+ to V-	3	4	Output goes low, if other input is positive	B
V- to IN2+	4	5	Output goes low, if other input is positive	B
IN2+ to IN2-	5	6	Output may be low or high	B
In2- to OUT2	6	7	Output may be low or high	B
OUT2 to V+	7	8	Thermal stress due to high power dissipation	A
V+ to OUT1	8	1	Thermal stress due to high power dissipation	A

Table 4-5. Pin FMA for Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	Thermal stress due to high power dissipation	A
IN1-	2	Output goes low, if other input is less positive	B
IN1+	3	Output goes high, if other input is less positive	B
V-	4	Main supply shorted out (no power to device)	B
IN2+	5	Output goes high, if other input is less positive	B
IN2-	6	Output goes low, if other input is less positive	B
OUT2	7	Thermal stress due to high power dissipation	A
V+	8	No change if same node as V+	D