Functional Safety Information

AMC1351-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Table of Contents

Trademarks

1 Overview

This document contains information for the AMC1351-Q1 (SOIC package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

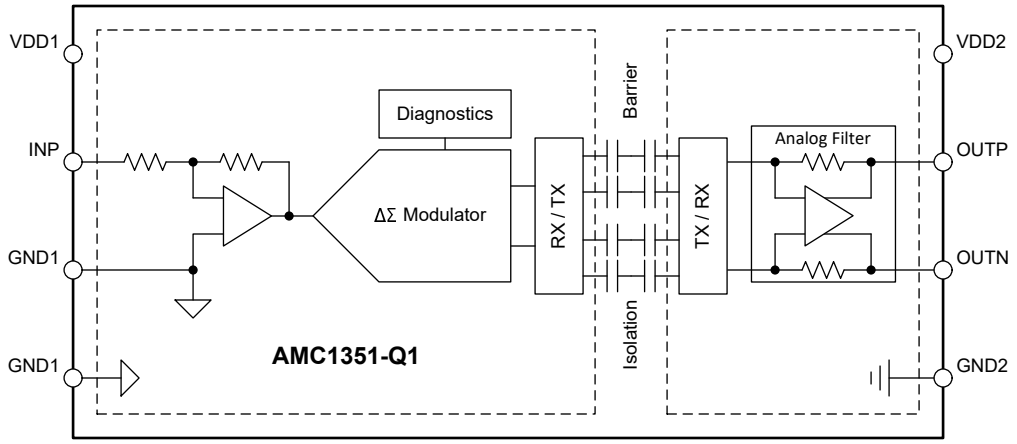

Figure 1-1. Functional Block Diagram

The AMC1351-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the AMC1351-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	17
Die FIT rate	3
Package FIT rate	14

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 96 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the AMC1351-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Output out of specification (gain error)	20%
Output out of specification (offset error)	20%
Output out of specification (differential output at positive or negative full scale)	20%
OUTN stuck high or low	10%
OUTP stuck high or low	10%
Reduced CMTI performance	9%
Output out of specification (spikes, increased noise)	5%
Device behavior undetermined	5%
Output fail-safe function fails to indicate an error(1)	1%

(1) Die faults that lead to a fail-safe indication of an error on the output are excluded.

The FMD in Table 3-1 excludes short-circuit faults across the isolation barrier. Faults for short circuits across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a safety-separated extra low voltage (SELV) or protective extra low voltage (PELV) power supply is used, pollution degree 2 / OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the AMC1351-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the AMC1351-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the AMC1351-Q1 data sheet.

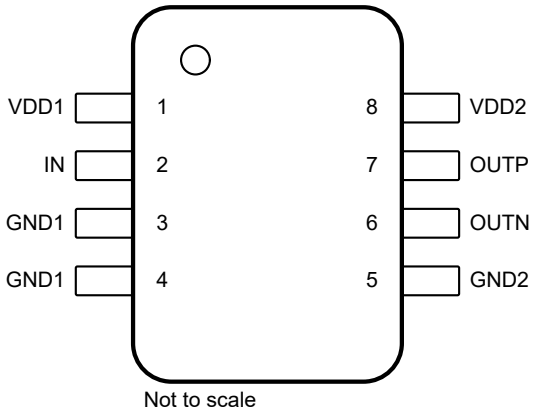

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- RC filter on IN.
  The series resistor is sized to limit the input current into IN to <10 mA under all circumstances (for example, if the device is unpowered and the input signal is applied).
- For pins on primary side:
  Short-circuited to ground means short to GND1.
  Short-circuited to supply means short to VDD1.
- For pins on secondary side:
  Short-circuited to ground means short to GND2.
  Short-circuited to supply means short to VDD2.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD1	1	Device primary side unpowered. Fail-safe output (see data sheet for more details). Observe that the absolute maximum ratings for the IN pin of the device is met, otherwise device damage may be plausible.	A
IN	2	IN stuck low (GND1). Differential output (V_{OUTP} – V_{OUTN}) = 0 V with common-mode voltage approximately 1.44 V.	B
GND1	3	No effect. Normal operation.	D
GND1	4	No effect. Normal operation.	D
GND2	5	No effect. Normal operation.	D
OUTN	6	OUTN stuck low (GND2). Excess current consumption from VDD2 source because of short-circuit condition. Device damage plausible if condition is present for extended period of time.	A
OUTP	7	OUTP stuck low (GND2). Excess current consumption from VDD2 source because of short-circuit condition. Device damage plausible if condition is present for extended period of time.	A
VDD2	8	Device secondary side unpowered. OUTP and OUTN pins are driven to GND2.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD1	1	Device primary side unpowered. Fail-safe output (see data sheet for more details).	B
INP	2	Differential output (V_{OUTP} – V_{OUTN}) undetermined.	B
GND1	3	Device input buffer is missing ground reference. Differential output (V_{OUTP} – V_{OUTN}) undetermined.	B
GND1	4	Device high side unpowered. Fail-safe output (see data sheet for more details).	B
GND2	5	Device behavior undetermined. V_{OUTN} and V_{OUTP} undetermined.	B
OUTN	6	Differential output (V_{OUTP} – V_{OUTN}) undetermined.	B
OUTP	7	Differential output (V_{OUTP} – V_{OUTN}) undetermined.	B
VDD2	8	Device secondary side unpowered. OUTP and OUTN pins are driven to GND2.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VDD1	1	IN	IN stuck high (VDD1). Differential output (V_{OUTP} – V_{OUTN}) = V_{VDD1} x 0.4.	B
IN	2	GND1	IN stuck low. Differential output (V_{OUTP} – V_{OUTN}) = 0 V.	B
GND1	3	GND1	No effect. Normal operation.	D
GND1	4	GND2	Not considered. Corner pin.	D
GND2	5	OUTN	OUTN stuck low (GND2). Excess current consumption from VDD2 source because of short-circuit condition. Device damage plausible if condition is present for extended period of time.	A
OUTN	6	OUTP	Differential output (V_{OUTP} – V_{OUTN}) = 0 V with common-mode voltage approximately 1.44 V. Excess current consumption from VDD2 source. Device damage plausible if condition is present for extended period of time.	A
OUTP	7	VDD2	OUTP stuck high (VDD2). Excess current consumption from VDD2 source. Device damage plausible if condition is present for extended period of time.	A
VDD2	8	VDD1	Not considered. Corner pin.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD1	1	No effect. Normal operation.	D
IN	2	IN stuck high (VDD1). Differential output (V_{OUTP} – V_{OUTN}) = V_{VDD1} x 0.4.	B
GND1	3	Incorrect ground reference for input buffer. Differential output (V_{OUTP} – V_{OUTN}) incorrect.	B
GND1	4	Device primary side unpowered. Fail-safe output (see data sheet for details). Observe that the absolute maximum ratings for IN is met, otherwise device damage may be plausible.	A
GND2	5	Device secondary side unpowered. OUTP and OUTN pins are driven to GND2.	B
OUTN	6	OUTN stuck high (VDD2). Excess current consumption from VDD2 source. Device damage plausible if condition is present for extended period of time.	A
OUTP	7	OUTP stuck high (VDD2). Excess current consumption from VDD2 source. Device damage plausible if condition is present for extended period of time.	A
VDD2	8	No effect. Normal operation.	D

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