Functional Safety Information

UCC28781-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the UCC28781-Q1 (RTW package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

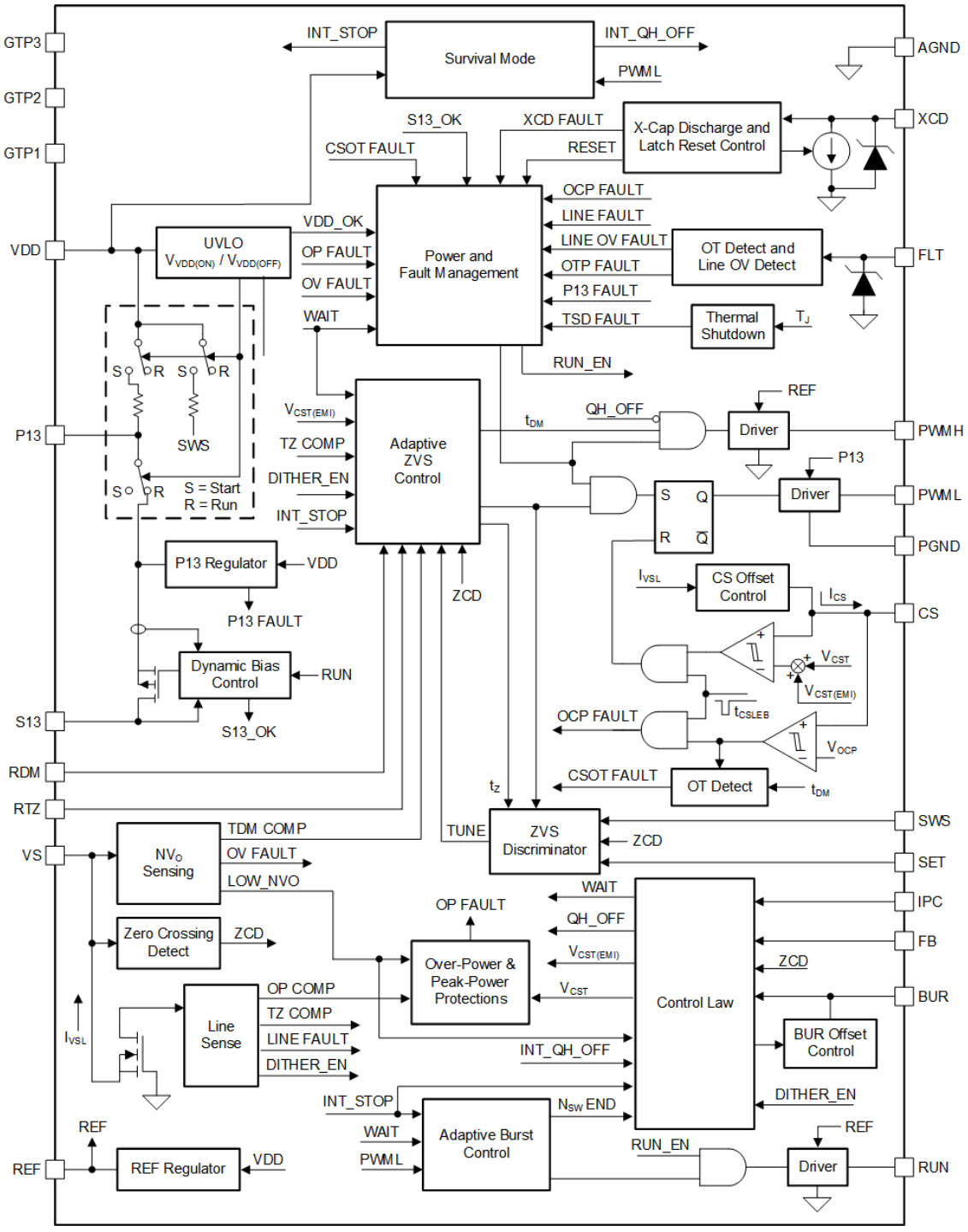

Figure 1-1. Functional Block Diagram

The UCC28781-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the UCC28781-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate (100 mW, 200 mW, 300 mW)	14, 14, 15
Die FIT rate (100 mW, 200 mW, 300 mW)	3, 3, 4
Package FIT rate (100 mW, 200 mW, 300 mW)	11, 11, 11

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: motor control from table 11
- Power dissipation: 100 mW, 200 mW, 300 mW
- Climate type: world-wide table 8
- Package factor (lambda 3): table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the UCC28781-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
PWML or PWMH wrong on-time	24
PWML or PWMH not switching	31
Lost x-cap discharge function	10
No effect	35

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the UCC28781-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the UCC28781-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the UCC28781-Q1 data sheet.

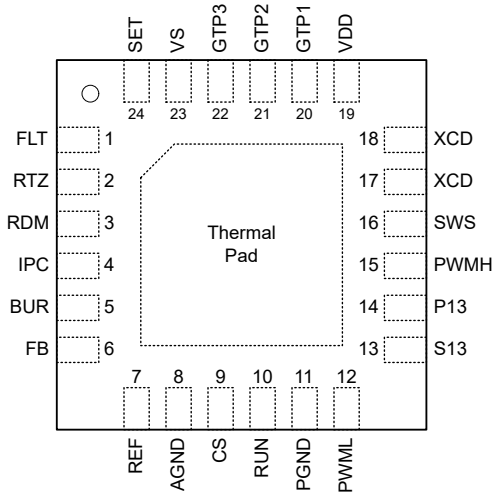

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- IC is set up according to the typical application circuit shown in UCC28781-Q1 datasheet Figure 11-1
- VDD pin is considered as the supply pin

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
FLT	1	IC enters fault mode, no PWML or PWMH output.	B
RTZ	2	Pin short protection. IC tries to restart. Converter has no output.	B
RDM	3	Pin short protection. IC tries to restart. Converter has no output.	B
IPC	4	No impact on operation. Converter operates with slightly lower efficiency at light load.	C
BUR	5	Burst mode threshold sets to minimum. Light load efficiency will be worse.	C
FB	6	Converter delivers minimum power. PWML with minimum on time. No PWMH output.	B
REF	7	No PWML or PWMH output. Converter has no output.	B
AGND	8	No effect.	D

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
CS	9	Controller enters CS pin short protection. IC tries to restart. Converter has no output.	B
RUN	10	VREF overload. IC shuts down and retries.	B
PGND	11	No effect.	D
PWML	12	PWML has no output. IC protects and retries after UVLO.	B
S13	13	No PWML or PWMH output. Converter has no output.	B
P13	14	No PWML or PWMH output. Converter has no output.	B
PWMH	15	VREF overload. IC shuts down and retries.	B
SWS	16	IC can't start up.	B
XCD	17	XCD function is lost. Possible damage on the line sensing device.	B
XCD	18	XCD function is lost. Possible damage on the line sensing device.	B
VDD	19	No PWML or PWMH output. Converter has no output.	B
GTP1	20	No effect.	D
GTP2	21	No effect.	D
GTP3	22	No effect.	D
VS	23	Controller enters brownout protection. IC enters UVLO mode and retries.	B
SET	24	Configure to GaN MOSFET. Either no impact, or converter operates with worse efficiency.	C

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
FLT	1	No impact on operation. IC loses FLT pin fault protection function.	C
RTZ	2	RTZ pin open pin protection. IC tries to restart. Converter has no output.	B
RDM	3	RDM pin open pin protection. IC tries to restart. Converter has no output.	B
IPC	4	No impact on operation. Converter operates with slightly higher efficiency at light load. Converter might have audible noise.	C
BUR	5	Burst level sets to highest. Burst mode threshold and the light load efficiency will be different.	C
FB	6	OVP is triggered. IC shuts down and retries.	B
REF	7	No effect. IC might shutdown due to the noise coupling into REF pin.	C
AGND	8	Behavior can be unpredictable. IC damage is possible.	A
CS	9	CS pin open protection. IC enters UVLO mode and retries.	B
RUN	10	No effect.	D
PGND	11	Behavior can be unpredictable. IC damage is possible.	A
PWML	12	Converter has no output.	B
S13	13	No effect.	D
P13	14	P13 pin open pin protection.	B
PWMH	15	No SR driver signal, converter operates with less efficiency. Power stage might get damaged.	C
SWS	16	IC does not start.	B
XCD	17	No effect.	D
XCD	18	No effect.	D
VDD	19	IC is not biased. No PWML or PWMH output.	B
GTP1	20	No effect.	D
GTP2	21	No effect.	D
GTP3	22	No effect.	D
VS	23	IC enters protection mode, shuts down and retries.	B
SET	24	IC sets to Si MOSFET mode. Either no impact or converter operates with worse efficiency	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
FLT	1	RTZ	RTZ pin setting is wrong. Converter efficiency will be lower. RTZ pin short protection is possible. IC loses FLT pin fault protection function.	C
RTZ	2	RDM	RDM pin open protection. IC tries to restart. Converter has no output.	B
RDM	3	IPC	RDM pin short protection. IC tries to restart. Converter has no output.	B
IPC	4	BUR	Burst level is lower than designed. Wrong burst threshold. Converter light load efficiency might be worse.	C
BUR	5	FB	Burst level is higher than designed. Wrong burst threshold. Converter light load efficiency might be different. The converter might reduce its maximum power handling capability.	C
FB	6	N/A	N/A	N/A
REF	7	AGND	No PWML or PWMH output. Converter has no output.	B
AGND	8	CS	IC enters CS pin short protection. IC enters UVLO mode and retries.	B
CS	9	RUN	IC shuts down and retries. Converter has no output.	B
RUN	10	PGND	VREF overload protection. IC shuts down and retries.	B
PGND	11	PWML	VREF overload protection. IC shuts down and retries.	B
PWML	12	N/A	N/A	N/A
S13	13	P13	No impact.	D
P13	14	PWMH	PWMH stays high. Possible IC and power stage damage.	A
PWMH	15	SWS	IC can't start up.	B
SWS	16	XCD	XCD function is lost.	C
XCD	17	XCD	No effect.	D
XCD	18	N/A	N/A	N/A
VDD	19	GTP1	IC is not biased. No PWML or PWMH output.	B
GTP1	20	GTP2	No effect.	D
GTP2	21	GTP3	No effect.	D
GTP3	22	VS	IC can't start up.	B
VS	23	SET	IC can't start up.	B
SET	24	N/A	N/A	N/A

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
FLT	1	IC enters protection mode. Possible IC damage.	A
RTZ	2	IC shuts down and retries. Possible IC damage.	A
RDM	3	IC shuts down and retries. Possible IC damage.	A
IPC	4	IC operates with higher peak current at light load mode. Possible IC damage.	A
BUR	5	IC shuts down and retries. Possible IC damage.	A
FB	6	IC triggers OVP protection. Possible IC damage.	A
REF	7	IC enters protection mode. Possible IC damage.	A
AGND	8	IC is not biased. No PWML or PWMH output. Converter has no output	B
CS	9	IC enters protection mode. Possible IC damage.	A
RUN	10	IC enters protection mode. Possible IC damage.	A
PGND	11	IC is not biased. No PWML or PWMH output. Converter has no output.	B
PWML	12	IC can't start up.	B
S13	13	IC can't start up.	B
P13	14	IC can't start up.	B
PWMH	15	IC can't start up.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SWS	16	IC tries to start up. Possible power stage damage.	B
XCD	17	XCD function is lost. Possible IC damage if VDD exceeds 30V.	A
XCD	18	XCD function is lost. Possible IC damage if VDD exceeds 30V.	A
VDD	19	No effect	D
GTP1	20	IC is not biased. No PWML or PWMH output. Converter has no output.	B
GTP2	21	IC is not biased. No PWML or PWMH output. Converter has no output.	B
GTP3	22	IC is not biased. No PWML or PWMH output. Converter has no output.	B
VS	23	OVP is triggered. IC shuts down and retries. Possible IC damage.	A
SET	24	IC sets to Si MOSFET mode. Possible IC damage.	A

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265