Functional Safety Information

TPS629xx-Q1
Functional Safety FIT Rate, FMD, and Pin FMA

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1 Overview

This document contains information for the TPS629xx-Q1 (VQFN package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

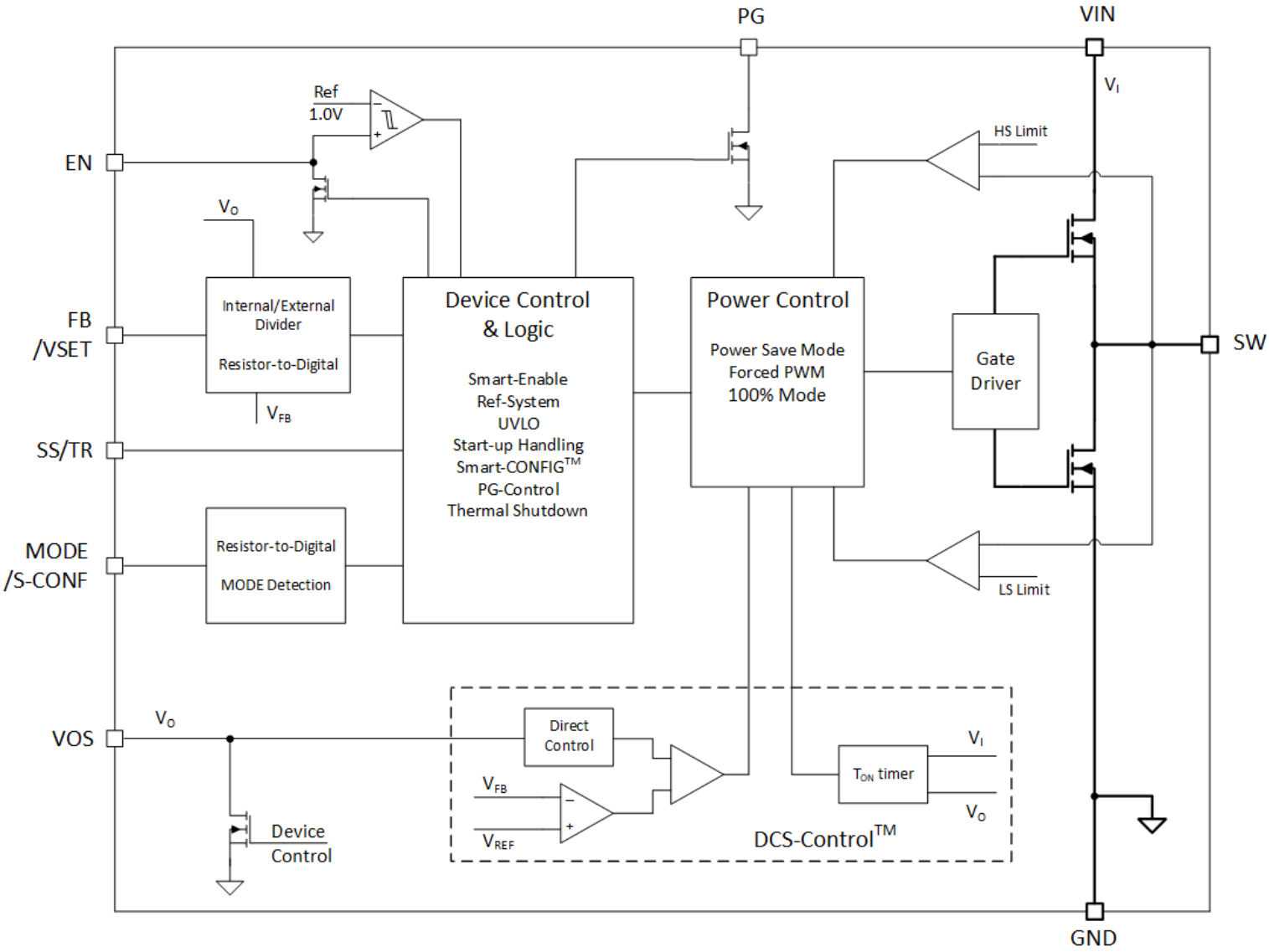

Figure 1-1. Functional Block Diagram

The TPS629xx-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TPS629xx-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)		
Power Dissipation	**0.5W**	**1.0W**	**1.5W**
Total Component FIT Rate	12	26	59
Die FIT Rate	8	22	55
Package FIT Rate	4	4	4

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Automotive control from table 11 or figure 16
- Power dissipation: 1500mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2T

Table	Category	Reference FIT Rate	Reference Virtual T_j
5	CMOS, BICMOS Digital, analog and mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_j (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS629xx-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
SW output not in specification – voltage	22
SW power HS or LS FET stuck on	20
Power FET damage	36
PG false trip or fails to trip	13
EN enable fails or false enable	9

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS629xx-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VIN (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TPS629xx-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS629xx-Q1 datasheet.

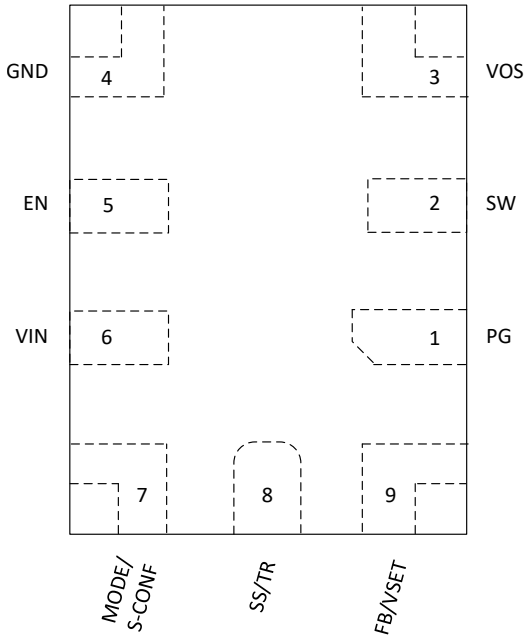

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device is operating in one of the two typical application configurations shown in Figure 4-2 or Figure 4-3.

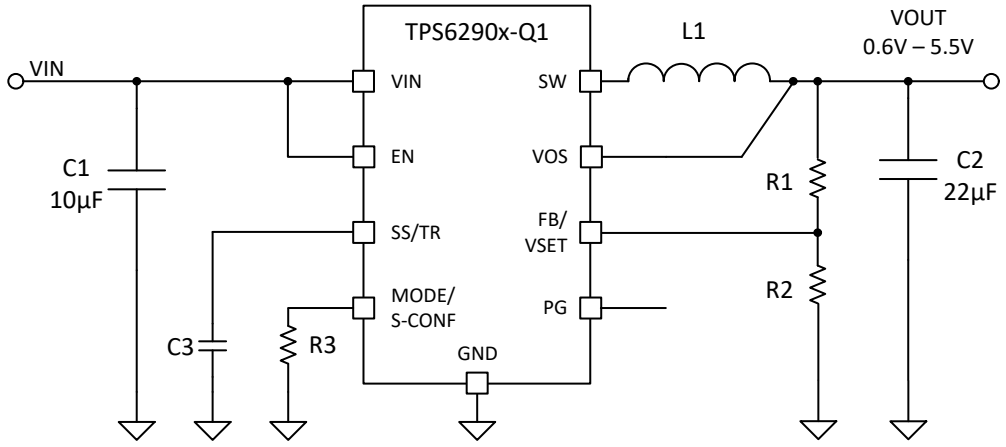

Figure 4-2. Adjustable V_O Operation Schematic

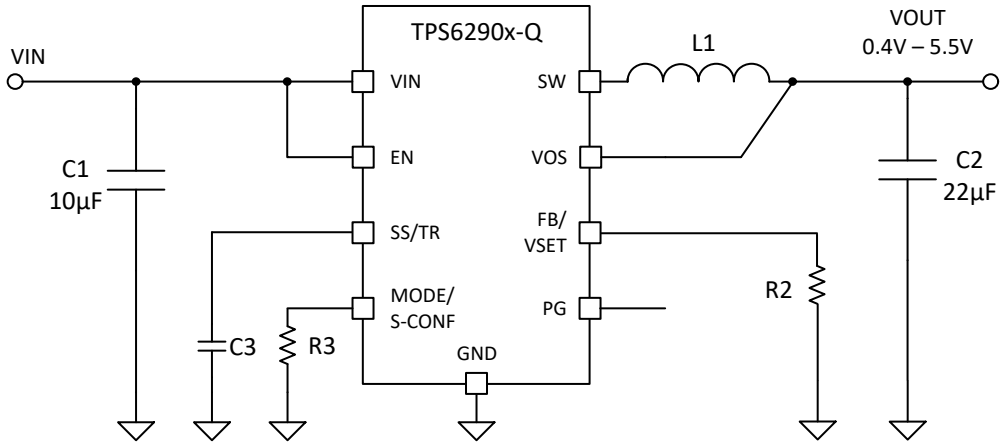

Figure 4-3. Selectable V_O Operation Schematic

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Application Configuration	Description of Potential Failure Effects	Failure Effect Class
PG	1		There is a loss of PG functionality.	C
SW	2		The device is possibly damaged.	A
VOS	3		There is a loss of the output voltage.	B
GND	4		This is the intended pin connection.	D
EN	5		The device does not power on.	B
VIN	6		The device does not power on.	B
MODE/S-CONF	7	External FB(3)	The device runs in 2.5MHz APFM with AEE mode.(5)	C(5)
		Internal FB(4)	There is a loss of output voltage regulation. The output voltage goes to V_{IN}.(5) The device is possibly damaged.(2) The absolute maximum voltage is potentially exceeded.	A(5)
SS/TR	8		The device does not power on.	B
FB/VSET	9	External FB(3)	There is a loss of output voltage regulation. The output voltage goes to V_{IN}. The device is possibly damaged.(2) The absolute maximum voltage is potentially exceeded.	A
		Internal FB(4)	The device regulates the output voltage to 1.2V.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Application Configuration	Description of Potential Failure Effects	Failure Effect Class
PG	1		There is a loss of PG functionality.	C
SW	2		There is a loss of output voltage regulation.	B
VOS	3	External FB(3)	Open loop operation. The behavior of the output voltage is undetermined.	B
		Internal FB(4)	There is a loss of output voltage regulation. The output voltage potentially goes to V_{IN}. The device is possibly damaged.(2) The absolute maximum voltage is potentially exceeded.	A
GND	4		The device is potentially damaged.	A
EN	5		The device does not power on.	B
VIN	6		The device does not power on.	B
MODE/S-CONF	7	External FB(3)	The device runs in 2.5MHz APFM with AEE mode(5). The output voltage is not set based on the external resistor divider ratio. Instead, V_{OUT} is set according to the internal FB (VSET) table based on the external feedback resistance values.	B(5)
		Internal FB(4)	The device runs in 2.5MHz APFM with AEE mode.(5)	C(5)
SS/TR	8		Allowable pin condition. The soft-start time is minimized.	D
FB/VSET	9	External FB(3)	There is a loss of output voltage regulation. The output voltage potentially goes to V_{IN}. The device is possibly damaged.(2) The absolute maximum voltage is potentially exceeded.	A
		Internal FB(4)	The device regulates the output voltage to 3.3V.	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Application Configuration	Description of Potential Failure Effects	Failure Effect Class
PG	1	SW		There is a loss of output voltage regulation and the device is possibly damaged.(1) The absolute maximum voltage is potentially exceeded if the PG pin is connected to the VOS pin through a resistor.	A
SW	2	VOS		There is a loss of output voltage regulation. The device is possibly damaged.(1) The absolute maximum voltage is potentially exceeded.	A
VOS	3	GND		There is a loss of the output voltage.	B
GND	4	EN		The device does not power on.	B
EN	5	VIN		The device cannot be disabled.	B
VIN	6	MODE/S_CONF	External FB(3)	The device runs in 2.5MHz FPFM mode.	C
			Internal FB(4)	There is a loss of output voltage regulation. The output voltage goes to V_{IN}.(5) The device is possibly damaged.(2) The absolute maximum voltage is potentially exceeded.	A
MODE/ S_CONF	7	SS/TR	External FB(3)	The device operating mode is indeterminate. (5)	B(5)
			Internal FB(4)	There is a loss of output voltage regulation. The device is possibly damaged.(1) The absolute maximum voltage is potentially exceeded.	A
SS/TR	8	FB/VSET		The output voltage is regulated below the target value.	B
FB/VSET	9	PG		There is a loss of output voltage regulation. The device is possibly damaged.(1) The absolute maximum voltage is potentially exceeded if the PG pin is connected to the VIN pin through a resistor.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN

Pin Name	Pin No.	Application Configuration	Description of Potential Failure Effects	Failure Effect Class
PG	1		The device is potential damaged. Absolute maximum current rating for the pin.	A
SW	2		The device is possibly damaged.(2) The absolute maximum voltage is potentially exceeded.	A
VOS	3		The device is possibly damaged.(1) The absolute maximum voltage is potentially exceeded.	A
GND	4		The device is not functional.	B
EN	5		The device cannot be disabled.	B
VIN	6		This is the intended pin connection.	D
MODE/S-CONF	7	External FB(3)	The device runs in 2.5MHz FPFM mode.(5)	C(5)
		Internal FB(4)	There is a loss of output voltage regulation. The output voltage goes to V_{IN}.(5) The device is potentially damaged.(2) The absolute maximum voltage is potentially exceeded.	A(5)
SS/TR	8		The device is potentially damaged. Absolute maximum current rating for pin.	A
FB/VSET	9		The device is device possibly damaged.(1) The absolute maximum voltage is potentially exceeded.	A

(1) Damage occurs if V_{IN} is greater than the 6V absolute maximum rating for the pin.
(2) Damage occurs if V_{IN} is greater than the 6V absolute maximum rating for the VOS pin.
(3) Applies to a typical application schematic as shown in Figure 4-2.
(4) Applies to a typical application schematic as shown in Figure 4-3.
(5) Assumes pin FMA condition occurs prior to the device being enabled. If a pin FMA condition occurs after the device is operating, the device continues operating as previously configured.

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from May 6, 2022 to July 16, 2026 (from Revision * (May 2022) to Revision A (July 2026)) **Page**

- Added bullet for the FMD information....2
- Added the *Failure Mode Distribution (FMD)* section....4

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