Functional Safety Information

OPT4001-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the OPT4001-Q1 (USON(6) package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

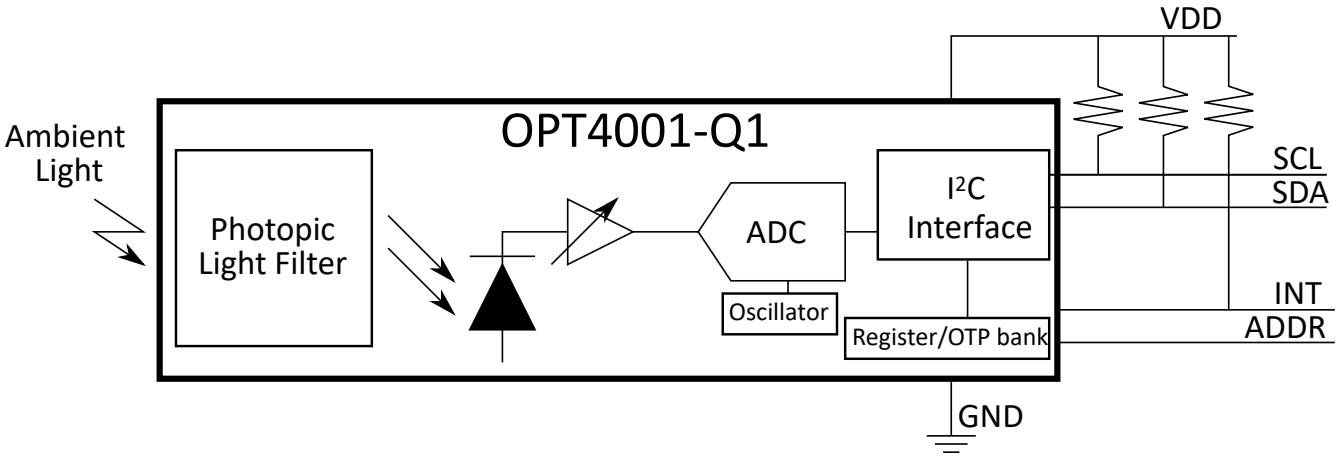

Figure 1-1. Functional Block Diagram

The OPT4001-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the OPT4001-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	4
Die FIT rate	2
Package FIT rate	2

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 0.1mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	60 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the OPT4001-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
I^2C communication error	10
Some output register bits stuck or false values	15
ADC offset in output measurement	15
Photodiode current out of specification	15
Control register bank data bit error	15
INT pin false trigger or fail to trigger	5
Optical filter characteristics changing over time	15
Device output reading out of specification	10

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the OPT4001-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the OPT4001-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the OPT4001-Q1 data sheet.

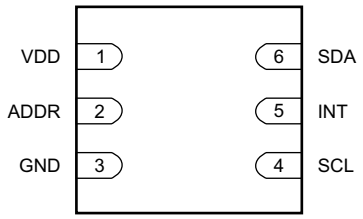

Figure 4-1. OPT4001-Q1 USON(6) Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device is the only target on the I^2C bus
- External pull-up resistor on SCL and SDA pins

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VDD	1	Device is not powered. Device is not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is plausible.	A
ADDR	2	Limited I^2C address selection. Communication can be corrupted.	B
GND	3	No Effect. Normal Operation.	D
SCL	4	No I^2C communication with the device is possible.	B
INT	5	Limited functionality of the device. Interrupt generation mechanism does not function and the device cannot indicate completion of conversion.	B
SDA	6	No I^2C communication with the device is possible.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VDD	1	Device functionality is undetermined. Device is not powered if all external analog and digital pins are held low.	B
ADDR	2	Limited address selection. I^2C communication can be corrupted.	B
GND	3	Device functionality is undetermined. Device can be not powered or connected to GND internally through an alternate pin ESD diode and power up.	B
SCL	4	No I^2C communication with the device is possible.	B
INT	5	Limited functionality of the device. Interrupt generation mechanism does not function and the device cannot indicate completion of conversion.	B
SDA	6	No I^2C communication with the device is possible.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
VDD	1	ADDR	Limited I^2C address selection. Communication can be corrupted.	B
ADDR	2	GND	Limited I^2C address selection. Communication can be corrupted.	B
SCL	4	INT	I^2C communication can be corrupted. Limited functionality of the device. Interrupt generation mechanism does not function and the device cannot indicate completion of conversion.	B
INT	5	SDA	I^2C communication can be corrupted. Limited functionality of the device. Interrupt generation mechanism does not function and the device cannot indicate completion of conversion.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VDD	1	No Effect. Normal Operation.	D
ADDR	2	Limited I^2C address selection. Communication can be corrupted.	B
GND	3	Device functionality is undetermined. Device is not powered if all external analog and digital pins are held low. Device can power up through internal ESD diodes to VDD if voltages are above the power-on reset threshold of the device and present on any of the analog or digital pins.	B
SCL	4	No I^2C communication with device is possible.	B
INT	5	Limited functionality of the device. Interrupt generation mechanism does not function and the device cannot indicate completion of conversion.	B
SDA	6	No I^2C communication with the device is possible.	B

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