Functional Safety Information

TPS7A16-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the TPS7A16-Q1 (HVSSOP package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

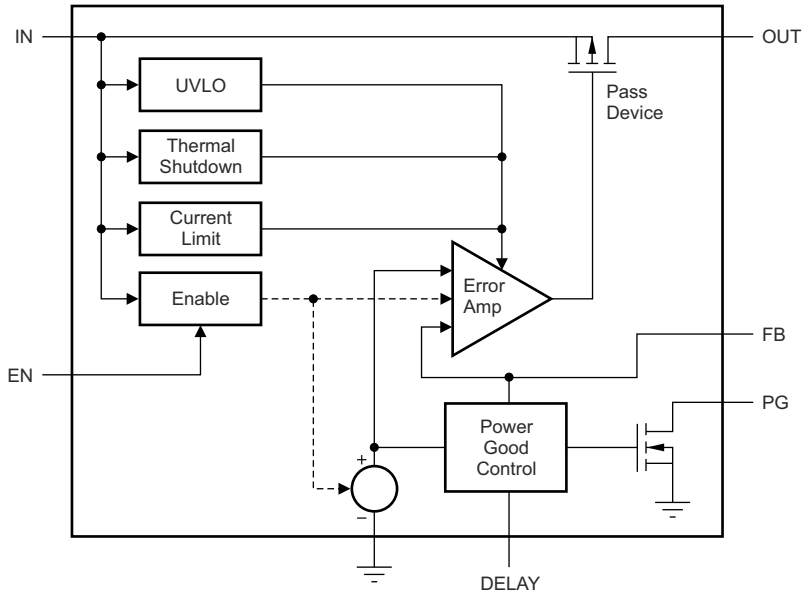

Figure 1-1. Functional Block Diagram

The TPS7A16-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TPS7A16-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	11
Die FIT rate	7
Package FIT rate	4

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 500 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	Power amplifier and regulator ≤ 1 Watt – (LDO)	40 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS7A16-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
V_{OUT} high (following V_{IN})	35
V_{OUT} not in specification	15
V_{OUT} low (no output)	35
PG false trigger, fails to trigger	10
Short circuit any two pins	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS7A16-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Pin FMA for Device Pins Open-Circuited)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TPS7A16-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS7A16-Q1 data sheet.

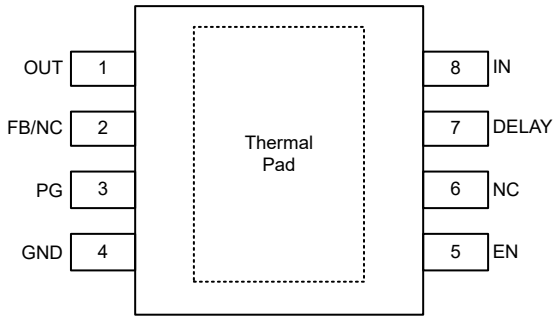

Figure 4-1. Pin Diagram

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Current limit is triggered, and the device can repeatedly enter and exit thermal shutdown depending on power dissipation.	B
FB/NC	2	(Fixed output.) No effect. Normal operation. (Adjustable output.) Output voltage is input voltage minus dropout voltage because the error amplifier drives the pass transistor gate to the rail.	B/D
PG	3	Power-good never asserts when the output voltage is at target, thus potentially effecting power sequencing	B
GND	4	No effect. Normal operation.	D
EN	5	The device is disabled, resulting in no output voltage.	B
NC	6	No effect. Normal operation.	D
DELAY	7	Ground current is permanently increased.	C
IN	8	Power is not supplied to the device. System performance depends on upstream current limiting.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	The device output is disconnected from the load.	B
FB/NC	2	(Fixed output.) No effect. Normal operation. (Adjustable output.) The error amplifier input is not connected. The output voltage is indeterminate.	D/B
PG	3	The power-good signal is not accessible. Power sequencing can be effected.	B
GND	4	There is no current loop for the supply voltage. The device is not operational and does not regulate.	B
EN	5	The enable circuit is in an unknown state. The device can be enabled or disabled.	B
NC	6	No effect. Normal operation.	D
DELAY	7	PG output is high-impedance when V_{OUT} is greater than the PG trip point without a time delay.	B
IN	8	Power is not supplied to the device, resulting in no output voltage.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
OUT	1	FB/NC (pin 2)	(Fixed output.) No effect. Normal operation. (Adjustable output.) The output voltage is equal to the internal reference voltage.	B/D
FB/NC	2	PG (pin 3)	(Fixed output.) No effect. Normal operation. (Adjustable output) Damage to the device as excess current can flow through PG pin.	D/A
PG	3	GND (pin 4)	Power-good never asserts when the output voltage is at target, thus potentially effecting power sequencing	B
EN	5	NC (pin 6)	No effect. Normal operation.	D
NC	6	DELAY (pin 7)	No effect. Normal operation.	D
DELAY	7	IN (pin 8)	PG can incorrectly assert when the output voltage is not at target. The pin absolute maximum rating (5.5 V max) can be exceeded and the pin can be damaged.	B/A

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Regulation is not possible. Damage is possible if the absolute maximum rating is exceeded (20 V max).	A
FB/NC	2	(Fixed output) No effect. Normal operation. (Adjustable output) If V_{IN} < 3.0 V and if there is any loading on the device, the output is approximately 0 V. If there is no load on the device, the output is equal to V_{IN}. Damage is possible if the absolute maximum rating is exceeded (3 V).	A/D
PG	3	Power-good functionality cannot operate correctly. PG can be damaged if the absolute maximum rating (5.5 V) is violated.	B/A
GND	4	Power is not supplied to the device. System performance depends on upstream current limiting.	B
EN	5	The device is always enabled when the input is powered.	B
NC	6	No effect. Normal operation.	D
DELAY	7	PG can incorrectly assert when the output voltage is not at target. The pin absolute maximum rating (5.5 V max) can be exceeded and the pin can be damaged.	B/A
IN	8	No effect. Normal operation.	D

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