Functional Safety Information

DP83TC813x-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for DP83TC813x-Q1 (VQFN package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

DP83TC813x-Q1 was developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

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2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for DP83TC813x-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	25
Die FIT rate	3
Package FIT rate	22

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 290 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	70 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for DP83TC813x-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Fault in MDI transmitter causing IEEE spec compliance issues.	8
Fault in MDI transmitter causing high RF emissions.	4
Fault in MDI receiver causing poor-link quality/link-loss.	8
Fault in internal power circuits causing poor link quality and higher power consumption.	12
Fault in internal clock circuits causing IEEE compliance issues and poor link-quality.	8
Fault in GPIO causing higher RF emissions.	8
Fault in GPIO causing Rgmii/JEDEC/Datasheet spec violation.	8
Fault in ESD on MDI making IEC ESD performance lower than 8 KV.	4
Fault in ESD on GPIOs making CDM performance lower than 2 KV.	4
Digital core has stuck or transient faults causing link-up or PCS faults.	36

The FMD in Table 3-1 excludes short-circuit faults across the isolation barrier. Faults for short circuits across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a safety-separated extra low voltage (SELV) or protective extra low voltage (PELV) power supply is used, pollution degree 2 / OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

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4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the DP83TC813x-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

Pin short-circuited to ground (seeTable 4-2)

- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5, Table 4-6, Table 4-7, and Table 4-8).

Table 4-2 through Table 4-8 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the DP83TC813x-Q1 data sheet.

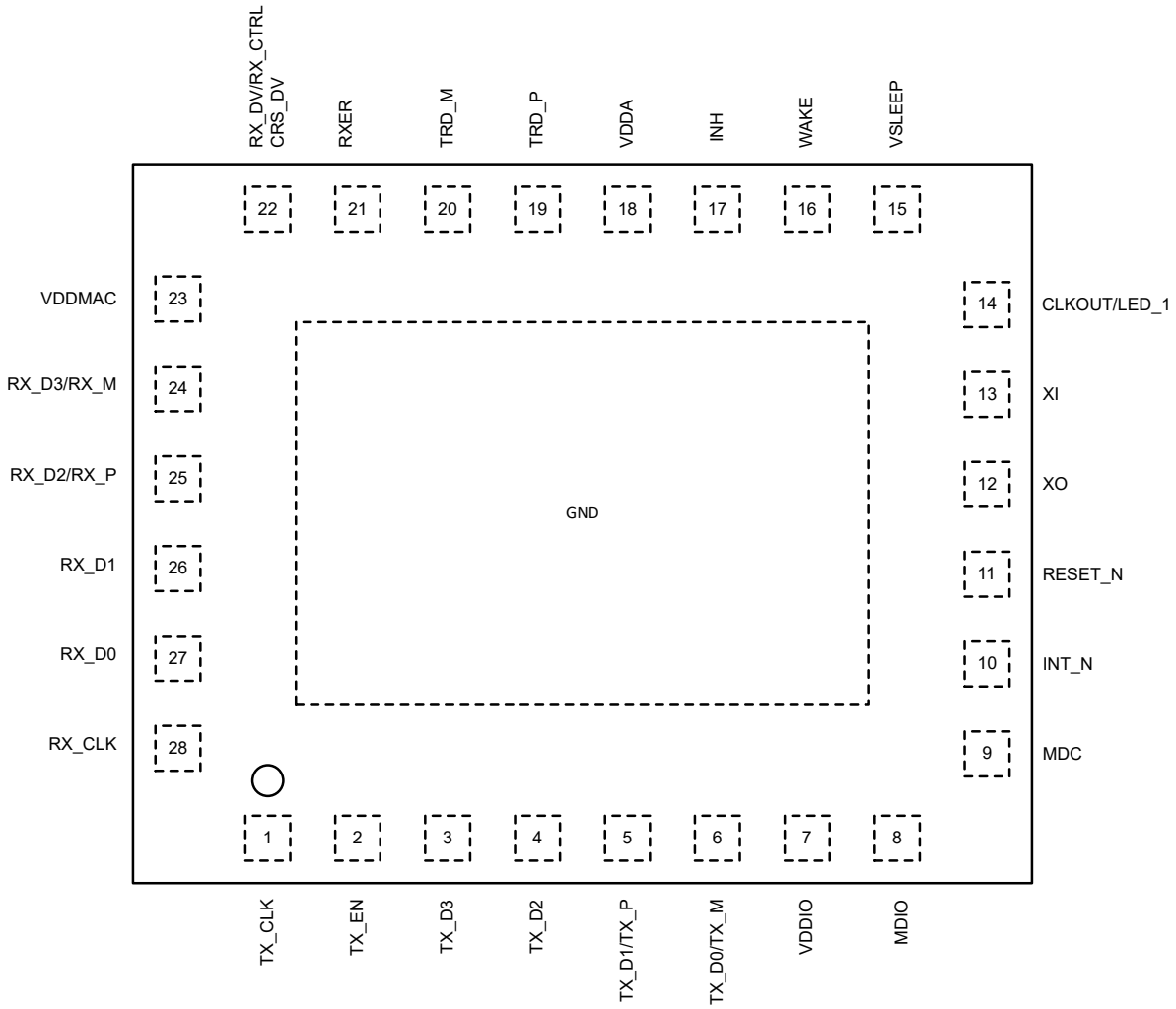

Figure 4-1. DP83TC813S-Q1 Pin Diagram

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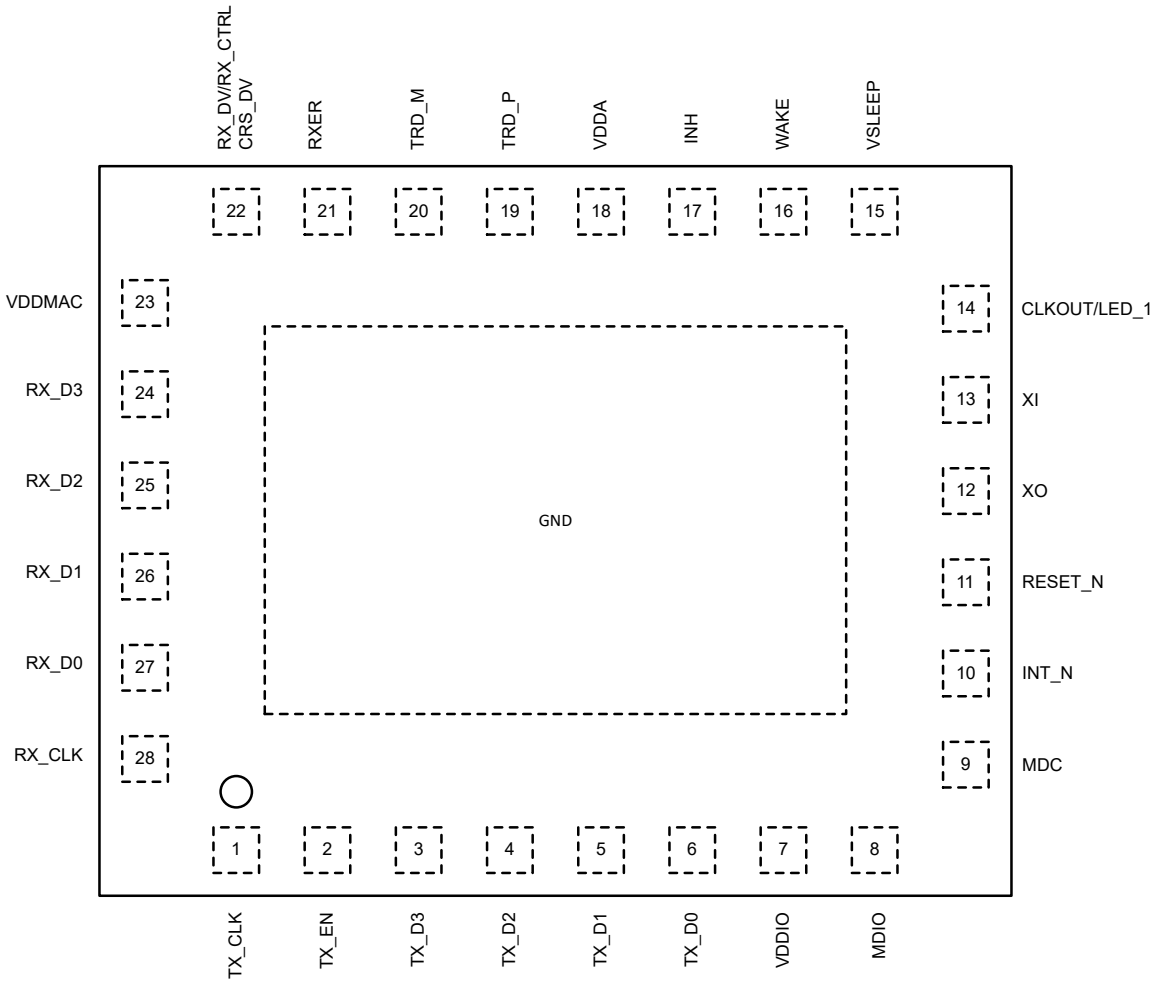

Figure 4-2. DP83TC813R-Q1 Pin Diagram

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Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TX_CLK	1	Valid data cannot be received.	B
TX_EN/TX_CTRL	2	Valid data cannot be received.	B
TX_D3	3	Valid data cannot be received.	B
TX_D2	4	Valid data cannot be received.	B
TX_D1/TX_P	5	Valid data cannot be received.	B
TX_D0/TX_M	6	Valid data cannot be received.	B
VDDIO	7	Invalid IO supply.	B
MDIO	8	No SMI communication available.	B
MDC	9	No SMI communication available.	B
INT	10	No valid interrupt status.	B
RESET	11	Device in Reset state.	B
XO	12	Crystal resonator clock will not start-up. Device PLL not operational. PHY state not known.	B
XI	13	Crystal resonator clock will not start-up. Device PLL not operational. PHY state not known.	B
CLKOUT/LED_1	14	GPIO not operational.	B
VSLEEP	15	Device is disabled. VSLEEP supply short.	B
WAKE	16	Device can enter into sleep state.	B
INH	17	Inhibit is not operational.	B
VDDA	18	Invalid core supply.	B
TRD_P	19	Link/data transfer cannot occur.	A
TRD_M	20	Link/data transfer cannot occur.	A
RX_ER	21	Valid data cannot be sent to MAC.	B
RX_DV/CRS_DV/ RX_CTRL	22	Valid data cannot be sent to MAC.	B
VDDMAC	23	Invalid VDDMAC supply.	B
RX_D3/RX_M	24	Valid data cannot be sent to MAC.	B
RX_D2/RX_P	25	Valid data cannot be sent to MAC.	B
RX_D1	26	Valid data cannot be sent to MAC.	B
RX_D0	27	Valid data cannot be sent to MAC	B
RX_CLK	28	Valid data cannot be sent to MAC.	B

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Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TX_CLK	1	Valid data cannot be received.	B
TX_EN/TX_CTRL	2	Valid data cannot be received.	B
TX_D3	3	Valid data cannot be received.	B
TX_D2	4	Valid data cannot be received.	B
TX_D1/TX_P	5	Valid data cannot be received.	B
TX_D0/TX_M	6	Valid data cannot be received.	B
VDDIO	7	Device is disabled. IO supply open.	B
MDIO	8	No SMI communication available.	B
MDC	9	No SMI communication available.	B
INT	10	Interrupt will not be available.	B
RESET	11	Normal operation.	D
XO	12	Crystal resonator clock will not start-up. Device PLL not operational. PHY state not known	B
XI	13	Crystal resonator clock will not start-up. Device PLL not operational. PHY state not known.	B
CLKOUT/LED_1	14	No issue.	D
VSLEEP	15	Device is disabled. V_{SLEEP} supply open	B
WAKE	16	No issue.	D
INH	17	Inhibit is not operational.	B
VDDA	18	Device is disabled. Core supply open.	B
TRD_P	19	Link/data transfer cannot occur	B
TRD_M	20	Link/data transfer cannot occur.	B
RX_ER	21	Valid data cannot be sent to MAC.	B
RX_DV/CRS_DV/ RX_CTRL	22	Valid data cannot be sent to MAC.	B
VDDMAC	23	Device is disabled. MAC supply open.	B
RX_D3/RX_M	24	Valid data cannot be sent to MAC.	B
RX_D2/RX_P	25	Valid data cannot be sent to MAC.	B
RX_D1	26	Valid data cannot be sent to MAC.	B
RX_D0	27	Valid data cannot be sent to MAC.	B
RX_CLK	28	Valid data cannot be sent to MAC.	B

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Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
TX_CLK	1	TX_EN/ TX_CTRL	Valid data cannot be received.	B
TX_EN/ TX_CTRL	2	TX_D3	Valid data cannot be received.	B
TX_D3	3	TX_D2	Valid data cannot be received.	B
TX_D2	4	TX_D1/TX_P	Valid data cannot be received.	B
TX_D1/TX_P	5	TX_D0/TX_M	Valid data cannot be received.	B
TX_D0/TX_M	6	VDDIO	If VDDIO equals VDDMAC, valid data cannot be received. If VDDIO does not equal VDDMAC, device can be damaged.	B A
VDDIO	7	MDIO	No SMI communication available.	B
MDIO	8	MDC	No SMI communication available.	B
MDC	9	INT	No SMI communication available; no valid interrupt status.	B
INT	10	RESET	When device intending to give interrupt it enters reset. Also, when host resets the PHY, host will get ISR triggered.	B
RESET	11	XO	Device will keep getting reset.	B
XO	12	XI	Device in unknown state.	B
XI	13	CLKOUT/ LED_1	Device in unknown state.	B
CLKOUT/ LED_1	14	VSLEEP	Device may get damaged.	A
VSLEEP	15	WAKE	Wake functionality is lost.	B
WAKE	16	INH	Inhibit is not operational as per its definition.	B
INH	17	VDDA	Inhibit is not operational.	B
VDDA	18	TRD_P	Link/data transfer cannot occur.	A
TRD_P	19	TRD_M	Link/data transfer cannot occur.	B
TRD_M	20	RX_ER	Link/data transfer cannot occur.	B
RX_ER	21	RX_DV/ CRS_DV/ RX_CTRL	Communication to MAC may be lost. Valid data will trigger an error. PHY Address range restricted. MDC/MDIO communication could be lost.	B
RX_DV/ CRS_DV/ RX_CTRL	22	VDDMAC	Valid data cannot be sent to MAC.	B
VDDMAC	23	RX_D3/RX_M	Valid data cannot be sent to MAC.	B
RX_D3/RX_M	24	RX_D2/RX_P	Valid data cannot be sent to MAC.	B
RX_D2/RX_P	25	RX_D1	MAC interface selection may be corrupt. Valid data cannot be sent to MAC.	B
RX_D1	26	RX_D0	MAC interface selection may be corrupt. Valid data cannot be sent to MAC.	B
RX_D0	27	RX_CLK	MAC interface selection may be corrupt. Valid data cannot be sent to MAC.	B
RX_CLK	28	TX_CLK	Valid data cannot be exchanged with MAC.	B

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Table 4-5. Pin FMA for Device Pins Short-Circuited to VDDIO

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TX_CLK	1	Device may get damaged when VDDIO and VDDMAC are of different voltage levels.	A
TX_EN/TX_CTRL	2	Device may get damaged when VDDIO and VDDMAC are of different voltage levels.	A
TX_D3	3	Device may get damaged when VDDIO and VDDMAC are of different voltage levels.	A
TX_D2	4	Device may get damaged when VDDIO and VDDMAC are of different voltage levels.	A
TX_D1/TX_P	5	Device may get damaged when VDDIO and VDDMAC are of different voltage levels.	A
TX_D0/TX_M	6	If VDDIO equals VDDMAC, valid data cannot be received. If VDDIO does not equal VDDMAC, device can be damaged.	B A
VDDIO	7	Appropriate connection.	D
MDIO	8	No SMI communication available.	B
MDC	9	No SMI communication available.	B
INT	10	No interrupt status.	B
RESET	11	Can never reset the device.	B
XO	12	PHY state not known.	B
XI	13	PHY state not known.	B
CLKOUT/LED_1	14	GPIO not operational.	B
VSLEEP	15	PHY may not power up.	B
WAKE	16	Device may not go into sleep state.	B
INH	17	Inhibit is not operational.	B
VDDA	18	Device may not power up.	B
TRD_P	19	Link/data transfer cannot occur. Device may get damaged.	A
TRD_M	20	Link/data transfer cannot occur. Device may get damaged.	A
RX_ER	21	PHY Address range restricted. MDC/MDIO communication could be lost. Device may get damaged when VDDIO and VDDMAC are different.	B A
RX_DV/CRS_DV/ RX_CTRL	22	PHY Address range restricted. MDC/MDIO communication could be lost. Device may get damaged when VDDIO and VDDMAC are different.	B A
VDDMAC	23	No issue	D
RX_D3/RX_M	24	Device may get damaged when VDDIO and VDDMAC are of different voltage levels.	A
RX_D2/RX_P	25	Device may get damaged when VDDIO and VDDMAC are of different voltage levels.	A
RX_D1	26	Device may get damaged when VDDIO and VDDMAC are of different voltage levels.	A
RX_D0	27	Device may get damaged when VDDIO and VDDMAC are of different voltage levels.	A
RX_CLK	28	Device may get damaged when VDDIO and VDDMAC are of different voltage levels.	A

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Table 4-6. Pin FMA for Device Pins Short-Circuited to VDDMAC

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TX_CLK	1	Valid data cannot be received from MAC.	B
TX_EN/TX_CTRL	2	Valid data cannot be received from MAC.	B
TX_D3	3	Valid data cannot be received from MAC.	B
TX_D2	4	Valid data cannot be received from MAC.	B
TX_D1/TX_P	5	Valid data cannot be received from MAC	B
TX_D0/TX_M	6	Valid data cannot be received from MAC.	B
VDDIO	7	Device will be functional.	D
MDIO	8	No SMI communication available. Device may get damaged when VDDIO and VDDMAC are of different voltage levels.	A
MDC	9	Device may get damaged when VDDIO and VDDMAC are of different voltage levels.	A
INT	10	Device may get damaged when VDDIO and VDDMAC are of different voltage levels.	A
RESET	11	Device may get damaged when VDDIO and VDDMAC are of different voltage levels.	A
XO	12	PHY state not known.	B
XI	13	PHY state not known.	B
CLKOUT/LED_1	14	GPIO not operational. Device may get damaged when VDDIO and VDDMAC are of different voltage levels.	A
VSLEEP	15	PHY may not powerup.	B
WAKE	16	Device may not go into sleep state.	B
INH	17	Inhibit is not operational.	B
VDDA	18	Device may not power up.	B
TRD_P	19	Link/data transfer cannot occur. Device may get damaged.	A
TRD_M	20	Link/data transfer cannot occur. Device may get damaged.	A
RX_ER	21	PHY Address range restricted. MDC/MDIO communication could be lost. Invalid data triggered to the MAC.	B
RX_DV/CRS_DV/ RX_CTRL	22	PHY Address range restricted. MDC/MDIO communication could be lost. Invalid data triggered to the MAC.	B
VDDMAC	23	No issue.	D
RX_D3/RX_M	24	Valid data cannot be sent to MAC.	B
RX_D2/RX_P	25	Valid data cannot be sent to MAC.	B
RX_D1	26	Valid data cannot be sent to MAC.	B
RX_D0	27	Valid data cannot be sent to MAC.	B
RX_CLK	28	Valid data cannot be sent to MAC.	B

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Table 4-7. Pin FMA for Device Pins Short-Circuited to VDDA

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TX_CLK	1	Device may get damaged.	A
TX_EN/TX_CTRL	2	Device may get damaged.	A
TX_D3	3	Device may get damaged.	A
TX_D2	4	Device may get damaged.	A
TX_D1/TX_P	5	Device may get damaged.	A
TX_D0/TX_M	6	Device may get damaged.	A
VDDIO	7	Device will be functional.	D
MDIO	8	No SMI communication available. Device may get damaged.	A
MDC	9	Device may get damaged.	A
INT	10	Device may get damaged.	A
RESET	11	Device may get damaged.	A
XO	12	PHY state not known.	B
XI	13	PHY state not known.	B
CLKOUT/LED_1	14	Device may get damaged.	A
VSLEEP	15	Device will be functional.	D
WAKE	16	Device may not go into sleep state.	B
INH	17	Inhibit is not operational.	B
VDDA	18	Appropriate connection.	D
TRD_P	19	Link/data transfer cannot occur. Device may get damaged.	A
TRD_M	20	Link/data transfer cannot occur. Device may get damaged.	A
RX_ER	21	Device may get damaged.	A
RX_DV/CRS_DV/ RX_CTRL	22	Device may get damaged.	A
VDDMAC	23	Device will be functional.	D
RX_D3/RX_M	24	Device may get damaged.	A
RX_D2/RX_P	25	Device may get damaged.	A
RX_D1	26	Device may get damaged.	A
RX_D0	27	Device may get damaged.	A
RX_CLK	28	Device may get damaged.	A

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Table 4-8. Pin FMA for Device Pins Short-Circuited to VSLEEP

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TX_CLK	1	Device may get damaged.	A
TX_EN/TX_CTRL	2	Device may get damaged.	A
TX_D3	3	Device may get damaged.	A
TX_D2	4	Device may get damaged.	A
TX_D1/TX_P	5	Device may get damaged.	A
TX_D0/TX_M	6	Device may get damaged.	A
VDDIO	7	Device will be functional.	D
MDIO	8	No SMI communication available. Device may get damaged.	A
MDC	9	Device may get damaged.	A
INT	10	Device may get damaged.	A
RESET	11	Device may get damaged.	A
XO	12	PHY state not known.	B
XI	13	PHY state not known.	B
CLKOUT/LED_1	14	Device may get damaged.	A
VSLEEP	15	Appropriate connection.	D
WAKE	16	Device may not go into sleep state.	B
INH	17	Inhibit is not operational.	B
VDDA	18	Device will be functional.	D
TRD_P	19	Link/data transfer cannot occur. Device may get damaged.	A
TRD_M	20	Link/data transfer cannot occur. Device may get damaged.	A
RX_ER	21	Device may get damaged.	A
RX_DV/CRS_DV/ RX_CTRL	22	Device may get damaged.	A
VDDMAC	23	Device will be functional.	D
RX_D3/RX_M	24	Device may get damaged.	A
RX_D2/RX_P	25	Device may get damaged.	A
RX_D1	26	Device may get damaged	A
RX_D0	27	Device may get damaged.	A
RX_CLK	28	Device may get damaged.	A

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5 Revision History

Changes from Revision A (December 2022) to Revision B (July 2023)	Page
• Added secondary description for VDDIO not equal to VDDMAC for pin 6 short circuit to adjacent pin, and pins 6, 21, 22 short circuit to VDDIO	5

Changes from Revision * (December 2022) to Revision A (April 2023)	Page
• Added "-Q1" designation to device throughout document	2
• Corrected description for CLKOUT/LED_1 pin when shorted to VDDIO. Clarified descriptions for potential failure effects when pins when shorted to GND	5

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