Functional Safety Information

TPS4H000-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for TPS4H000-Q1 (HTSSOP package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

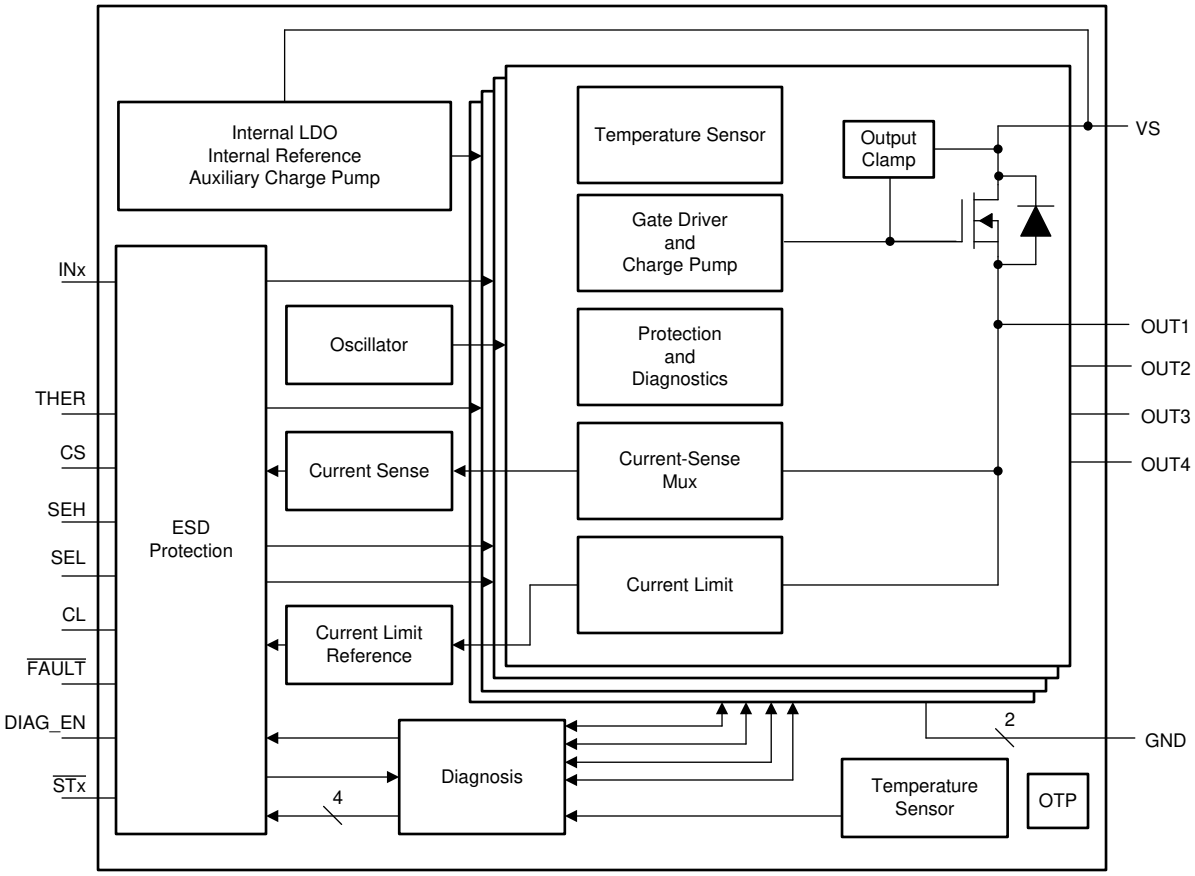

Figure 1-1. Functional Block Diagram

TPS4H000-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TPS4H000-Q1 based on an industry-wide used reliability standard:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	17
Die FIT Rate	5
Package FIT Rate	12

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 500 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS4H000-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUT1,2,3,4 open (HiZ)	20%
OUT1,2,3,4 stuck on (VS)	10%
OUT1,2,3,4 not in specification voltage or timing	45%
Diagnostics not in specification	10%
Protection functions fails to trip	10%
Pin to pin short any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS4H000-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VS (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TPS4H000-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS4H000-Q1 data sheet.

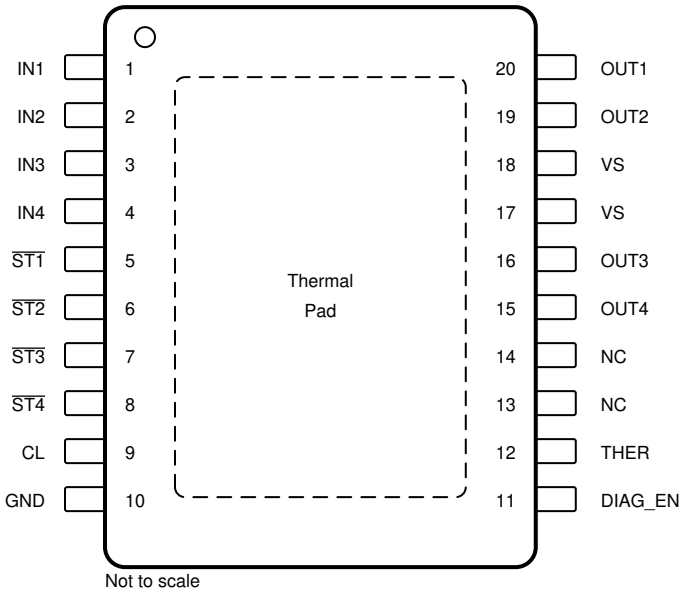

Figure 4-1. Pin Diagram (Version A)

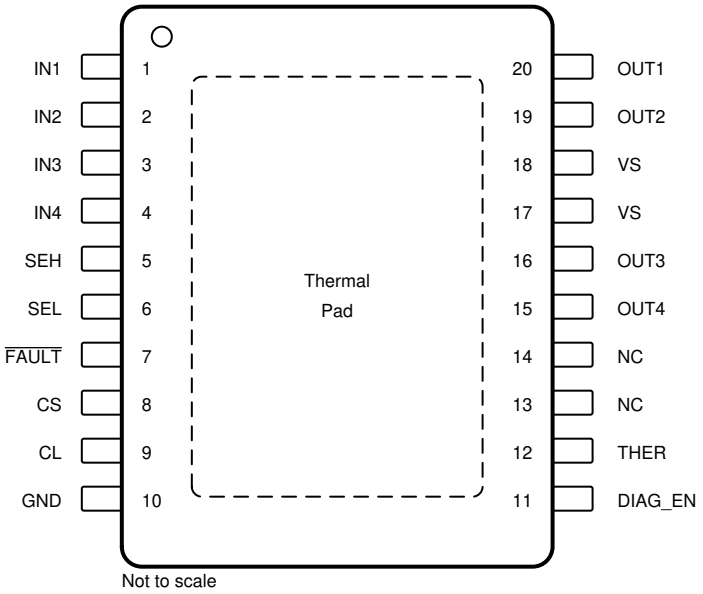

Figure 4-2. Pin Diagram (Version B)

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Follows data sheet recommendation for operating conditions, external components selection, and PCB layout

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
INx	1, 2, 3, 4	Shutdown of corresponding channel.	B
$\overline{\text{STx}}$	5, 6, 7, 8	Version A only. Status being reported erroneous.	B
SEH	5	Version B only. If DIAG_EN is high then only channel 3 or 4's (depending on SEL) sense current output on SNS pin.	B
SEL	6	Version B only. If DIAG_EN is high then only channel 1 or 2's (depending on SEH) sense current output on SNS pin.	B
$\overline{\text{FAULT}}$	7	Version B only. Status being reported erroneous.	B
CS	8	Version B only. Sense current not valid from CS pin.	B
CL	9	Device defaults to internal current limit.	C
GND	10	Resistor/diode network bypassed if present.	B
DIAG_EN	11	Diagnostics disabled.	B
THER	12	Device defaults to "auto-retry" mode when encountering thermal fault.	B
NC	13, 14	No effect.	D
OUTx	15, 16, 19, 20	Current limit of device engages.	B
VS	17, 18	Device has no input supply and therefore not function.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
INx	1, 2, 3, 4	Corresponding channel shutdown and INx pulled down internally.	B
$\overline{\text{STx}}$	5, 6, 7, 8	Version A only. $\overline{\text{STx}}$ pin cannot pull high and diagnostics cannot be reported.	B
SEH	5	Version B only. Pulled low internally, however wrong SNS current potentially reported on CS if DIAG_EN is high.	B
SEL	6	Version B only. If DIAG_EN is high then only channel 1 or 2's (depending on SEH) sense current output on SNS pin.	B
$\overline{\text{FAULT}}$	7	Version B only. Fault signal not reported.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
CS	8	Version B only. Correct sense current cannot be read.	B
CL	9	Device defaults to internal current limit.	C
GND	10	Loss of ground detection engages and device shuts off.	B
DIAG_EN	11	Internally pulled down. Diagnostics disabled.	B
THER	12	Internally pulled down. Device defaults to "auto-retry" mode when encountering thermal fault.	B
NC	13, 14	No effect.	D
OUTx	15, 16, 19, 20	No effect. If configured, open load detection triggers.	B
VS	17, 18	Device has no input supply and therefore not function.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
IN1	1	IN2	IN1 signal affects IN2 signal and vice versa.	B
IN2	2	IN3	IN2 signal affects IN3 signal and vice versa.	B
IN3	3	IN4	IN3 signal affects IN4 signal and vice versa.	B
IN4	4	ST1	Version A only. If ST1 is high then channel 4 is on.	B
IN4	4	SEH	Version B only. IN4 signal affects SEH and vice versa.	B
$\overline{\text{ST1}}$	5	$\overline{\text{ST2}}$	Version A only. Fault reporting of channel 1 and channel 2 erroneous.	B
SEH	5	SEL	Version B only. SEH signal affects SEL and vice versa. If DIAG_EN is high only channel 1 or 4 can be read at SNS.	B
$\overline{\text{ST2}}$	6	$\overline{\text{ST3}}$	Version A only. Fault reporting of channel 2 and channel 3 erroneous.	B
SEL	6	$\overline{\text{FAULT}}$	Version B only. If $\overline{\text{FAULT}}$ high and DIAG_EN high, only channel 2 or channel 4 can be read at SNS.	B
$\overline{\text{ST3}}$	7	$\overline{\text{ST4}}$	Version A only. Fault reporting of channel 3 and channel 4 erroneous.	B
$\overline{\text{FAULT}}$	7	CS	Version B only. Fault reporting and current sense reporting erroneous.	B
$\overline{\text{ST4}}$	8	CL	Version A only. $\overline{\text{ST4}}$ voltage can cause erroneous current limit to be set on device.	B
CS	8	CL	Version B only. Voltage level on CS can cause erroneous current limit to be set on device.	B
CL	9	GND	Device defaults to internal current limit.	C
DIAG_EN	11	THER	DIAG_EN signal affects THER signal and vice versa.	B
THER	12	NC	No effect	D
NC	14	OUT4	No effect.	D
OUT4	15	OUT3	Output of channel 4 tied to output of channel 3.	B
OUT3	16	VS	Channel 3 cannot be turned off. Short-to-battery detection triggered if configured.	B
VS	17	VS	No effect.	D
VS	18	OUT2	Channel 2 cannot be turned off. Short-to-battery detection triggered if configured.	B
OUT2	19	OUT1	Output of channel 2 tied to output of channel 1.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply (VBB)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
INx	1, 2, 3, 4	Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell.	A
$\overline{\text{STx}}$	5, 6, 7, 8	Version A only. Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply (VBB) (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SEH	5	Version B only. Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell	A
SEL	6	Version B only. Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell.	A
$\overline{\text{FAULT}}$	7	Version B only. Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell.	A
CS	8	Version B only. Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell.	A
CL	9	Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell.	A
GND	10	Supply power bypassed and device does not turn on.	B
DIAG_EN	11	Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell.	A
THER	12	Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell.	A
NC	13, 14	No effect.	D
OUTx	15, 16, 19, 20	Output pulled to supply voltage. Short-to-battery detection triggered if configured.	B
VS	17, 18	No effect.	A

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265