Functional Safety Information

TPS281C30x
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for TPS281C30x (RGW (QFN, 20) package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

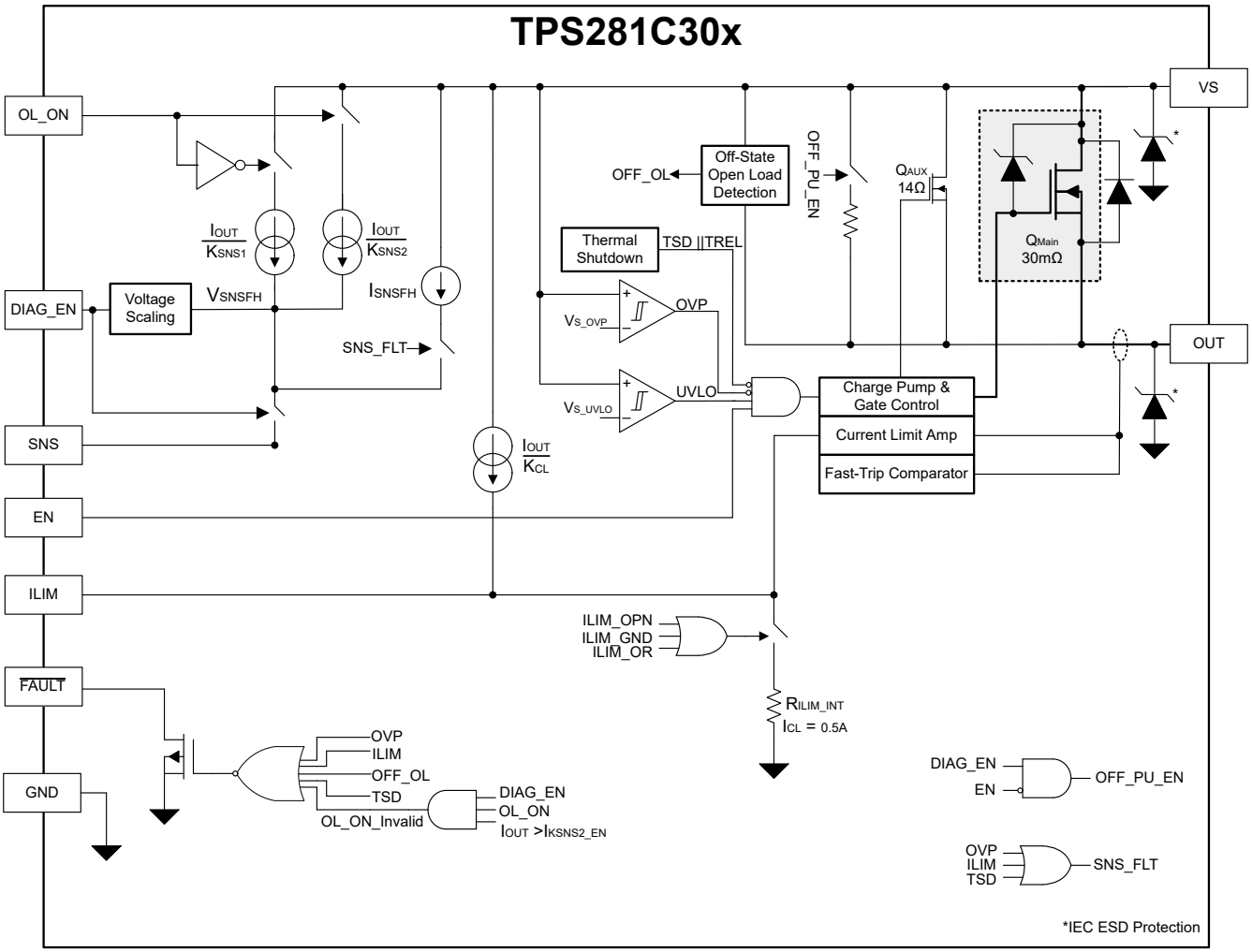

Figure 1-1. Functional Block Diagram

The TPS281C30x was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for TPS281C30x based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	21
Die FIT rate	5
Package FIT rate	16

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 750mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS281C30x in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT open (Hi-Z)	20
VOUT stuck ON to VS	10
VOUT functional – not in specification voltage or timing	50
Diagnostics not in specification	10
Protection function fails to trip	10

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS281C30x. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VS supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TPS281C30x pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS281C30x data sheet.

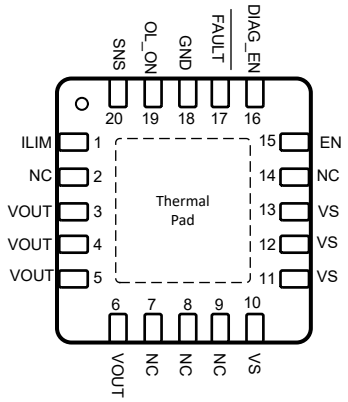

Figure 4-1. Pin Diagram for RGW (QFN, 20)

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device pins are connected per the recommendation in the data sheet, including pullup and pulldown resistors, as needed.
- The data sheet recommendations for operating conditions, external component selection, and PCB layout are followed.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
ILIM	1	The current limit is set at a low level, as per the data sheet.	C
NC	2	No effect.	D
	7		
	8		
	9		
	14		

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VOUT	3	The current limit of the device engages, and thermal protection turns off the FET.	B
	4		
	5		
	6		
VS	10	The output stages are not powered, and the FET does not turn ON.	B
	11		
	12		
	13		
EN	15	The main FET is turned off.	B
DIAG_EN	16	Diagnostics features do not function, including current sense and fault reporting.	B
$\overline{\text{FAULT}}$	17	The reported fault status is potentially erroneous.	B
GND	18	Any GND network, connected for protection, is bypassed.	B
OL_ON	19	High-accuracy current sense is not available.	B
SNS	20	The reported SNS current or fault status on the SNS pin is erroneous.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
ILIM	1	The current limit is set at a low level, as per the data sheet.	C
NC	2	No effect.	D
	7		
	8		
	9		
	14		
VOUT	3	During the ON state of the device, if any one pin is open, the switch resistance increases. During the OFF state of the device, if the DIAG_EN pin is high, an open-load fault reports.	B
	4		
	5		
	6		
VS	10	During the ON state of the device, if any one pin is open, the switch resistance increases. If all pins are open, the device is not powered and the switch is kept OFF.	B
	11		
	12		
	13		
EN	15	The main FET is turned off.	B
DIAG_EN	16	Diagnostics features do not function, including ON state current sense, OFF state open-load, and short-to-battery.	B
$\overline{\text{FAULT}}$	17	The fault condition is not reported.	B
GND	18	The loss of ground detection engages, and the device turns OFF.	B
OL_ON	19	High-accuracy current sense is not available.	B
SNS	20	The current sense voltage of the pin is clamped internally and no current sense information is available.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
ILIM	1	NC	No effect.	D
NC	2	VOUT	No effect.	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
VOUT	3	N/A	Not plausible (corner pin).	D
	4			
	5			
VOUT	6	NC	No effect.	D
NC	7	VS	No effect.	D
	8			
	9			
VS	10	N/A	Not plausible (corner pin).	D
VS	11	NC	No effect.	D
	12			
	13			
NC	14	EN	No effect.	D
EN	15	N/A	Not plausible (corner pin).	D
DIAG_EN	16	$\overline{\text{FAULT}}$	Fault reporting is erroneous. Diagnostics are enabled if the $\overline{\text{FAULT}}$ pin is pulled high.	B
$\overline{\text{FAULT}}$	17	GND	The reported fault status is potentially erroneous.	B
GND	18	OL_ON	High-accuracy current sense is not available.	B
OL_ON	19	SNS	The current sensing output is potentially erroneous, and effects the high-accuracy current sense.	B
SNS	20	N/A	Not plausible (corner pin).	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to VS Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
ILIM	1	There is a potential violation of the absolute maximum rating for the pin and a possible breakdown of the ESD cell.	A
NC	2	No effect.	D
	7		
	8		
	9		
	14		
VOUT	3	The output is pulled to supply voltage. A short-to-battery detection triggers during the OFF state if the DIAG_EN pin is high.	B
	4		
	5		
	6		
VS	10	No effect.	D
	11		
	12		
	13		
EN	15	There is a potential violation of the absolute maximum rating for the pin and a possible breakdown of the ESD cell.	A
DIAG_EN	16	There is a potential violation of the absolute maximum rating for the pin and a possible breakdown of the ESD cell.	A
$\overline{\text{FAULT}}$	17	There is a potential violation of the absolute maximum rating for the pin and a possible breakdown of the ESD cell.	A
GND	18	The supply power is bypassed, and the device stays OFF.	B
OL_ON	19	There is a potential violation of the absolute maximum rating for the pin and a possible breakdown of the ESD cell.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to VS Supply (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SNS	20	There is a potential violation of the absolute maximum rating for the pin and a possible breakdown of the ESD cell.	A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2025	*	Initial Release

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