Functional Safety Information

LM393LV-Q1 and LM339LV-Q1 Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for the LM393LV-Q1 and LM339LV-Q1 (dual and quad channels) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

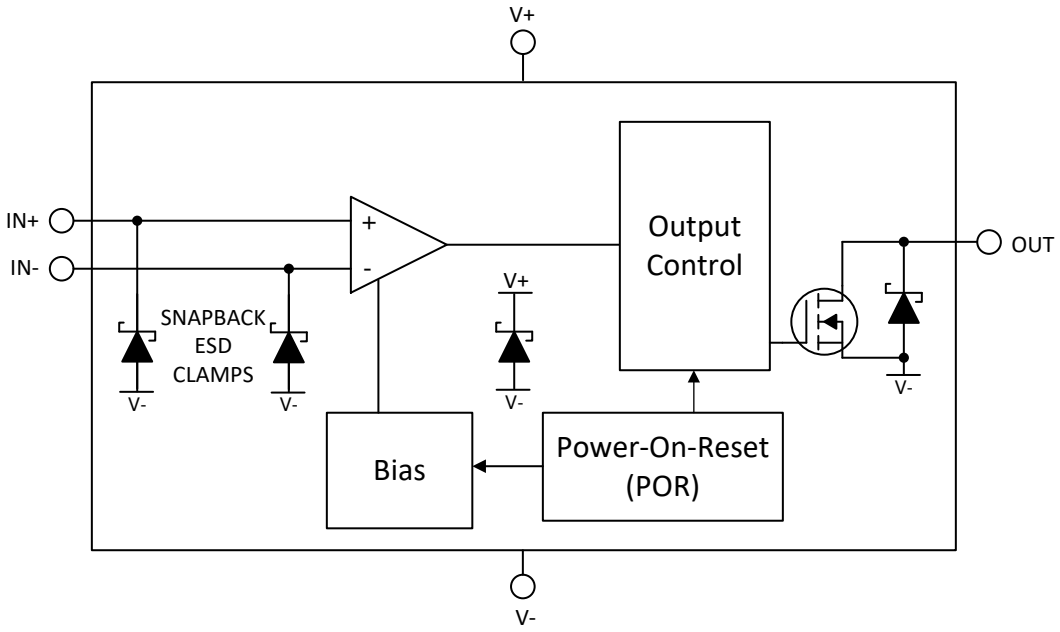

Figure 1-1. Functional Block Diagram (Open-Drain and Push-Pull)

The LM393LV-Q1 and LM339LV-Q1 were developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 Dual Packages

This section provides functional safety failure in time (FIT) rates for the packages of the LM393LV-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)				
Package	SOIC-8	TSSOP-8	VSSOP-8	WSON-8	SOT23-8
Total component FIT rate	9	8	6	4	4
Die FIT rate	2	2	2	2	2
Package FIT rate	7	6	4	2	2

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 250 µW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	CMOS, BICMOS Digital, analog, or mixed	12FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 Quad Packages

This section provides functional safety failure in time (FIT) rates for the packages of the LM339LV-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)			
Package	SOIC-14	TSSOP-14	SOT23-14	WQFN-16
Total component FIT rate	16	10	6	8
Die FIT rate	2	2	2	2
Package FIT rate	14	8	4	6

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 500 µW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	CMOS, BICMOS Digital, analog, or mixed	12 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the LM393LV-Q1 and LM339LV-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Out open (HIZ)	30
Out saturate low	30
Out functional (not in specification)	35
Short circuit any two pins	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the LM339LV-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1 .

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the LM339LV-Q1 pin diagram. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the data sheet.

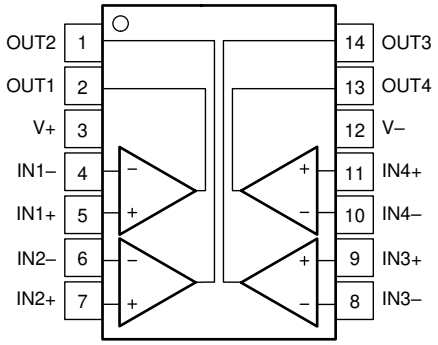

Figure 4-1. Pin Diagram

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT2	1	No change if GND pin is GND node	B
OUT1	2	No change if GND pin is GND node	B
V+	3	Main supply shorted out (no power to device)	B
IN1-	4	Output goes high, if other input is positive	B
IN1+	5	Output goes low, if other input is positive	B
IN2-	6	Output goes high, if other input is positive	B
IN2+	7	Output goes low, if other input is positive	B
IN3-	8	Output goes high, if other input is positive	B
IN3+	9	Output goes low, if other input is positive	B
IN4-	10	Output goes high, if other input is positive	B
IN4+	11	Output goes low, if other input is positive	B
V-	12	No change if same node as GND	D
OUT4	13	No change if GND pin is GND node	B
OUT3	14	No change if GND pin is GND node	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT2	1	Output can't drive application load	B
OUT1	2	Output can't drive application load	B
V+	3	Main supply open (no power to device)	B
IN1-	4	Output can be low or high	B
IN1+	5	Output can be low or high	B
IN1-	6	Output can be low or high	B
IN2+	7	Output can be low or high	B
IN3-	8	Output can be low or high	B
IN3+	9	Output can be low or high	B
IN4-	10	Output can be low or high	B
IN4+	11	Output can be low or high	B
V-	12	Lowest voltage pin drives GND pin internally (via diode)	A
OUT4	13	Output can't drive application load	B
OUT3	14	Output can't drive application load	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
UT2	1	OUT1	Output can be low or high	B
OUT1	2	V+	Thermal stress due to high power dissipation	A
V+	3	IN1-	Output goes low, if other input is less positive	B
IN1-	4	IN1+	Output can be low or high	B
IN1+	5	IN2-	Output can be low or high	B
IN2-	6	IN2+	Output can be low or high	B
IN2+	7	IN3-	Output can be low or high	B
IN3-	8	IN3+	Output can be low or high	B
IN3+	9	IN4-	Output can be low or high	B
IN4-	10	IN4+	Output can be low or high	B
IN4+	11	V-	Output goes low, if other input is positive	B
V-	12	OUT4	No change if GND pin is GND node	B
OUT4	13	OUT3	Output can be low or high	B
OUT3	14	OUT2	Output can be low or high	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT2	1	Thermal stress due to high power dissipation	A
OUT1	2	Thermal stress due to high power dissipation	A
V+	3	No change if same node as VCC	D
IN1-	4	Output goes low, if other input is less positive	B
IN1+	5	Output goes high, if other input is less positive	B
IN2-	6	Output goes low, if other input is less positive	B
IN2+	7	Output goes high, if other input is less positive	B
IN3-	8	Output goes low, if other input is less positive	B
IN3+	9	Output goes high, if other input is less positive	B
IN4-	10	Output goes low, if other input is less positive	B
IN4+	11	Output goes high, if other input is less positive	B
V-	12	Main supply shorted out (no power to device)	B
OUT4	13	Thermal stress due to high power dissipation	A
OUT3	14	Thermal stress due to high power dissipation	A

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