Functional Safety Information

AMC1035-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for the AMC1035-Q1 (SOIC package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards

Figure 1-1 shows the device functional block diagram for reference.

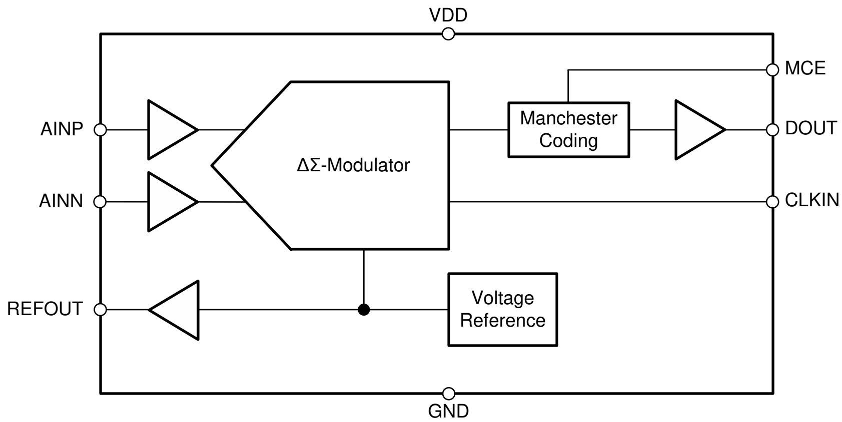


Figure 1-1. Functional Block Diagram

The AMC1035-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the AMC1035-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	9
Die FIT rate	7
Package FIT rate	2

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: motor control from table 11
- Power dissipation: 46 mW
- Climate type: world-wide table 8
- Package factor (lambda 3): table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the AMC1035-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
DOUT stuck high or low	30%
Bitstream output out of specification (equivalent to gain error)	20%
Device behavior undetermined	20%
Bitstream output out of specification (equivalent to offset error)	15%
Reference output out of specification[(1)]	10%
Bitstream output out of specification (increased noise)	5%

(1) This failure mode also causes gain error failures.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the AMC1035-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

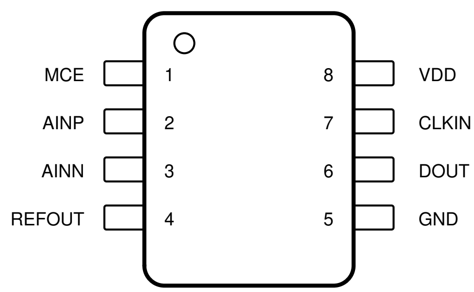
- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the AMC1035-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the AMC1035-Q1 data sheet.



Not to scale

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Analog inputs are connected to a resistive signal source.
- Differential RC filter on AINP or AINN.
  Series resistors are sized to limit the input currents into AINP and AINN to <10 mA in all circumstances (for example, if the device is unpowered and the input signal is applied).
- CLKIN is driven with CMOS-compliant signal levels.
- DOUT load is only capacitive (no DC connection to DGND or DVDD).
- Manchester encoding is disabled (MCE pin connected to GND).
- REFOUT is not used (left floating).

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
MCE	1	Manchester encoding disabled. Normal operation for the assumed use case.	D
AINP	2	AINP stuck low (GND). Value of DOUT output bitstream proportional to voltage difference (V_{GND} – V_{AINN}).	B
AINN	3	AINN stuck low (GND). Value of DOUT output bitstream proportional to voltage difference V_{AINP} – V_{AGND} .	B
REFOUT	4	Excess current consumption from VDD source. DOUT bitstream not affected. Long-term damage plausible.	A
GND	5	No effect. Normal operation.	D
DOUT	6	DOUT stuck low (GND). No valid DOUT output bitstream. Excess current consumption from VDD source when DOUT tries to drive high. Long-term damage plausible.	A
CLKIN	7	CLKIN stuck low (GND). Device not functional due to missing clock input. DOUT stuck in the state (high or low) that it was when CLKIN stopped. No valid DOUT output bitstream.	B
VDD	8	Device is unpowered. DOUT pin is driven to GND. No valid DOUT output bitstream. Observe that the absolute maximum ratings for CLKIN of the device are met, otherwise device damage is plausible.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
MCE	1	Manchester encoding disabled (internal pulldown). Normal operation for the assumed use case.	D
AINP	2	Value of DOUT output bitstream undetermined.	B
AINN	3	Value of DOUT output bitstream undetermined.	B
REFOUT	4	No effect. Normal operation for the assumed use case.	D
GND	5	Device is periodically powered through ESD diode of the CLKIN pin when CLKIN is driven low. If the CLK driver can supply 8.3 mA of current then the device may function and produce a DOUT output bitstream. However the logic high and low levels of DOUT are not met. Otherwise the DOUT output bitstream is undetermined.	B
DOUT	6	DOUT undetermined. No valid DOUT output bitstream.	B
CLKIN	7	CLKIN floating. Device not functional due to missing clock input. DOUT stuck in the state (high or low) that it was when CLKIN stopped. No valid DOUT output bitstream.	B
VDD	8	Device secondary side periodically powered through ESD diode of the CLKIN pin when CLKIN is driven high. If the CLK driver can supply 8.3 mA of current then the device may function and produce a DOUT output bitstream. However the logic high and low levels of DOUT are not met. Otherwise the DOUT output bitstream is undetermined.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
MCE	1	AINP	Encoding scheme undetermined.	B
AINP	2	AINN	AINP shorted to AINN resulting in zero differential input voltage. Value of DOUT output bitstream at mid-scale (50% zeros, 50% ones).	B
AINN	3	REFOUT	AINN stuck at V_{REFOUT} (2.5 V). Value of DOUT output bitstream proportional to voltage difference ($V_{AINP} – V_{REFOUT}$).	B
REFOUT	4	GND	Not considered. Corner pin.	D
GND	5	DOUT	DOUT stuck low (GND). No valid DOUT output bitstream. Excess current consumption from VDD source when DOUT tries to drive high. Long-term damage plausible.	A
DOUT	6	CLKIN	DOUT output bit stream corrupted. Excess current consumption from VDD source when DOUT tries to drive high, while CLKIN drives low and vice versa. Long-term damage plausible.	A
CLKIN	7	VDD	CLKIN stuck high (VDD). Device not functional due to missing clock input. DOUT stuck in the state (high or low) that it was when CLKIN stopped. No valid DOUT output bitstream.	B
VDD	8	MCE	Not considered. Corner pin.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
MCE	1	Manchester encoding enabled. Incorrect coding for the assumed use case.	B
AINP	2	AINP stuck high (VDD). Value of DOUT output bitstream proportional to voltage difference (V_{VDD} – V_{AINN}). Overrange or common-mode overvoltage detection is likely to trigger (see data sheet for more details).	B
AINN	3	AINN stuck high (VDD). Value of DOUT output bitstream proportional to voltage difference (V_{AINP} – V_{VDD}). Overrange or common-mode overvoltage detection is likely to trigger (see data sheet for more details).	B
REFOUT	4	Excess current consumption from VDD source. DOUT bitstream not affected. Long-term damage plausible.	A
GND	5	Device is unpowered. DOUT pin is driven to GND. No valid DOUT output bitstream. Observe that the absolute maximum ratings for CLKIN of the device are met, otherwise device damage is plausible.	A
DOUT	6	DOUT stuck high (DVDD). No valid DOUT output bitstream. DOUT output bitstream looks like fail-safe output response if MCE = 0 (see data sheet for details). Excess current consumption from DVDD source when DOUT tries to drive low. Long-term damage plausible.	A
CLKIN	7	CLKIN stuck high (DVDD). Device not functional due to missing clock input. DOUT stuck in the state (high or low) that it was when CLKIN stopped. No valid DOUT output bitstream.	B
VDD	8	No effect. Normal operation.	D