Functional Safety Information

DRV5056-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the DRV5056-Q1 (SOT-23 and TO-92 packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

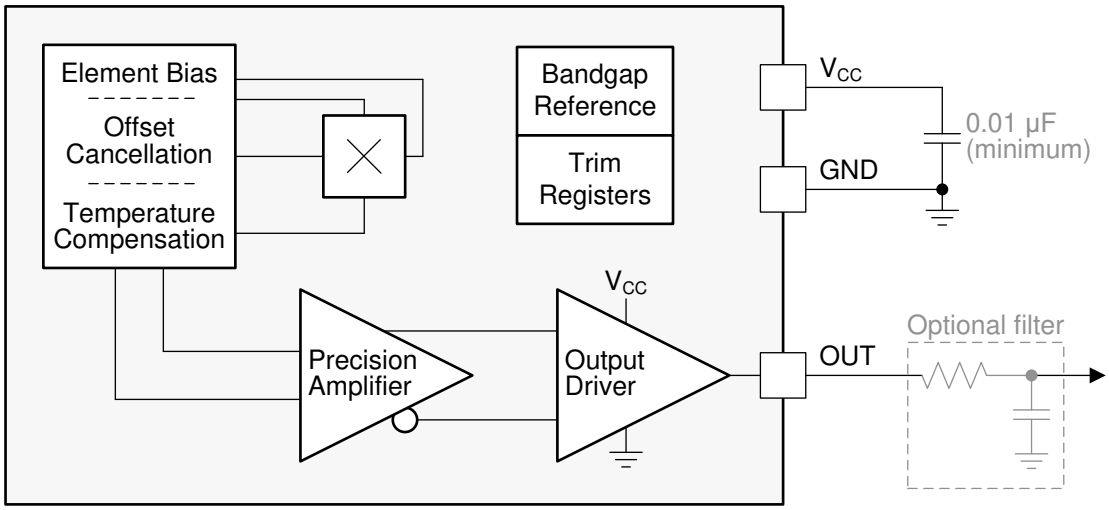

Figure 1-1. Functional Block Diagram

The DRV5056-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 SOT-23 Package

This section provides functional safety failure in time (FIT) rates for the SOT-23 package of the DRV5056-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	5
Die FIT rate	3
Package FIT rate	2

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 55 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 TO-92 Package

This section provides functional safety failure in time (FIT) rates for the TO-92 package of the DRV5056-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	19
Die FIT rate	3
Package FIT rate	16

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 55 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the DRV5056-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Incorrect channel selected	15
Channel-channel short	10
ADC output code bit error	15
ADC gain out of specification	20
ADC offset out of specification	20
Communication error	20

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the DRV5056-Q1 (SOT-23 and TO-92 packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2 and Table 4-5.)
- Pin open-circuited (see Table 4-3 and Table 4-6)
- Pin short-circuited to supply (see Table 4-4 and Table 4-7)

Table 4-2 through Table 4-7 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- External pullup resistor on $\overline{CS}$ to VDD
- RC filter on every analog input, AINx.

  Series resistors are sized to limit the input currents into the analog inputs to <10 mA in all circumstances (for example, in case the device is unpowered and the input signal is applied).
- The device is the only slave on the SPI bus.

4.1 SOT-23 Package

Figure 4-1 shows the DRV5056-Q1 pin diagram for the SOT-23 package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the DRV5056-Q1 data sheet.

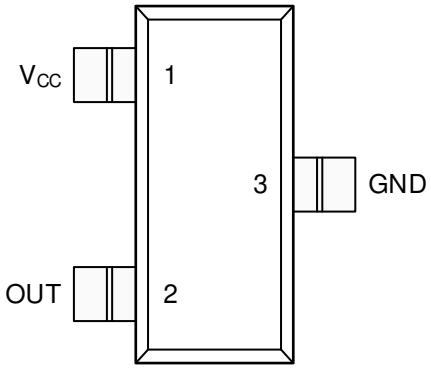

Figure 4-1. Pin Diagram (SOT-23) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
V_{CC}	1	Supply shorted to Ground. System will source high current as a result and may current limit. Thermal damage may result.	B
OUT	2	DRV5056-Q1 will not be damaged. Output will be pulled down by short to GND.	C
GND	3	Normal Mode of operation	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
V_{CC}	1	DRV5056-Q1 will not be damaged. There will be no power supply current and therefore no functionality.	B
OUT	2	DRV5056-Q1 will not be damaged. Supply current will be normal, but the output is not driving any load.	C
GND	3	DRV5056-Q1 will not be damaged. There will be no power supply current and therefore no functionality.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
V_{CC}	1	Normal mode of operation	D
OUT	2	DRV5056-Q1 will not be damaged. The output will sink about 14 mA (limited by overcurrent protection feature). The output signal will be pulled to VCC. Any MCU monitoring the output would observe VCC as an input which may result in over voltage.	B
GND	3	Supply shorted to Ground. System will source high current as a result and may current limit. Thermal damage may result.	B

4.2 TO-92 Package

Figure 4-2 shows the DRV5056-Q1 pin diagram for the TO-92 package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the DRV5056-Q1 data sheet.

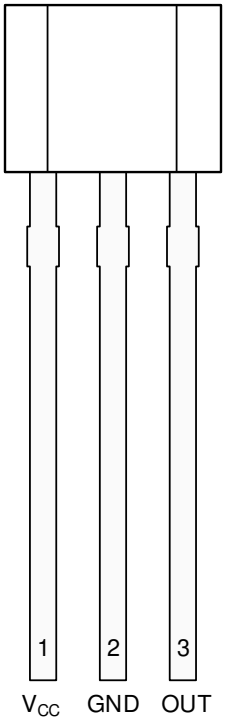

Figure 4-2. Pin Diagram (TO-92 Package)

Table 4-5. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
V_{CC}	1	Supply shorted to Ground. System will source high current as a result and may current limit. Thermal damage may result. B	B
GND	2	Normal Mode of operation	D
OUT	3	DRV5056-Q1 will not be damaged. Output will be pulled down by short to GND.	C

Table 4-6. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
V_{CC}	1	DRV5056-Q1 will not be damaged. There will be no power supply current and therefore no functionality.	B
GND	2	DRV5056-Q1 will not be damaged. There will be no power supply current and therefore no functionality.	B
OUT	3	DRV5056-Q1 will not be damaged. Supply current will be normal, but the output is not driving any load.	C

Table 4-7. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
V_{CC}	1	Normal mode of operation	D
GND	2	Supply shorted to Ground. System will source high current as a result and may current limit. Thermal damage may result.	B
OUT	3	DRV5056-Q1 will not be damaged. The output will sink about 14 mA (limited by overcurrent protection feature). The output signal will be pulled to VCC. Any MCU monitoring the output would observe VCC as an input which may result in over voltage.	B

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