Functional Safety Information

LM74912-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for LM74912-Q1 to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

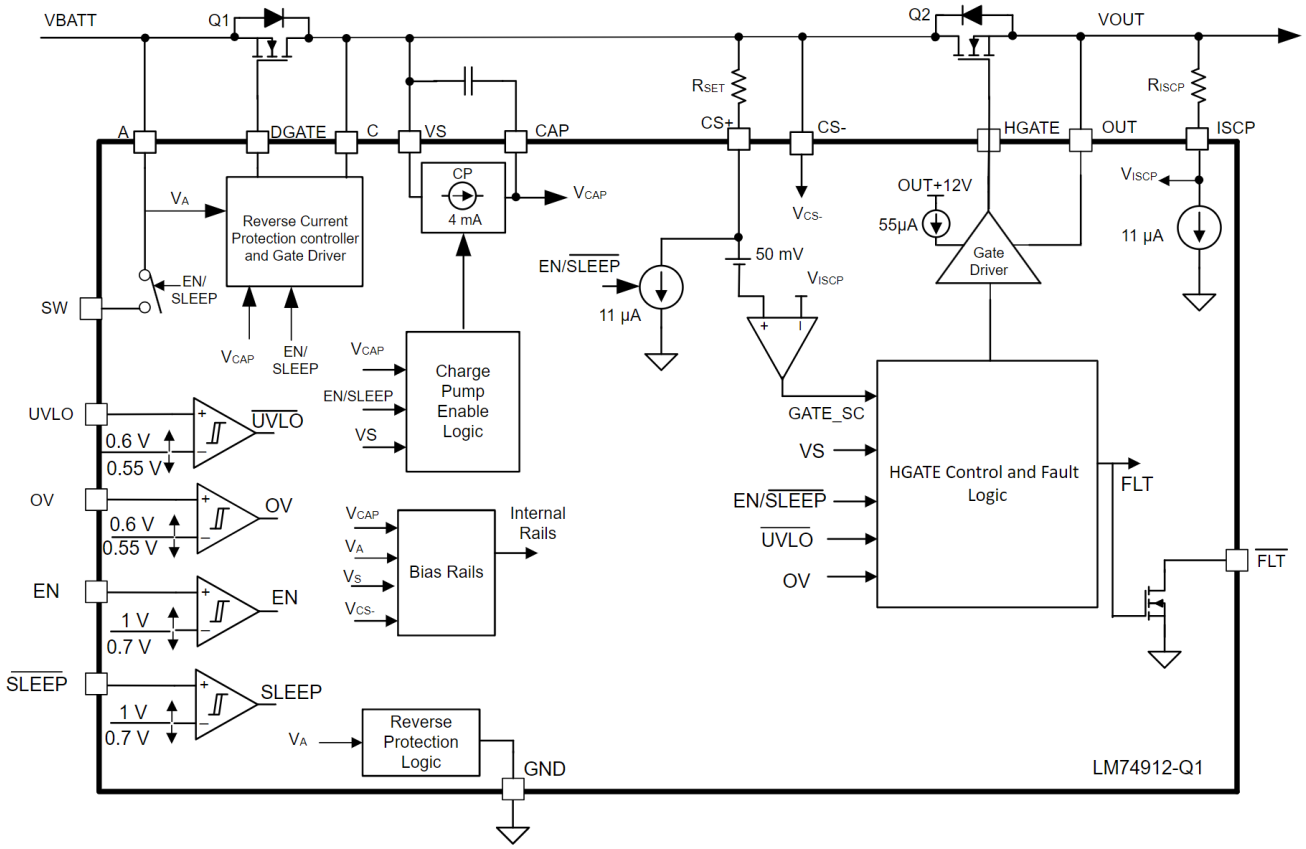

Figure 1-1. Functional Block Diagram

LM74912-Q1 is developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for LM74912-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	14
Die FIT rate	3
Package FIT rate	11

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor control from table 11
- Power dissipation: 42mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS logic	25	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LM74912-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
DGATE output functional, not in specification voltage or timing	13
DGATE stuck at high	10
DGATE stuck at low	14
HGATE output functional, not in specification voltage or timing	8
HGATE stuck at high	4
HGATE stuck at low	16
Short circuit protection fails to trip or false trip	6
SLEEP switch stuck off	8
SLEEP switch stuck on	8
UVLO, OV fails to trip or false trip	8
Pin to pin short	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the LM74912-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the LM74912-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the LM74912-Q1 data sheet.

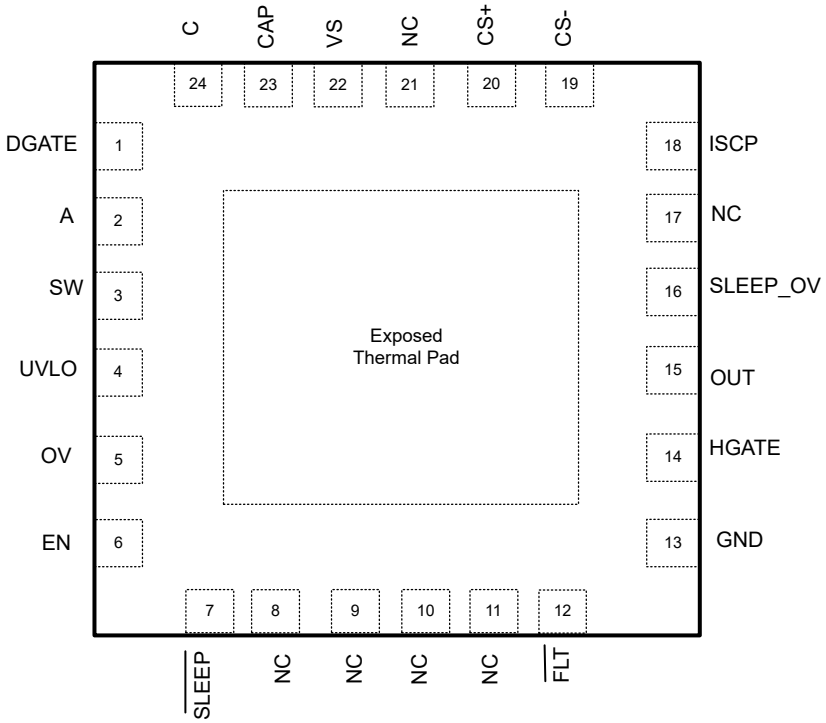

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device is operating under the specified ranges within the *Recommended Operating Conditions* section of the data sheet.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
DGATE	1	Device is damaged due to internal conduction. External DGATE FET can also damage due to maximum VGS rating violation.	A
A	2	Input supply is shorted to ground. Device is not functional.	B
SW	3	Device is damaged if enabled.	A
UVLO	4	Device HGATE drive is off.	B
OV	5	Overvoltage protection functionality is disabled.	B
EN	6	Device is in shutdown mode.	B
$\overline{\text{SLEEP}}$	7	Device is in SLEEP mode.	B
NC	8, 9, 10, 11, 17, 21	No effect on device operation.	D
$\overline{\text{FLT}}$	12	Fault indication functionality is not available.	B
GND	13	No impact on device functionality.	D
HGATE	14	Device is damaged.	A
OUT	15	External FET VGS(max) rating can be exceeded and damage the external FET. The device can experience an increase in quiescent current.	D
SLEEP_OV	16	Overvoltage protection during SLEEP mode is not available.	B
ISCP	18	Device damage is expected due to internal current flow.	A
CS-	19	Device damage is expected due to internal current flow.	A
CS+	20	Device damage is expected due to internal current flow.	A
VS	22	Device does not power up.	B
CAP	23	Device is damaged due to internal conduction between VS and CAP.	A
C	24	Linear regulation functionality and reverse current blocking functionality are not available. Device quiescent current can increase.	B
RTN	—	The input reverse polarity protection feature is not available.	B

Table 4-3. Pin FMA for Device Pins Open Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
DGATE	1	The appropriate diode FET cannot be controlled. The reverse current blocking feature is not available. Load current flows through the body diode of the FET.	B
A	2	The appropriate diode FET is turned off due to linear regulation sink current. Load current flows through the body diode of the FET.	B
SW	3	The battery voltage monitoring feature is not available.	B
UVLO	4	Device HGATE drive is off due to internal pulldown on the UVLO pin.	B
OV	5	Overvoltage protection functionality is disabled as the OV pin is internally pulled low.	B
EN	6	Device is in shutdown mode as the EN pin is internally pulled low.	B
$\overline{\text{SLEEP}}$	7	The SLEEP mode feature is not available.	B
NC	8, 9, 10, 11, 17, 21	No effect on device operation.	D
$\overline{\text{FLT}}$	12	Fault indication functionality is not available.	B
GND	13	Device does not power up.	D
HGATE	14	HGATE control to turn on or turn off the external FET is not available.	B
OUT	15	HGATE control to turn on or turn off the external FET is not available.	D
SLEEP_OV	16	Overvoltage protection during SLEEP mode is not available.	B
ISCP	18	The short circuit protection feature is not available.	B
CS-	19	Device is in overcurrent protection mode and the HGATE drive is turned off.	B
CS+	20	Overcurrent protection and current monitoring output is not available.	B
VS	22	Device does not power up.	B
CAP	23	Charge pump does not build up and gate drives DGATE and HGATE are disabled.	B
C	24	DGATE drive remains off.	B
RTN	—	No effect on device operation.	D

Table 4-4. Pin FMA for Device Pins Short Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
DGATE	1	A	The appropriate diode FET is off. Load current flows through the body diode of the FET.	B
A	2	SW	No effect on device operation.	D
SW	3	UVLO	UVLO feature is not available.	B
UVLO	4	OV	Either OV or UVLO comparator trigger and HGATE is off.	B
OV	5	EN	HGATE drive is off in case device is enabled (EN = High).	B
$\overline{\text{SLEEP}}$	7	NC	No effect on device operation.	D
$\overline{\text{FLT}}$	12	NC	No effect on device operation.	D
GND	13	HGATE	GND shorted to HGATE can cause device damage.	A
HGATE	14	OUT	HGATE FET is off as HGATE is shorted to OUT causing VGS short condition.	B
OUT	15	SLEEP_OV	No effect on device operation. Device supports only overvoltage clamp operation during SLEEP mode.	B
SLEEP_OV	16	NC	No effect on device operation.	B
ISCP	18	NC	No effect on device operation.	D
CS-	19	CS+	Short circuit and overcurrent protection is not available.	B
CS+	20	NC	Overcurrent limit and current monitoring output parameters are out of specification.	B
VS	22	CAP	Device charge pump does not come up. DGATE and HGATE drive are off.	B
CAP	23	C	Device charge pump does not come up. DGATE and HGATE drive are off.	B

Table 4-5. Pin FMA for Device Pins Short Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
DGATE	1	DGATE is shorted to supply. The appropriate diode FET remains off.	B
A	2	No effect on device operation.	D
SW	3	Battery voltage monitoring feature is available irrespective of EN pin status.	B
UVLO	4	UVLO functionality is not available.	B
OV	5	HGATE is turned off due to OV comparator input going high.	B
EN	6	Device is always on as EN is pulled to supply.	B
$\overline{\text{SLEEP}}$	7	SLEEP mode feature is not available.	B
NC	8, 9, 10, 11, 17, 21	No effect on device operation.	D
$\overline{\text{FLT}}$	12	Fault indication functionality is not available.	B
GND	13	Device does not power up due to supply shorted to GND.	D
HGATE	14	HGATE control to turn on or turn off the external FET is not available. Device quiescent current can increase.	B
OUT	15	Supply is shorted to output. The appropriate diode (DGATE) and load disconnect (HGATE) features are not functional as supply is shorted to output.	B
SLEEP_OV	16	Device provides overvoltage cut-off functionality only during SLEEP mode.	B
ISCP	18	Device has a default short circuit protection threshold of 20mV.	B
CS-	19	Overcurrent protection functionality is not available.	B
CS+	20	Device is in overcurrent protection mode.	B
VS	22	No effect on device operation.	B
CAP	23	Charge pump does not build up and gate drives DGATE and HGATE are disabled.	B
C	24	The appropriate diode functionality is not available (reverse current blocking).	B
RTN	—	No effect on device operation.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
February 2025	*	Initial Release

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