

# TMUX1208-Q1

## Functional Safety FIT Rate, FMD and Pin FMA

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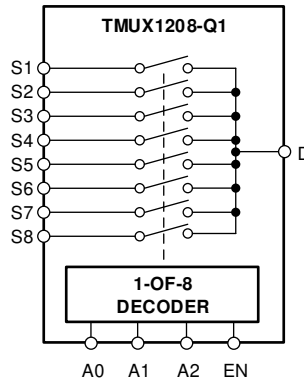
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## 1 Overview

This document contains information for the TMUX1208-Q1 (TMUX1208QRSVRQ1, UQFN package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.



**Figure 1-1. Functional Block Diagram**

The TMUX1208-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

## 2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TMUX1208-Q1 based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

**Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 <sup>9</sup> Hours)
Total component FIT rate	6
Die FIT rate	3
Package FIT rate	3

The failure rate and mission profile information in [Table 2-1](#) comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 94.5mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2**

Table	Category	Reference FIT Rate	Reference Virtual T <sub>J</sub>
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T<sub>J</sub> (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

### 3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TMUX1208-Q1 in [Table 3-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

**Table 3-1. Die Failure Modes and Distribution**

Die Failure Modes	Failure Mode Distribution (%)
MUX no output (HI-Z)	40
MUX channel stuck on	10
MUX channel stuck off	10
MUX functional out of specification voltage or timing	40

## 4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TMUX1208-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

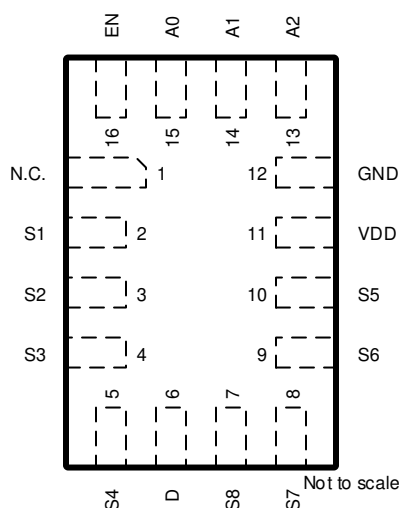
- Pin short-circuited to ground (see [Table 4-2](#))
- Pin open-circuited (see [Table 4-3](#))
- Pin short-circuited to an adjacent pin (see [Table 4-4](#))
- Pin short-circuited to supply (see [Table 4-5](#))

[Table 4-2](#) through [Table 4-5](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

**Table 4-1. TI Classification of Failure Effects**

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

[Figure 4-1](#) shows the TMUX1208-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TMUX1208-Q1 data sheet.



**Figure 4-1. Pin Diagram**

**Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground**

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
NC	1	No effect, unconnected pin.	D
S1	2	Corruption of the signal passed to the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
S2	3	Corruption of the signal passed on to the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
S3	4	Corruption of the signal passed to the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
S4	5	Corruption of the signal passed to the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
D	6	Corruption of the signal passed onto the S pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
S8	7	Corruption of the signal passed to the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
S7	8	Corruption of the signal passed to the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
S6	9	Corruption of the signal passed to the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
S5	10	Corruption of the signal passed to the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
VDD	11	Device is not powered. Device is not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is plausible.	A
GND	12	No effect, normal operation.	D
A2	13	Address stuck low, cannot control switch states.	B
A1	14	Address stuck low, cannot control switch states.	B
A0	15	Address stuck low, cannot control switch states.	B
EN	16	Address stuck low, cannot control switch states.	B

**Table 4-3. Pin FMA for Device Pins Open-Circuited**

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
NC	1	No effect, unconnected pin.	D
S1	2	Corruption of the signal passed to the D pin.	B
S2	3	Corruption of the signal passed to the D pin.	B
S3	4	Corruption of the signal passed to the D pin.	B
S4	5	Corruption of the signal passed to the D pin.	B
D	6	Corruption of the signal passed to the S pins.	B
S8	7	Corruption of the signal passed to the D pin.	B
S7	8	Corruption of the signal passed to the D pin.	B
S6	9	Corruption of the signal passed to the D pin.	B
S5	10	Corruption of the signal passed to the D pin.	B
VDD	11	Device is not powered. Device is not functional.	B
GND	12	Device not powered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible.	A
A2	13	Control of the address pin is lost, cannot control switch.	B
A1	14	Control of the address pin is lost, cannot control switch.	B
A0	15	Control of the address pin is lost, cannot control switch.	B
EN	16	Control of the address pin is lost, cannot control switch.	B

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
NC	1	S1	No connect pin electrically floating, no effect.	D
S1	2	S2	Possible corruption of the signal passed to the D pin.	B
S2	3	S3	Possible corruption of the signal passed to the D pin.	B
S3	4	S4	Not considered, corner pin.	D
S4	5	D	Possible corruption of the signal passed to the SX and D pin.	B
D	6	S8	Possible corruption of the signal passed to the SX and D pin.	B
S8	7	S7	Possible corruption of the signal passed to the D pin.	B
S7	8	S6	Not considered, corner pin.	D
S6	9	S5	Possible corruption of the signal passed to the D pin.	B
S5	10	VDD	Corruption of the signal passed to the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	B
VDD	11	GND	Device likely receives no power. Possible damage to VDD and GND pin.	A
GND	12	A2	Control of the switch state is lost.	B
A2	13	A1	Not considered, corner pin.	D
A1	14	A0	Control of the switch state is lost.	B
A0	15	EN	Control of the switch state is lost.	B
EN	16	NC	Not considered, corner pin.	D

**Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply**

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
NC	1	No effect, unconnected pin.	D
S1	2	Corruption of the signal passed to the D pin. If there is no limiting resistor in the switch path, then device damage is possible	A
S2	3	Corruption of the signal passed to the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
S3	4	Corruption of the signal passed to the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
S4	5	Corruption of the signal passed to the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
D	6	Corruption of the signal passed to the S pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
S8	7	Corruption of the signal passed to the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
S7	8	Corruption of the signal passed to the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
S6	9	Corruption of the signal passed to the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
S5	10	Corruption of the signal passed to the D pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
VDD	11	No effect, normal operation	D
GND	12	Device is not powered. Device is not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is plausible.	A
A2	13	Address stuck low, cannot control switch states.	B
A1	14	Address stuck low, cannot control switch states.	B
A0	15	Address stuck low, cannot control switch states.	B
EN	16	Address stuck low, cannot control switch states.	B

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