Functional Safety Information

INA74X-Q1 Functional Safety FIT Rate, FMD and Pin FMA

1 Overview

This document contains information for INA74X-Q1 (INA745B in 3x5 QFN package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

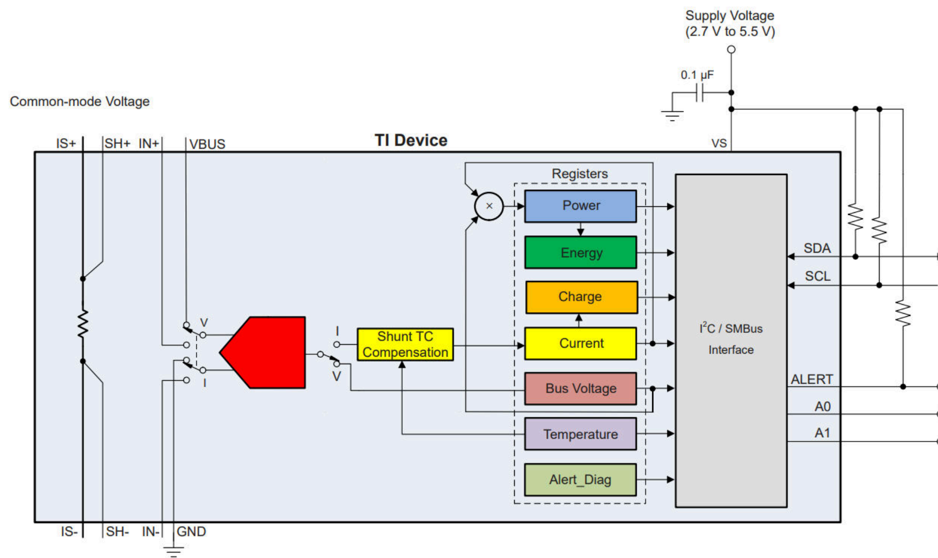

Figure 1-1. Functional Block Diagram

INA74X-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

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2 Functional Safety Failure In Time (FIT) Rates

2.1 3x5 QFN Package

This section provides functional safety failure in time (FIT) rates for the 3x5 QFN package of INA74X-Q1 (INA745B) based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	18
Die FIT rate	9
Package FIT rate	9

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 625mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS/BICMOS ASICs, Analog and Mixed ≤ 50V Supply	60 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for INA74X-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
ADC output bit error	20
ADC gain out of specification	20
ADC offset out of specification	20
Communication error	15
Register bit error	10
ADC mux select error	5
ALERT - false trip or failure to trip	5
Pin to pin short, any two pins	5

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4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the INA74X-Q1 (3x5 QFN package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VS (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- T_A = -40°C to +125°C
- V_S = 3.3V
- V_{CM} = V_{IN-} = 12V

4.1 3x5 QFN Package

Figure 4-1 shows the INA74X-Q1 pin diagrams for the 3x5 QFN package. For a detailed description of the device pins please refer to the corresponding *Pin Configuration and Functions* sections in the INA745 data sheet.

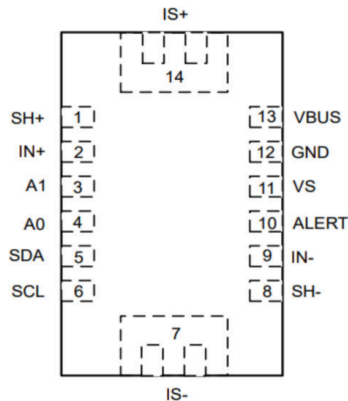

Figure 4-1. Pin Diagram 3x5 QFN Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SH+	1	A short from the bus supply to GND occurs. High current flows from bus supply to GND. Bond wires of pins IN+ and SH+ and die metal trace between pins IN+ and SH+ are damaged.	A
IN+	2	In high-side configuration, a short from the bus supply to GND occurs resulting in high current flow. In low-side configuration, input pins are shorted.	B
A1	3	A1 shorted to GND. No change if initially grounded. Loss of I2C communication if tied to SDA or SCL. Power supply shorted to GND if tied to VS.	D for A1 = GND B otherwise
A0	4	A0 shorted to GND. No change if initially grounded. Loss of I2C communication if tied to SDA or SCL. Power supply shorted to GND if tied to VS.	D for A1=GND B otherwise

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Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SDA	5	SDA shorted to GND. Loss of communication.	B
SCL	6	SCL shorted to GND. Loss of communication.	B
IS-	7	In high-side configuration, a short from the bus supply to GND occurs. High current flows from bus supply to GND. The shunt could be damaged due to high current.	A for high-side
		In low-side configuration, normal operation.	D for low-side
SH-	8	In high-side configuration, a short from the bus supply to GND occurs. High current flows from bus supply to GND. Shunt bond wires of pin SH- and die metal trace between pin IN- and SH- can be damaged.	A for high-side
		In low-side configuration, normal operation.	D for low-side
IN-	9	In high-side configuration, a short from the bus supply to GND occurs resulting in high current flow.	B for high-side;
		In low-side configuration, normal operation.	D for low-side
ALERT	10	ALERT forced to active mode. Loss of ALERT functionality.	B
VS	11	Power supply shorted to GND. No power to the device.	B
GND	12	Normal operation.	D
VBUS	13	VBUS shorted to GND. High current flows from bus supply to GND.	B
IS+	14	A short from the bus supply to GND occurs. High current flows from bus supply to GND. This affects the system functionality but does not affect the IC.	C

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SH+	1	Shunt resistor is not connected to amplifier. IN+ pin floats to an unknown value. Output goes to an unknown value not to exceed VS or GND.	C
IN+	2	Cannot measure sense voltage.	B
A1	3	A1 pin is open. Undefined device address.	B
A0	4	A0 pin is open. Undefined device address.	B
SDA	5	SDA pin is open. Loss of communication.	B
SCL	6	SCL pin is open. Loss of communication.	B
IS-	7	Bus supply to load path is cut off and no load current flows. IN- is at the same potential as bus supply. Differential input voltage is 0V.	C
SH-	8	Shunt resistor is not connected to amplifier. IN- pin floats to an unknown value. Output goes to an unknown value not to exceed VS or GND.	C
IN-	9	Cannot measure sense voltage.	B
ALERT	10	ALERT pin is open. Loss of ALERT functionality.	B
VS	11	No power to the device.	B
GND	12	No power to the device.	B
VBUS	13	VBUS pin floats to an unknown voltage. Any measurements and calculations that depend on VBUS are invalid.	B
IS+	14	Bus supply to load path is cut off and no load current flows. IN+ is at the same potential as GND. Differential input voltage is 0V.	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
SH+	1	2 - IN+	Normal operation.	D
IN+	2	3 - A1	IN+ shorted to A1. No change in low-side configuration. Loss of I2C communication unless A1=GND. Damage possible in high-side configuration.	A for high-side
				B for low-side
A1	3	4 - A0	A1 shorted to A0. No change if A1 and A0 are initially the same. Loss of I2C communication for any short combination between GND, SDA, SCL, or if SCL is tied to VS. Power supply shorted to ground if one pin is Vs and the other is GND. If SDA is shorted to VS, then the device can be damaged when SDA is driven low by the device if input current is > 10mA.	A for SDA to VS
				D for A1 = A0
				B otherwise

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Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
A0	4	5 - SDA	A0 shorted to SDA. Normal operation if A0 = SDA by design.	D if A0 to SDA
				B otherwise
SDA	5	6 - SCL	SDA shorted to SCL. Loss of communication.	B
SCL	6	7 - IS-	SCL shorted to IS-. Loss of I2C communication. Damage is possible in high-side configuration.	A for high-side
				B for low-side
IS-	7	8 - SH-	IS- shorted to SH-. Measurement accuracy is degraded. There is no effect on the IC.	C
SH-	8	9 - IN-	Normal operation.	D
IN-	9	10 - ALERT	IN- shorted to ALERT. In high-side configuration, when ALERT is driven low, device can be damaged.	A for high-side
			In low-side configuration, loss of functionality.	B for low-side
ALERT	10	11 - VS	ALERT shorted to VS. When ALERT is driven low, device can be damaged.	A
VS	11	11 - GND	Power supply shorted to GND. No power to the device.	B
GND	12	12 - VBUS	VBUS shorted to GND. High current flows from bus supply to GND.	B
VBUS	13	14 - IS+	VBUS shorted to IS+. In high-side configuration, normal operation.	D for high-side
			In low-side configuration, VBUS is shorted to GND, resulting in loss of some functionality.	B for low-side
IS+	14	1 - SH+	IS+ shorted to SH+. Measurement accuracy is degraded. There is no effect on the IC.	C

Table 4-5. Pin FMA for Device Pins Short-Circuited to VS

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SH+	1	A short from the bus supply to VS occurs High current flows from bus supply to VS or VS to bus supply. Die metal trace between pin IN+ and SH+ is damaged.	A
IN+	2	In high-side configuration, VBUS shorted to VS. The device could be damaged if VS is driven to a voltage > 6V.	A for high-side
		In low-side configuration, power supply to short to GND. No power to the device.	B for low-side
A1	3	A1 shorted to VS. No change if initially set to VS. Loss of I2C communication if SCL is tied to VS. Power supply shorted to ground if A1 is GND. If A1 is SDA then the device can be damaged when SDA is driven low by the device if input current is > 10mA.	A for A1 = SDA
			D for A1 = VS
			B otherwise
A0	4	A0 shorted to VS. No change if initially set to VS. Loss of I2C communication if SCL is tied to VS. Power supply shorted to ground if A1 is GND. If A1 is SDA then the device can be damaged when SDA is driven low by the device if input current is > 10mA.	A for A0 = SDA
			D for A0 = VS
			B otherwise
SDA	5	SDA shorted to VS. When SDA is driven low, device can be damaged if input current is > 10mA.	A
SCL	6	SCL shorted to VS. Loss of communication.	B
IS-	7	In high-side configuration, a short from the bus supply to VS occurs. High current flows from bus supply to VS or VS to bus supply. The shunt can be damaged due to high current.	A for high-side
		In low-side configuration, system functionality is affected negatively but not the IC.	C for low-side
SH-	8	A short from the bus supply to VS occurs. High current flows from bus supply to VS or VS to bus supply. The shunt and die metal trace between pin IN- and SH- is damaged.	A
IN-	9	In high-side configuration, VBUS shorted to VS. The device can be damaged if VS is driven to a voltage > 6 V.	A for high-side
		In low-side configuration, power supply to short to GND. No power to the device.	B for low-side
ALERT	10	ALERT shorted to VS. When ALERT is driven low, device can be damaged if input current is > 10mA.	A
VS	11	Normal operation.	D
GND	12	Power supply shorted to GND. No power to the device.	B

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Table 4-5. Pin FMA for Device Pins Short-Circuited to VS (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VBUS	13	VBUS shorted to VS. The device can be damaged if VS is driven to a voltage > 6V.	A
IS+	14	In low-side configuration, a short from VS to GND occurs. The shunt can be damaged due to high current.	A for low-side
		In high-side configuration, bus supply is shorted to VS and system functionality is affected negatively but not the IC.	C for high-side

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