Functional Safety Information

TPS7B87-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the TPS7B87-Q1 (TO-252 and HSOIC packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

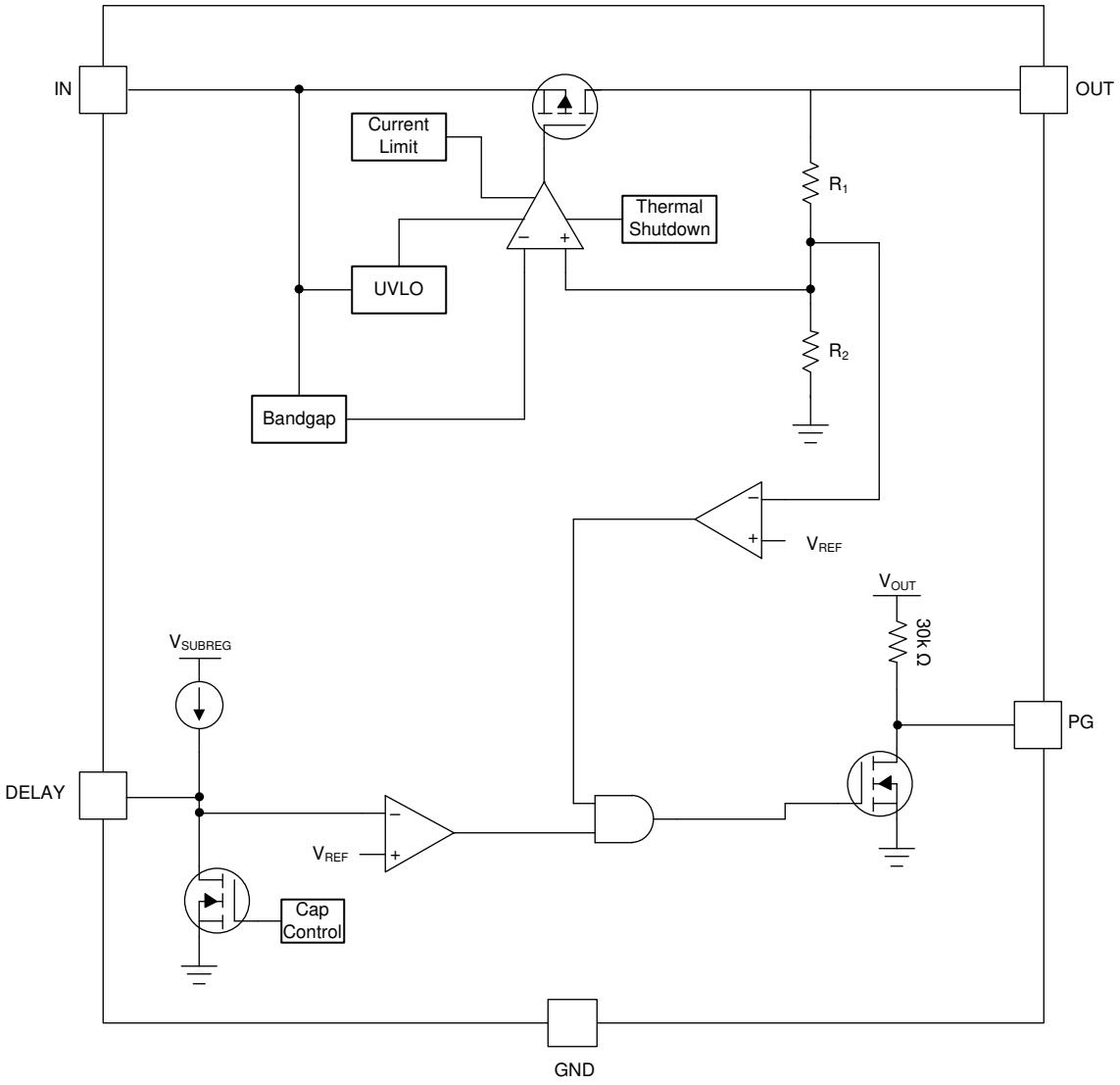

Figure 1-1. Functional Block Diagram

The TPS7B87-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 TO-252 Package

This section provides functional safety failure in time (FIT) rates for the TO-252 package of the TPS7B87-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	15
Die FIT rate	4
Package FIT rate	11

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 500mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS and BICMOS ASICs, analog, and mixed ≤ 50V supply	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 HSOIC Package

This section provides functional safety failure in time (FIT) rates for the HSOIC package of the TPS7B87-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	14
Die FIT rate	5
Package FIT rate	9

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 500mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS and BICMOS ASICs, analog, and mixed ≤ 50V supply	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS7B87-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT high (following VIN)	15
VOUT not in specification (voltage or timing)	60
VOUT low (no output)	15
PG false trigger, fails to trigger	5
Short circuit any two pins	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS7B87-Q1 (TO-252 and HSOIC packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2 and Table 4-6)
- Pin open-circuited (see Table 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8)
- Pin short-circuited to V_{IN} (see Table 4-5 and Table 4-9)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device operates at free-air temperatures between -40°C and 150°C.
- Device operates at an input voltage of at least 3V and no more than 40V.
- Device operates according to all recommended operating conditions, and the absolute maximum ratings in the device data sheet are not exceeded.
- NC pins are floating.

4.1 TO-252 Package

Figure 4-1 shows the TPS7B87-Q1 pin diagram for the TO-252 package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS7B87-Q1 data sheet.

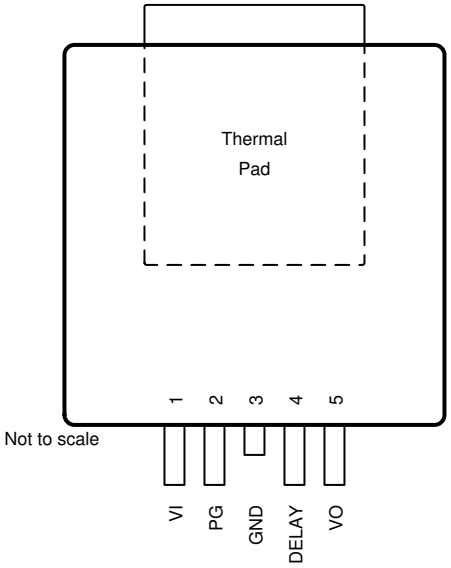

Figure 4-1. Pin Diagram (TO-252 Package)

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	Power is not supplied to the device. System performance depends on upstream current limiting.	B
PG	2	Power-good never asserts when the output voltage is at target, thus, potentially effecting power sequencing.	B
GND	3	No effect. Normal operation.	D
DELAY	4	Ground current is permanently increased.	C
OUT	5	Regulation is not possible; the device operates at current limit. The device can cycle in and out of thermal shutdown.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	Power is not supplied to the device, resulting in no output voltage.	B
PG	2	The power-good signal is not accessible. Power sequencing can be effected.	B
GND	3	There is no current loop for the supply voltage. The device is not operational and does not regulate.	B
DELAY	4	The power-good delay is set to the minimum delay time, $t_{(DLY\_FIX)}$.	C
OUT	5	The device output is disconnected from the load.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
IN	1	2 - PG	Power-good functionality cannot operate correctly. PG can be damaged if the absolute maximum rating (20V) is violated.	A
				B
PG	2	3 - GND	Power-good never asserts when the output voltage is at target, thus, potentially effecting power sequencing.	B
GND	3	4 - DELAY	Ground current is permanently increased.	C
DELAY	4	5 - OUT	PG can incorrectly assert when the output voltage is not at target. The pin absolute maximum rating (6V max) can be exceeded and the pin can be damaged.	A
				B

Table 4-5. Pin FMA for Device Pins Short-Circuited to V_{IN}

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	No effect. Normal operation.	D
PG	2	Power-good functionality cannot operate correctly. PG can be damaged if the absolute maximum rating (20V) is violated.	A
			B
GND	3	Power is not supplied to the device. System performance depends on upstream current limiting.	B
DELAY	4	PG can incorrectly assert when the output voltage is not at target. The pin absolute maximum rating (6V max) can be exceeded and the pin can be damaged.	A
			B
OUT	5	Output held at V_{IN}, regulation is not possible. Damage is possible if the absolute maximum rating is exceeded (20V max).	A
			B

4.2 HSOIC Package B Version

Figure 4-2 shows the TPS7B87-Q1 pin diagram for the HSOIC package B version with PG. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS7B87-Q1 data sheet.

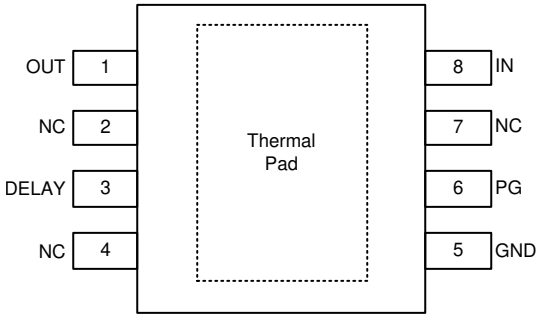

Figure 4-2. Pin Diagram
(HSOIC Package B Version With PG)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Regulation is not possible, the device operates at current limit. The device can cycle in and out of thermal shutdown.	B
NC	2	No effect. Normal operation.	B
DELAY	3	Ground current is permanently increased.	C
NC	4	No effect. Normal operation.	D
GND	5	No effect. Normal operation.	D
PG	6	Power-good never asserts when the output voltage is at target, thus, potentially effecting power sequencing.	B
NC	7	No effect. Normal operation.	D
IN	8	Power is not supplied to the device. System performance depends on upstream current limiting.	B

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	The device output is disconnected from the load.	B
NC	2	No effect. Normal operation.	D
DELAY	3	The power-good delay is set to the minimum delay time, $t_{(DLY\_FIX)}$.	C
NC	4	No effect. Normal operation.	D
GND	5	There is no current loop for the supply voltage. The device is not operational and does not regulate.	B
PG	6	The power-good signal is not accessible. Power sequencing can be effected.	B
NC	7	No effect. Normal operation.	D
IN	8	Power is not supplied to the device, resulting in no output voltage.	B

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
OUT	1	2 - NC	No effect. Normal operation.	D
NC	2	3 - DELAY	No effect. Normal operation.	D
DELAY	3	4 - NC	No effect. Normal operation.	D
GND	5	6 - PG	Power-good functionality cannot operate correctly, always low.	B
PG	6	7 - NC	No effect. Normal operation.	D
NC	7	8 - IN	No effect. Normal operation.	D

Table 4-9. Pin FMA for Device Pins Short-Circuited to V_{IN}

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Output held at V_{IN}, regulation is not possible. Damage is possible if the absolute maximum rating is exceeded (20V max).	A
NC	2	No effect. Normal operation.	D
DELAY	3	PG can incorrectly assert when the output voltage is not at target. The pin absolute maximum rating (6V max) can be exceeded and the pin can be damaged.	A
			B
NC	4	No effect. Normal operation.	D
GND	5	Power is not supplied to the device. System performance depends on upstream current limiting.	B
PG	6	Power-good functionality cannot operate correctly. PG can be damaged if the absolute maximum rating (20V) is violated.	A
			B
NC	7	No effect. Normal operation.	D
IN	8	No effect. Normal operation.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2025	*	Initial Release

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