Functional Safety Information

UCC27624V-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for the UCC27624V-Q1 (D, DGN, DDA, and DGK packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

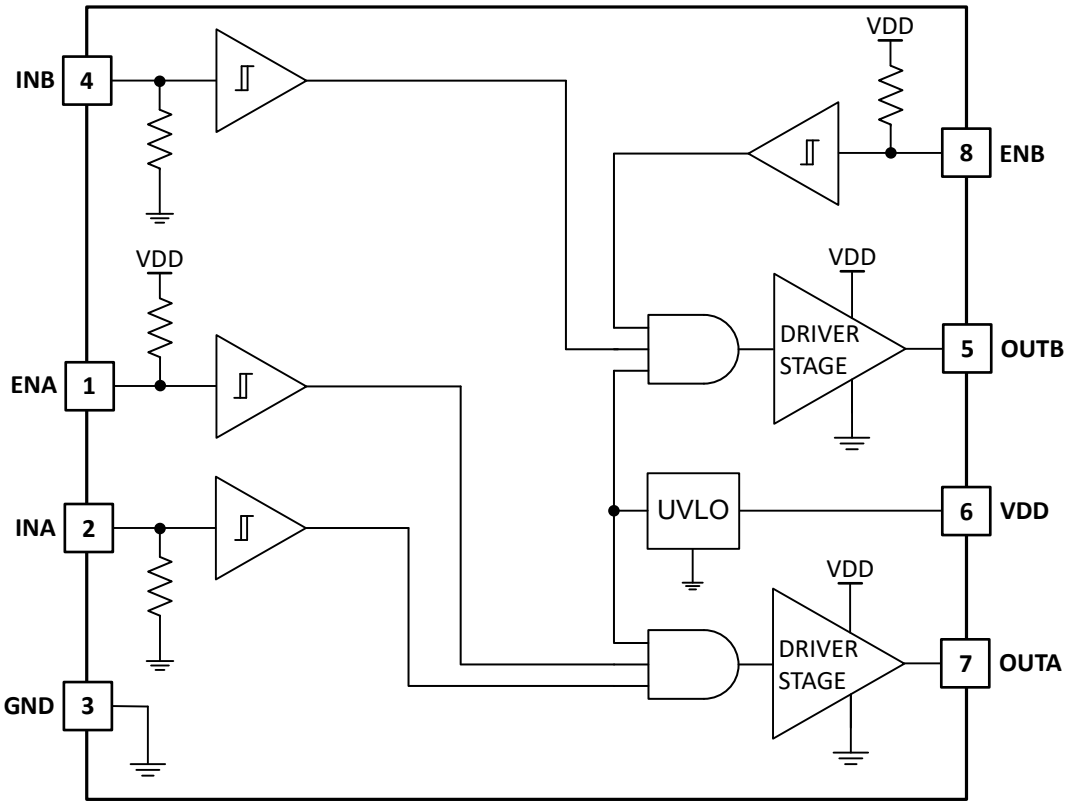

Figure 1-1. Functional Block Diagram

The UCC27624V-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 D and DDA Package

This section provides functional safety failure in time (FIT) rates for the D and DDA package of the UCC27624V-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	13
Die FIT rate	5
Package FIT rate	8

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 200mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 DGN and DGK Package

This section provides functional safety failure in time (FIT) rates for the DGN and DGK package of the UCC27624V-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	9
Die FIT rate	5
Package FIT rate	4

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 500mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the UCC27624V-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUTA stuck high	7
OUTA stuck low	7
OUTA functioning out of specification	7
OUTB stuck high	7
OUTB stuck low	7
OUTB functioning out of specification	7
ENA stuck high	7
ENA stuck low	7
ENA functioning out of specification	7
ENB stuck high	7
ENB stuck low	7
ENB functioning out of specification	7
UVLO false reporting	13
Test mode | EMI performance	3

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the UCC27624V-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1, Figure 4-2, Figure 4-3, and Figure 4-4 show the UCC27624V-Q1 pin diagrams. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the UCC27624V-Q1 datasheet.

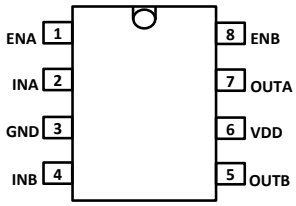

Figure 4-1. D Package Pin Diagram

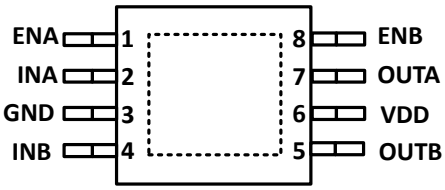

Figure 4-2. DGN Package Pin Diagram

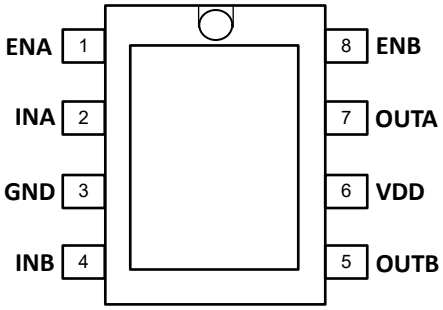

Figure 4-3. DDA Package Pin Diagram

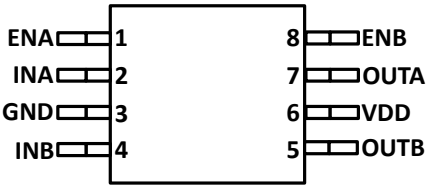

Figure 4-4. DGK Package Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Pin 1 shorted to pin 8, and pin 4 shorted to pin 5, are not considered.
- The case of a short-circuit to supply is analyzed as a short to VDD.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
ENA	1	The function of the ENA pin is disabled. The OUTA pin does not respond to the INA pin.	B
INA	2	The function of the INA pin is lost. The OUTA pin is stuck low.	B
GND	3	There is no impact on the device.	D
INB	4	The function of the INB pin is lost. The OUTB pin is stuck low.	B
OUTB	5	The OUTB pin is stuck low. The OUTB pin is short circuited if the INB pin is commanded *High*.	A
VDD	6	There is an undervoltage of the VDD pin. The OUTA and OUTB pins are off.	B
OUTA	7	The OUTA pin is stuck low. The OUTA pin is short circuited if the INA pin is commanded *High*.	A
ENB	8	The function of the ENB pin is disabled. The OUTB pin does not respond to the INB pin.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
ENA	1	The OUTA pin is always enabled. The OUTA pin responds to the INA pins.	B
INA	2	The function of the INA pin is lost. The OUTA pin is stuck low.	B
GND	3	The state of the OUTA and OUTB pins are unknown.	B
INB	4	The function of the INB pin is lost. The OUTB pin is stuck low.	B
OUTB	5	The OUTB pin is disconnected from the power FET.	B
VDD	6	There is an undervoltage of the VDD pin. The OUTA and OUTB pins are off.	B
OUTA	7	The OUTA pin is disconnected from the power FET.	B
ENB	8	The OUTB pin is always enabled. The OUTB pin responds to the INB pin.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
ENA	1	INA	The ENA pin cannot override the command of the INA pin. The OUTA pin responds to the INA pin.	B
INA	2	GND	The OUTA pin is stuck low.	B
GND	3	INB	The OUTB pin is stuck low.	B
OUTB	5	VDD	The OUTB pin is stuck high.	A
VDD	6	OUTA	The OUTA pin is stuck high.	A
OUTA	7	ENB	The function of the ENB pin depends on the state of the INA (OUTA) pin.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
ENA	1	The OUTA pin is always enabled. The OUTA pin responds to the INA pin.	B
INA	2	The OUTA pin is stuck high.	B
GND	3	The power supply is short circuited.	B
INB	4	The OUTB pin is stuck high.	B
OUTB	5	The OUTB pin is stuck high.	A
VDD	6	There is no impact on the device.	D
OUTA	7	The OUTA pin is stuck high.	A
ENB	8	The OUTB pin is always enabled. The OUTB pin responds to the INB pin.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from March 31, 2026 to May 12, 2026 (from Revision * (March 2026) to Revision A (May 2026)) **Page**

- Updated content and values in the *Die Failure Modes and Distribution* table.....5

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025