Functional Safety Information

TPS482H85-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the TPS482H85-Q1 (CHU (VQFN-HR, 12) package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

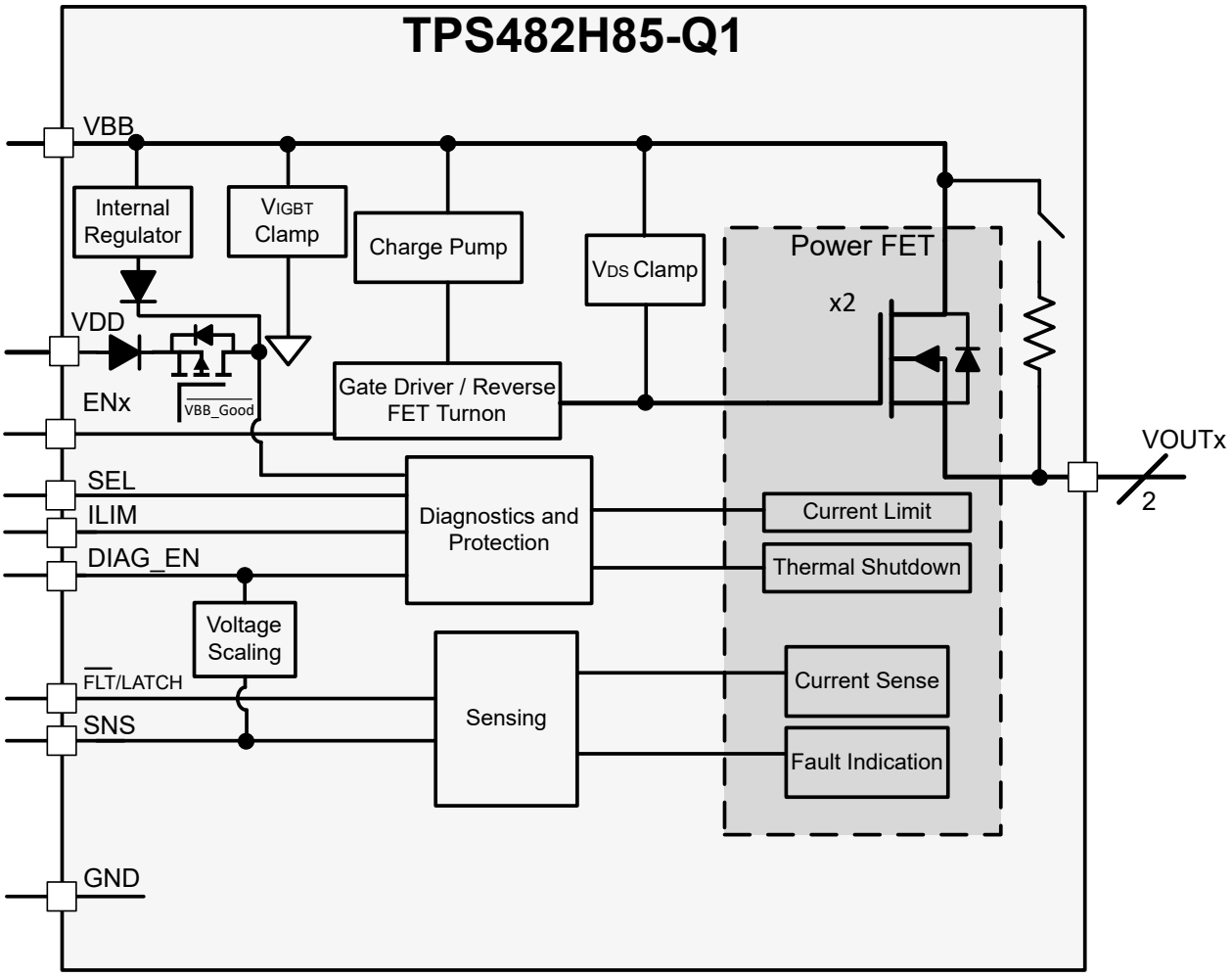

Figure 1-1. Functional Block Diagram

The TPS482H85-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TPS482H85-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	20
Die FIT rate	13
Package FIT rate	7

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 750mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): From table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS482H85-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT open (Hi-Z)	20
VOUT stuck ON to VBB	10
VOUT functional – not in specification voltage or timing	50
Diagnostics not in specification	10
Protection function fails to trip	10

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS482H85-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TPS482H85-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS482H85-Q1 data sheet.

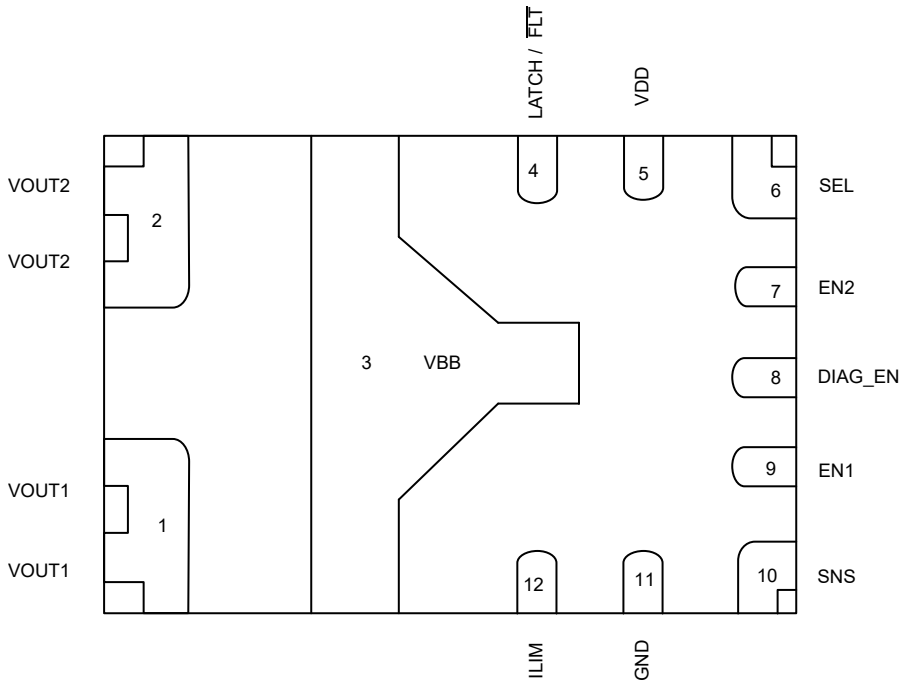

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device pins are connected per the recommendation in the data sheet, including pullup and pulldown resistors, as needed.
- The data sheet recommendations for operating conditions, external component selection, and PCB layout are followed.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VOUT1	1	The current limit of the output channel engages, and thermal protection turns off the FET.	B
VOUT2	2	The current limit of the output channel engages, and thermal protection turns off the FET.	B
VBB	3	The output stages are not powered, and the FET does not turn ON.	B
LATCH / $\overline{\text{FLT}}$	4	For the A and C variants, fault recovery is set at auto-retry mode. For the B variant, the reported fault status is potentially erroneous.	B
VDD	5	The internal regulator is enabled; the device consumes higher quiescent current through the VBB pin.	C
SEL	6	When the DIAG_EN pin is high, the SNS output shows the signal corresponding to channel 1.	B
EN2	7	The main FET for channel 2 is turned off.	B
DIAG_EN	8	Diagnostics features do not function, including current sense and fault reporting.	B
EN1	9	The main FET for channel 1 is turned off.	B
SNS	10	The reported SNS current or fault status on the SNS pin is erroneous.	B
GND	11	Any GND network, connected for protection, is bypassed.	B
ILIM	12	The current limit is set at 9A.	C

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VOUT1	1	During the OFF state of the device, if the DIAG_EN pin is high, an open-load fault reports.	B
VOUT2	2	During the OFF state of the device, if the DIAG_EN pin is high, an open-load fault reports.	B
VBB	3	The device is not powered, and the switch is kept OFF.	B
LATCH / $\overline{\text{FLT}}$	4	For the A and C variants, fault recovery is set at auto-retry mode. For the B variant, the fault condition is not reported.	B
VDD	5	The internal regulator is enabled, the device consumes higher quiescent current through the VBB pin.	C
SEL	6	When the DIAG_EN pin is high, the SNS output shows the signal corresponding to channel 1.	B
EN2	7	The main FET for channel 2 is turned off.	B
DIAG_EN	8	Diagnostics features do not function; including current sense and fault reporting.	B
EN1	9	The main FET for channel 1 is turned off.	B
SNS	10	The current sense voltage of the pin is clamped internally and no current sense information is available.	B
GND	11	The loss of ground detection engages, and the device turns OFF.	B
ILIM	12	The current limit is set at 10A.	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
VOUT1	1	VOUT2	If the outputs are shorted together during power-up, a thermal shutdown potentially occurs. If the outputs are shorted after power-up, a thermal shutdown does not occur, but a parametric shifts potentially occurs.	B
VOUT2	2	VBB	The output for channel 2 is pulled to the supply voltage. A short-to-battery detection triggers during the OFF state if the DIAG_EN pin is high.	B
VBB	3	LATCH / $\overline{\text{FLT}}$	No effect, the pin is rated for VBB.	D
LATCH / $\overline{\text{FLT}}$	4	VDD	For the A and C variants, fault recovery can be permanently set to latch mode. For the B variant, the fault condition potentially does not report. The internal regulator can also be enabled, and the device can consume higher quiescent current through the VBB pin.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
VDD	5	SEL	The SNS output shows the signal corresponding to channel 2 only, or the internal regulator is enabled, and the device consumes higher quiescent current through the VBB pin.	B
SEL	6	EN2	The SNS output potentially does not show the signal corresponding to the selected channel, or the main FET for channel 2 is potentially turned off.	B
EN2	7	DIAG_EN	The diagnostic features potentially do not function. The main FET for channel 2 can also turn off.	B
DIAG_EN	8	EN1	The diagnostic features potentially do not function. The main FET for channel 1 can also turn off.	B
EN1	9	SNS	The current sense information is potentially erroneous, assuming the EN1 voltage does not exceed the ADC pin voltage rating. The main FET for channel 1 can also turn off.	B
SNS	10	GND	The reported SNS current or fault status on the SNS pin is erroneous.	B
GND	11	ILIM	The current limit is set at 9A.	C
ILIM	12	VBB	No effect, the pin is rated for VBB.	D
VBB	3	VOUT1	The output for channel 1 is pulled to the supply voltage. A short-to-battery detection triggers during the OFF state if the DIAG_EN pin is high.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VOUT1	1	The output is pulled to the supply voltage. A short-to-battery detection triggers during the OFF state if the DIAG_EN pin is high.	B
VOUT2	2	The output is pulled to the supply voltage. A short-to-battery detection triggers during the OFF state if the DIAG_EN pin is high.	B
VBB	3	No effect.	D
LATCH / $\overline{\text{FLT}}$	4	No effect.	D
VDD	5	There is a potential violation of the absolute maximum rating for the pin and a possible breakdown of the ESD cell.	A
SEL	6	There is a potential violation of the absolute maximum rating for the pin and a possible breakdown of the ESD cell.	A
EN2	7	There is a potential violation of the absolute maximum rating for the pin and a possible breakdown of the ESD cell.	A
DIAG_EN	8	There is a potential violation of the absolute maximum rating for the pin and a possible breakdown of the ESD cell.	A
EN1	9	There is a potential violation of the absolute maximum rating for the pin and a possible breakdown of the ESD cell.	A
SNS	10	There is a potential violation of the absolute maximum rating for the pin and a possible breakdown of the ESD cell.	A
GND	11	The supply power is bypassed, and the device stays OFF.	B
ILIM	12	No effect.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2025	*	Initial Release

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265