



Table of Contents

1 Overview	2
2 Functional Safety Failure In Time (FIT) Rates	3
2.1 DUW-16 Ultra-Wide-SSOP Package.....	3
3 Failure Mode Distribution (FMD)	4
4 Pin Failure Mode Analysis (Pin FMA)	5
4.1 DUW-16 Ultra-Wide-SSOP Package	5
5 Revision History	10

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1 Overview

This document contains information for the ISO7742U (DUW-16 Ultra-Wide-SSOP packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

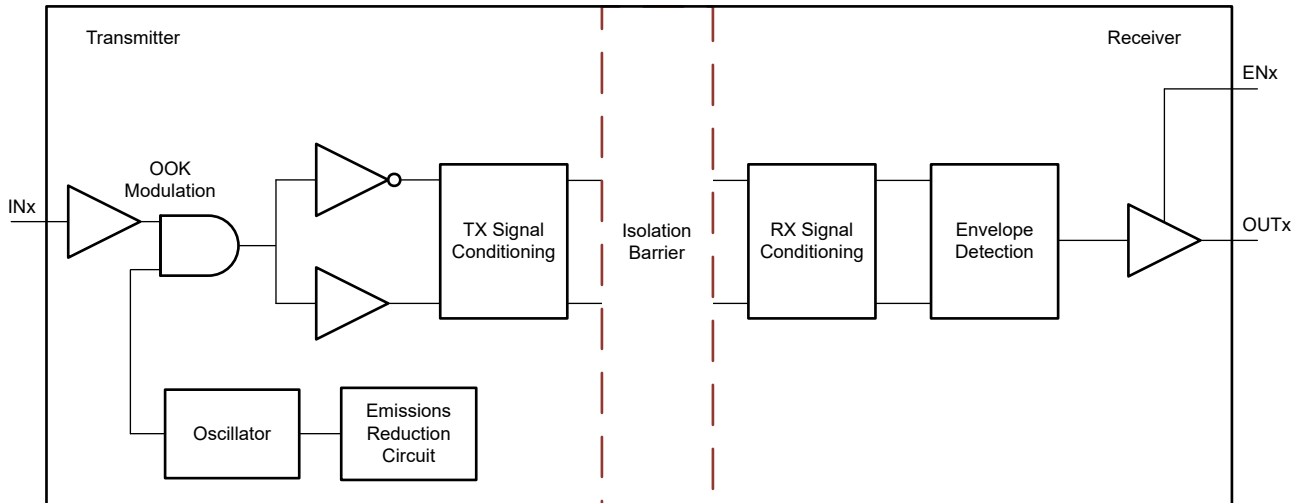


Figure 1-1. Functional Block Diagram

The ISO7742U was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

ADVANCE INFORMATION for preproduction products; subject to change without notice.

2 Functional Safety Failure In Time (FIT) Rates

2.1 DUW-16 Ultra-Wide-SSOP Package

This section provides functional safety failure in time (FIT) rates for the DUW-16 Ultra-Wide-SSOP package of the ISO7742U based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours)
Total component FIT rate	98
Die FIT rate	3
Package FIT rate	95

The failure rate and mission profile information in [Table 2-1](#) comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 143.6mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): From table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T _J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the ISO7742U in [Table 3-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUTx state is undetermined	35
OUTx is stuck to default state	25
OUTx is not in timing or voltage specification	30
OUTx is stuck high	5
OUTx is stuck low	5

The FMD in the *Die Failure Modes and Distribution* table excludes short-circuit faults across the isolation barrier. Faults for short circuits across the isolation barrier can be excluded according to IEC 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a safety-separated extra low voltage (SELV) or protective extra low voltage (PELV) power supply is used, pollution degree 2 / OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the ISO7742U (DUW-16 Ultra-Wide-SSOP packages). See the following section for pin FMA by package. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground
- Pin open-circuited
- Pin short-circuited to an adjacent pin
- Pin short-circuited to supply

The pin FMA by pinout (see following section) indicates how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

Table 4-1. TI Classification of Failure Effects

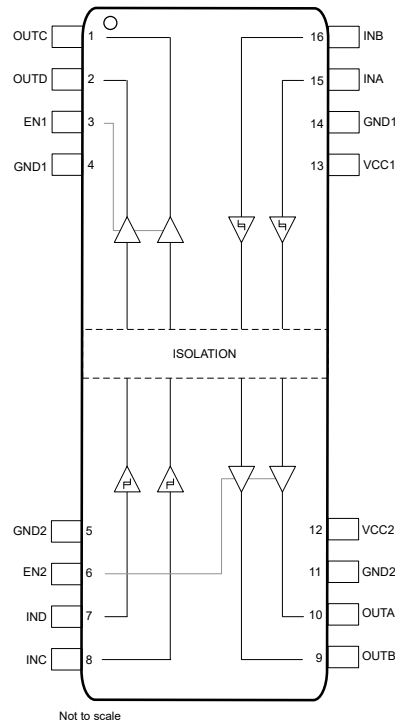
Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- For short-to-ground analysis, the ground referenced for the short is the ground on that side of the isolation barrier.
- For short-to-supply analysis, the supply referenced for the short is the supply on that side of the isolation barrier.
- The default output levels for the outputs of OUTx are:
 - High for: ISO7742U
 - Low for: ISO7742UF

4.1 DUW-16 Ultra-Wide-SSOP Package

[Figure 4-1](#) shows the ISO7742U pin diagram for the DUW-16 Ultra-Wide-SSOP package packages. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the [ISO7742U](#) datasheet.


Figure 4-1. Pin Diagram (DUW-16 Ultra-Wide-SSOP Package)
Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground, Open-Circuited, Short-Circuited to Adjacent Pin, and Short-Circuited to Supply

Pin Name	Pin Number	Potential Failure Mode	Description of Potential Failure Effects	Failure Effect Class
OUTC	1	Short-Circuited to Ground (Side-2)	The output of OUTC is shorted to ground. Communication through channel C is corrupted. Damage to the device is possible if INC is driven high for an extended period of time.	A
OUTC	1	Open-Circuited	The state of the OUTC output is undetermined. Communication through channel C is corrupted.	B
OUTC	1	Short-Circuited to Pin2 (OUTD)	Communication is corrupted for either channel or both channels. With an opposite logic state on both channels, high current can flow between the pins, supply, and ground and possibly cause damage to the device.	A
OUTC	1	Short-Circuited to Supply (Side-2)	The output of OUTC is stuck high. Communication through channel C is corrupted. Device damage is possible if INC is driven low for an extended period of time.	A
OUTD	2	Short-Circuited to Ground (Side-1)	The output of OUTD is shorted to ground. Communication through channel D is corrupted. Damage to the device is possible if IND is driven high for an extended period of time.	A
OUTD	2	Open-Circuited	The output state of OUTD is undetermined. Communication through channel D is corrupted.	B
OUTD	2	Short-Circuited to Pin3 (EN1)	Data communication is corrupted on OUTC and OUTD. If EN1 is pulled to the supply externally, damage to the device is possible when OUTD is driven low for an extended duration.	A
OUTD	2	Short-Circuited to Supply (Side-1)	OUTD is stuck high. Communication through channel D is corrupted. Damage to the device is possible if IND is driven low for an extended period of time.	A
EN1	3	Short-Circuited to Ground (Side-1)	EN1 is stuck low, so the output buffers for OUTC and OUTD are not enabled. Communication is corrupted for channel C and D.	B
EN1	3	Open-Circuited	Control on the input of EN1 is lost. EN1 has a weak internal pullup to VCC1. Communication on channels C and D continues normally since the weak internal pullup to VCC1 on EN1 enables the output buffers for OUTC and OUTD.	B

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground, Open-Circuited, Short-Circuited to Adjacent Pin, and Short-Circuited to Supply (continued)

Pin Name	Pin Number	Potential Failure Mode	Description of Potential Failure Effects	Failure Effect Class
EN1	3	Short-Circuited to Pin4 (GND1)	EN1 is stuck low, so the output buffers for OUTC and OUTD are not enabled. Communication is corrupted for channel C and D.	B
EN1	3	Short-Circuited to Supply (Side-1)	Control on the input of EN1 is lost since EN1 is shorted to a logic high. Communication on channels C and D continues normally since the high on EN1 enables the output buffers for OUTC and OUTD.	B
GND1	4	Short-Circuited to Ground (Side-1)	The device continues to function as expected. Normal operation.	D
GND1	4	Open-Circuited	The device receives return ground through pin 14 (GND1). Normal operation.	D
GND1	4	Short-Circuited to Pin5 (N/A)	Not applicable (N/A) across the isolation barrier	N/A
GND1	4	Short-Circuited to Supply (Side-1)	The device has no power on side-1 (the supply input is shorted to ground). The outputs of OUTA, OUTB, and OUTC are at the default logic state. The output state of OUTD is undetermined. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, damage to the device is possible. This short circuit potentially causes high current to flow between the two GND1 pins (pin4 and pin14); potentially damaging device.	A
GND2	5	Short-Circuited to Ground (Side-2)	The device continues to function as expected. Normal operation.	D
GND2	5	Open-Circuited	The device receives return ground through pin 11 (GND2). Normal operation.	D
GND2	5	Short-Circuited to Pin6 (EN2)	EN2 is stuck low, so the output buffers for OUTA and OUTB are not enabled. Communication is corrupted for channels A and B.	B
GND2	5	Short-Circuited to Supply (Side-2)	The device has no power on side-2 (the supply input is shorted to ground). The output of OUTD is at the default logic state. The output states of OUTA, OUTB, and OUTC are undetermined. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, damage to the device is possible. This short circuit potentially causes high current to flow between the two GND2 pins (pin5 and pin11); potentially damaging the device.	A
EN2	6	Short-Circuited to Ground (Side-2)	EN2 is stuck low so the output buffers for OUTA and OUTB OUTC are not enabled. Communication is corrupted for channels A and B.	B
EN2	6	Open-Circuited	Control on the input of EN2 is lost. EN2 has a weak internal pullup to VCC2. Communication on channels A and B continues normally since the weak internal pullup to VCC2 on EN2 enables the output buffers for OUTA and OUTB.	B
EN2	6	Short-Circuited to Pin7 (IND)	Communication is corrupted on all channels. The shorted external signals to EN2 and IND result in an unpredictable and non-deterministic level at the EN2 and IND inputs when the input level to EN2 and the input level to IND do not match. Thus, the enable status of the output buffers from EN2, which impacts channels A and B, is unknown, as are the levels of OUTA and OUTB. The input level to IND is unknown, as is the output on OUTD.	B
EN2	6	Short-Circuited to Supply (Side-2)	Control on the input of EN2 is lost since EN2 is shorted to a logic high. Communication from the on channels A and B continues normally since the high on EN2 enables the output buffers for OUTA and OUTB.	B
IND	7	Short-Circuited to Ground (Side-2)	The input signal is shorted to ground, so the output of OUTD is stuck low. Communication through channel D is corrupted.	B

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground, Open-Circuited, Short-Circuited to Adjacent Pin, and Short-Circuited to Supply (continued)

Pin Name	Pin Number	Potential Failure Mode	Description of Potential Failure Effects	Failure Effect Class
IND	7	Open-Circuited	Communication through channel D is not possible. The output of OUTD is at the default state (weak internal pullup or pulldown to the default state).	B
IND	7	Short-Circuited to Pin8 (INC)	Communication is corrupted for either channel or both channels.	B
IND	7	Short-Circuited to Supply (Side-2)	The input signal is shorted to supply, so the output of OUTD is stuck high. Communication through channel D is corrupted.	B
INC	8	Short-Circuited to Ground (Side-1)	The input signal is shorted to ground, so the output of OUTC is stuck low. Communication through channel C is corrupted.	B
INC	8	Open-Circuited	Communication through channel C is not possible. The output of OUTC is at the default state (weak internal pullup or pulldown to the default state).	B
INC	8	Short-Circuited to Pin2 (OUTB)	Not applicable (N/A), corner pin.	N/A
INC	8	Short-Circuited to Supply (Side-1)	The input signal is shorted to supply, so the output of OUTC is stuck high. Communication through channel C is corrupted.	B
OUTB	9	Short-Circuited to Ground (Side-2)	The output of OUTB is shorted to ground. Communication through channel B is corrupted. Damage to the device is possible if INB is driven high for an extended period of time.	A
OUTB	9	Open-Circuited	The state of the OUTB output is undetermined. Communication through channel B is corrupted.	B
OUTB	9	Short-Circuited to Pin10 (OUTA)	Communication is corrupted for either channel or both channels. With an opposite logic state on both channels, high current can flow between the pins, supply, and ground and possibly cause damage to the device.	A
OUTB	9	Short-Circuited to Supply (Side-2)	The output of OUTB is stuck high. Communication through channel B is corrupted. Device damage is possible if INB is driven low for an extended period of time.	A
OUTA	10	Short-Circuited to Ground (Side-2)	The output of OUTA is shorted to ground. Communication through channel A is corrupted. Damage to the device is possible if INA is driven high for an extended period of time.	A
OUTA	10	Open-Circuited	The state of the OUTA output is undetermined. Communication through channel A is corrupted.	B
OUTA	10	Short-Circuited to Pin11 (GND2)	The output of OUTA is shorted to ground. Communication through channel A is corrupted. Damage to the device is possible if INA is driven high for an extended period of time.	A
OUTA	10	Short-Circuited to Supply (Side-2)	The output of OUTA is stuck high. Communication through channel A is corrupted. Device damage is possible if INA is driven low for an extended period of time.	A
GND2	11	Short-Circuited to Ground (Side-2)	The device continues to function as expected. Normal operation.	D
GND2	11	Open-Circuited	The device receives return ground through pin 5 (GND2). Normal operation.	D
GND2	11	Short-Circuited to Pin12 (VCC2)	The device has no power on side-2 (the supply input is shorted to ground). The output of OUTD is at the default logic state. The output states of OUTA, OUTB, and OUTC are undetermined. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, damage to the device is possible. This short circuit potentially causes high current to flow between the two GND2 pins (pin5 and pin11); potentially damaging the device.	A

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground, Open-Circuited, Short-Circuited to Adjacent Pin, and Short-Circuited to Supply (continued)

Pin Name	Pin Number	Potential Failure Mode	Description of Potential Failure Effects	Failure Effect Class
GND2	11	Short-Circuited to Supply (Side-2)	The device has no power on side-2 (the supply input is shorted to ground). The output of OUTD is at the default logic state. The output states of OUTA, OUTB, and OUTC are undetermined. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, damage to the device is possible. This short circuit potentially causes high current to flow between the two GND2 pins (pin5 and pin11); potentially damaging the device.	A
VCC2	12	Short-Circuited to Ground (Side-2)	The device has no power on side-2 (the supply input is shorted to ground). The output of OUTD is at the default logic state. The output states of OUTA, OUTB, and OUTC are undetermined. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, damage to the device is possible. This short circuit potentially causes high current to flow between the two GND2 pins (pin5 and pin11); potentially damaging the device.	A
VCC2	12	Open-Circuited	The device has no power on side-2 (the supply input is open). The output of OUTD is at the default logic state. The output states of OUTA, OUTB, and OUTC are undetermined. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, damage to the device is possible.	A
VCC2	12	Short-Circuited to Pin1 (N/A)	Not applicable (N/A) across the isolation barrier	N/A
VCC2	12	Short-Circuited to Supply (Side-2)	The device continues to function as expected. Normal operation.	D
VCC1	13	Short-Circuited to Ground (Side-1)	The device has no power on side-1 (the supply input is shorted to ground). The outputs of OUTA, OUTB, and OUTC are at the default logic state. The output state of OUTD is undetermined. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, damage to the device is possible. This short circuit potentially causes high current to flow between the two GND1 pins (pin4 and pin14); potentially damaging the device.	A
VCC1	13	Open-Circuited	The device has no power on side-1 (the supply input is open). The outputs of OUTA, OUTB, and OUTC are at the default logic state. The output state of OUTD is undetermined. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, damage to the device is possible.	A
VCC1	13	Short-Circuited to Pin14 (GND1)	The device has no power on side-1 (the supply input is shorted to ground). The outputs of OUTA, OUTB, and OUTC are at the default logic state. The output state of OUTD is undetermined. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, damage to the device is possible. This short circuit potentially causes high current to flow between the two GND1 pins (pin4 and pin14); potentially damaging the device.	A
VCC1	13	Short-Circuited to Supply (Side-1)	The device continues to function as expected. Normal operation.	D
GND1	14	Short-Circuited to Ground (Side-1)	The device continues to function as expected. Normal operation.	D
GND1	14	Open-Circuited	The device receives return ground through pin 4 (GND1). Normal operation.	D
GND1	14	Short-Circuited to Pin15 (INA)	The input signal is shorted to ground, so the output of OUTA is stuck low. Communication through channel A is corrupted.	B

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground, Open-Circuited, Short-Circuited to Adjacent Pin, and Short-Circuited to Supply (continued)

Pin Name	Pin Number	Potential Failure Mode	Description of Potential Failure Effects	Failure Effect Class
GND1	14	Short-Circuited to Supply (Side-1)	The device has no power on side-1 (the supply input is shorted to ground). The outputs of OUTA, OUTB, and OUTC are at the default logic state. The output state of OUTD is undetermined. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, damage to the device is possible. This short circuit potentially causes high current to flow between the two GND1 pins (pin4 and pin14); potentially damaging device.	A
INA	15	Short-Circuited to Ground (Side-1)	The input signal is shorted to ground, so the output of OUTA is stuck low. Communication through channel A is corrupted.	B
INA	15	Open-Circuited	Communication through channel A is not possible. The output of OUTA is at the default state (weak internal pullup or pulldown to the default state).	B
INA	15	Short-Circuited to Pin16 (INB)	Communication is corrupted for either channel or both channels.	B
INA	15	Short-Circuited to Supply (Side-1)	The input signal is shorted to supply, so the output of OUTA is stuck high. Communication through channel A is corrupted.	B
INB	16	Short-Circuited to Ground (Side-1)	The input signal is shorted to ground, so the output of OUTB is stuck low. Communication through channel B is corrupted.	B
INB	16	Open-Circuited	Communication through channel B is not possible. The output of OUTB is at the default state (weak internal pullup or pulldown to the default state).	B
INB	16	Short-Circuited to Pin1 (INC)	Not applicable (N/A), corner pin.	N/A
INB	16	Short-Circuited to Supply (Side-1)	The input signal is shorted to supply, so the output of OUTB is stuck high. Communication through channel B is corrupted.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2026	*	Initial Release

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