*Application Note*

# *MSPM0 L-Series MCUs Hardware Development Guide*


**ABSTRACT**

The MSPM0 L-series microcontroller (MCU) portfolio offers a wide variety of 32-bit MCUs with ultra-low-power and integrated analog and digital peripherals for sensing, measurement and control applications. This application note covers information needed for hardware development with MSPM0 L-series MCUs, including detailed hardware design information for power supplies, reset circuitry, clocks, debugger connections, key analog peripherals, communication interfaces, GPIOs, and board layout guidance.


## Table of Contents

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# 1 MSPM0L Hardware Design Checklist

Table 1-1 describes the main signal that needs to be checked during the MSPM0L hardware design process. The following sections give more details.

**Table 1-1. MSPM0L Hardware Design Check List**

| Pin (1) | Description | Requirements |
|---|---|---|
| VDD | Power supply positive pin | Place 10µF and 100nF capacitors between VDD and VSS, and keep those part close to VDD and VSS. |
| VSS | Power supply negative pin | |
| VCORE | Core voltage (typical: 1.35V) | Connect a 470nF capacitor to VSS, do not supply any voltage or apply any external load to the VCORE pin. |
| NRST | Reset pin | Connect an external 47kΩ pullup resistor with a 10nF pulldown capacitor. |
| ROSC | External reference resistor pin | • Connect an external 100kΩ ±0.1% 25-ppm resistor to VSS to enable high SYSOSC accuracy if needed.<br>• Keep open is OK if does not have high accuracy requirement for SYSOSC. |
| VREF+ | Voltage reference power supply for external reference input | • When using VREF+ and VREF- to bring in an external voltage reference for analog peripherals such as the ADC, a decoupling capacitor must be placed on VREF+ to VREF-/GND with a capacitance based on the external reference source.<br>• Keeping this open is permitted if external voltage reference is not used. |
| VREF- | Voltage reference ground supply for external reference input | |
| SWCLK | Serial wire clock from debug probe | Internal pulldown to VDD; does not require any external part. |
| SWDIO | Bidirectional (shared) serial wire data | Internal pullup to VSS; does not require any external part. |
| PA0, PA1 | Open-drain I/O | Pull-up resistor required for output high |
| PA18 | Default BSL invoke pin | Keep pulled down to avoid entering BSL mode after reset. The BSL invoke pin can be remapped. |
| PAx (exclude PA0, PA1) | General-purpose I/O | Set corresponding pin functions to GPIO (PINCMx.PF = 0x1) and configure unused pins to output low or input with internal pullup or pulldown resistor. |
| OPAx_IN0-(2) | OPAx inverting terminal input 0 | This pin is high-impedance; does not need any external part if unused. |

(1) For any unused pin with a function that is shared with general-purpose I/O, follow the "PAx" unused pin connection guidelines.
(2) MSPM0L134x only

TI recommends connecting a combination of a 10µF and a 0.1nF low-ESR ceramic decoupling capacitor to the VDD and VSS pins . Higher-value capacitors can be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimeters).

The NRST reset pin is required to connect an external 47kΩ pullup resistor with a 10nF pulldown capacitor.

The SYSOSC frequency correction loop (FCL) circuit utilizes an external 100kΩ resistor, populated between the ROSC pin and VSS, to stabilize the SYSOSC frequency by providing a precision reference current for the SYSOSC. This resistor is not required if the SYSOSC FCL is not enabled.

A 0.47µF tank capacitor is required for the VCORE pin and must be placed close to the device with minimum distance to the device ground.

For 5V-tolerant open drain (ODIO), a pullup resistor is required to output high, this is required for I2C and UART functions if the ODIO are used.

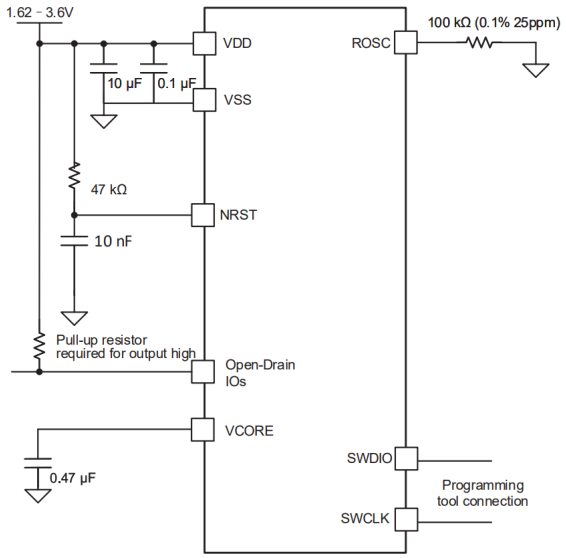


**Figure 1-1. MSPM0L Typical Application Schematic**

# 2 Power Supplies in MSPM0L Devices

Power is supplied to the device through the VDD and VSS connections. The device supports operation with a supply voltage of 1.62V to 3.6V and can start with a 1.62V supply. The power management unit (PMU) generates the regulated core supplies for the device and provides supervision of the external supply. This also contains a bandgap voltage reference used by the PMU and other analog peripherals. VDD is used directly to provide the IO supply (VDDIO) and the analog supply (VDDA). VDDIO and VDDA are internally connected to VDD so that additional power supply pins are not required (see the device-specific data sheet for details).

## 2.1 Digital Power Supply

### VCORE Regulator

There is an internal low-dropout linear voltage regulator to generate a 1.35-V supply rail to power the device core. In general, the core regulator output (VCORE) supplies power to the core logic, which includes the CPU, digital peripherals and the device memory. The core regulator requires an external capacitor (CVCORE) which is connected between the device VCORE pin and VSS (ground) (see Figure 2-1). See the device-specific data sheet for the correct value and tolerance of CVCORE. CVCORE should be placed close to the VCORE pin.

The core regulator is active in all power modes except for SHUTDOWN. In all other power modes (RUN, SLEEP, STOP, and STANDBY) the drive strength of the regulator is configured automatically to support the max load current of each mode. This reduces the quiescent current of the regulator when using low power modes, improving low power performance.

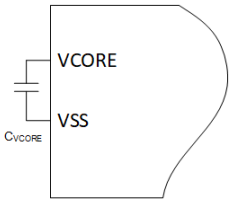


**Figure 2-1. VCORE Regulator Circuit**

## 2.2 Analog Power Supply

### Analog Mux VBOOST

The VBOOST circuit in the PMU generates an internal VBOOST supply which is used by the analog muxes in COMP, GPAMP, and OPA, if present on a device. The VBOOST circuit enables consistent analog mux performance across the external supply voltage (VDD) range.

### Enabling and Disabling VBOOST

SYSCTL automatically manages the enable request for the VBOOST circuit based on the following parameters:

1. The COMP, OPA, and GPAMP peripheral PWREN settings
2. The MODE setting of any COMP which is enabled (FAST vs. ULP mode).
3. The ANACPUMPCFG control bits in the GENCLKCFG register in SYSCTL.

VBOOST is disabled by default following a SYSRST. It is not necessary for application software to enable the VBOOST circuit before using the COMP, OPA, or GPAMP. When a COMP, OPA, or the GPAMP is enabled by application software, SYSCTL also enables the VBOOST circuit to support the analog peripheral.

The VBOOST circuit has a startup time requirement (12µs typical) to transition from a disabled state to an enabled state. In the event that the startup time of the COMP, OPA, or GPAMP is less than the VBOOST startup time, the peripheral startup time is extended to account for the VBOOST startup time.

### Bandgap Reference

The PMU provides a temperature and supply voltage stable bandgap voltage reference which is used by the device for internal functions, including:

- Driving the brownout reset circuit thresholds.
- Setting the output voltage for the core regulator.
- Driving the on-chip VREF levels for on-chip analog peripherals.

The bandgap reference is enabled in RUN, SLEEP, and STOP modes. It operates in a sampled mode in STANDBY to reduce power consumption. It is disabled in SHUTDOWN mode. SYSCTL manages the bandgap state automatically; no user configuration is required.

## 2.3 Built-in Power Supply and Voltage Reference

The VREF module for the MSPM0 L family is a shared voltage reference module which can be leveraged by a variety on on-board analog peripherals.

The VREF module features include:

- 1.4V and 2.5V user-selectable internal references.
- Support for receiving external reference on VREF+ and VREF- device pins.
- Sample and hold mode support VREF operation down to STANDBY operating mode.
- Internal reference supports for ADC, COMP, OPA.

When supplying the MCU with an external reference, connect a decoupling capacitor on the reference pins with a value based on the voltage source (see Figure 2-2).

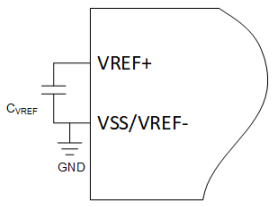


**Figure 2-2. VREF Circuit**

### 2.4 Recommended Decoupling Circuit for Power Supply

TI recommends connecting a combination of a 10µF plus a 100nF low-ESR ceramic decoupling capacitor to the DVCC pin (see Figure 2-3). Higher-value capacitors can be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that the pins decouple (within a few millimeters).

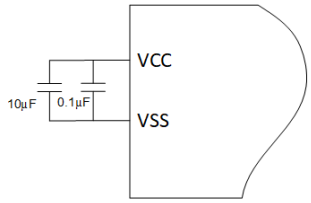


**Figure 2-3. Power Supply Decoupling Circuit**

## 3 Reset and Power Supply Supervisor

### 3.1 Digital Power Supply

The device has five reset levels:

- Power-on reset (POR)
- Brown-out reset (BOR)
- Boot reset (BOOTRST)
- System reset (SYSRST)
- CPU reset (CPURST)

The details of the relationships between reset levels is described in the MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual.

After a cold start, the NRST pin is configured in NRST mode. The NRST pin must be high for the device to boot successfully. There is no internal pullup resistor on NRST. External circuitry (either a pullup resistor to DVCC or a reset control circuit) must actively pull NRST high for the device to start. A capacitor and an open button are needed for manual reset (see Figure 3-1). After the device is started, a low pulse on NRST that is <1 second in duration triggers a BOOTRST. If a low pulse on NRST is held for >1 second, a POR is triggered.

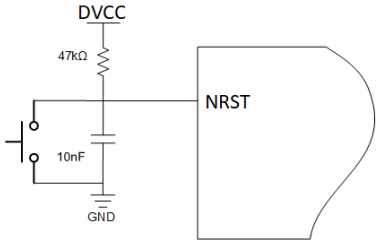


**Figure 3-1. NRST Recommended Circuit**

## 3.2 Power Supply Supervisor

### Power-On Reset (POR) Monitor

The power-on reset (POR) monitor supervises the external supply (VDD) and asserts or de-asserts a POR violation to SYSCTL. During cold power-up, the device is held in a POR state until VDD passes the POR+. Once VDD has passed POR+, the POR state is released and the bandgap reference and BOR monitor circuit are started. If VDD drops below the POR- level, then a POR- violation is asserted and the device is again held in a POR reset state.

The POR monitor does not indicate that VDD has reached a level high enough to support correct operation of the device. Rather, this is the first step in the boot process and is used to determine if the supply voltage is sufficient to power up the bandgap reference and BOR circuit, which are then used to determine if the supply has reached a level sufficient to for the device to run correctly. The POR monitor is active in all power modes including SHUTDOWN, and cannot be disabled. (The POR triggered waveform is shown in Figure 3-2).

### Brownout Reset (BOR) Monitor

The brown-out reset (BOR) monitor supervises the external supply (VDD) and asserts or de-asserts a BOR violation to SYSCTL. The primary responsibility of the BOR circuit is to verify that the external supply is maintained high enough to enable correct operation of internal circuits, including the core regulator. The BOR threshold reference is derived from the internal bandgap circuit. The threshold is programmable and is always higher than the POR threshold. During cold start, after VDD passes the POR+ threshold the bandgap reference and BOR circuit are started. The device is then held in a BOR state until VDD passes the BOR0+ threshold. Once VDD passes BOR0+, the BOR monitor releases the device to continue the boot process, and the PMU is started. (The BOR triggered waveform is shown in Figure 3-2).

### POR and BOR Behavior During Supply Changes

When the supply voltage (VDD) drops below POR-, the entire device state is cleared. Small variations in VDD which do not pass below the BOR0- threshold do not cause a BOR- violation, and the device continues to run. The BOR circuit is configured to generate an interrupt rather than immediately triggering a BOR reset.

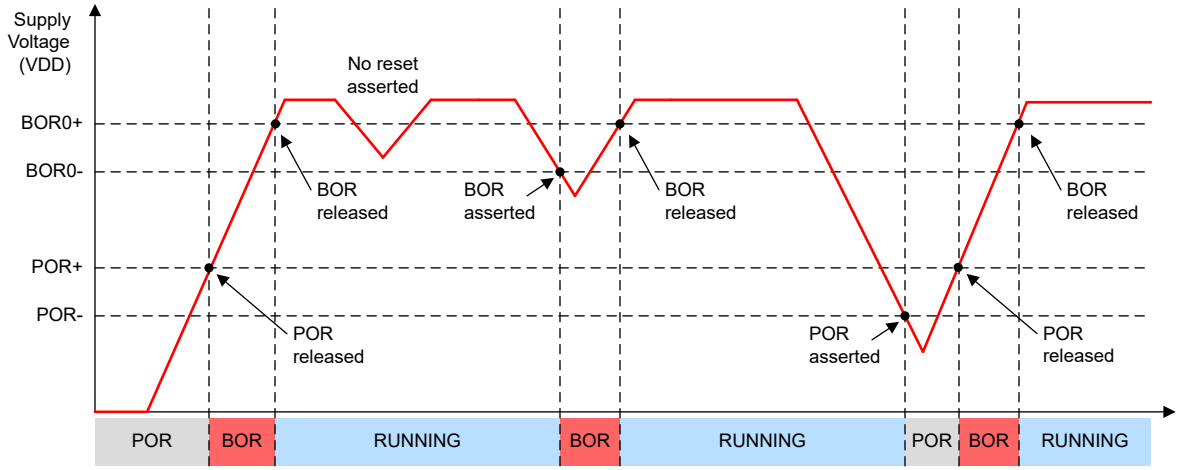


**Figure 3-2. POR/BOR vs. Supply Voltage (VDD)**

# 4 Clock System

The clock system of MSPM0L series contains the internal oscillators, the clock monitors, and the clock selection and control logic. This section describes the clock resources on different MSPM0L family devices and the interaction with external signals or devices.

## 4.1 Internal Oscillators

### Internal Low-Frequency Oscillator (LFOSC)

LFOSC is an on-chip low power oscillator that is factory trimmed to a frequency of 32.768kHz. This provides a low-frequency clock that can be used to help the system achieve low-power. LFOSC can provide higher accuracy when used over a reduced temperature range. See the device-specific data sheet for details.

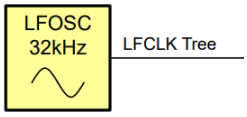


**Figure 4-1. MSPM0L Series LFOSC**

### Internal System Oscillator (SYSOSC)

SYSOSC is an on-chip, accurate, and configurable oscillator with factory-trimmed frequencies of 32MHz (base frequency) and 4 MHz (low frequency), as well as support for user-trimmed operation at either 24MHz or 16MHz. This provides a high-frequency clock that lets the CPU run at high speed for executing code and processing performance.

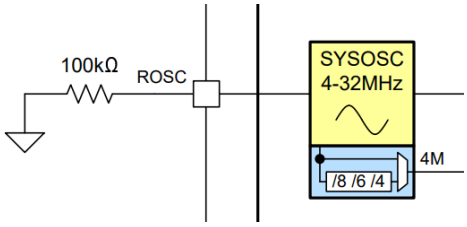


**Figure 4-2. MSPM0L Series SYSOSC**

### SYSOSC Frequency Correction Loop

The additional hardware setting for this oscillator is an external resistor, populated between the ROSC pin and VSS, to increase SYSOSC from a base accuracy of ±2.5% across temperature.

The overall SYSOSC application accuracy is determined by combining the following error sources to determine the total error:

1. The ROSC reference resistor error (due to tolerance and temperature drift)
2. The SYSOSC circuit error in FCL mode (±0.75% for -40°C to 85°C or ±0.90% for -40°C to 125°C)

Table 4-1 shows how to calculate the SYSOSC application accuracy for two different ROSC resistor specs across two temperature ranges. For more details, refer to the MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual.

**Table 4-1. SYSOSC Accuracy With FCL, by ROSC Tolerance, RSOC TCR, and Ambient Temperature ($T_A$)**

| Ambient Temperature ($T_A$) | -40 ≤ $T_A$ ≤ 125°C | | -40 ≤ $T_A$ ≤ 85°C | |
|---|---|---|---|---|
| **ROSC Resistor Parameters** | **±0.1% 25 ppm/°C** | **±0.5% 25 ppm/°C** | **±0.1% 25 ppm/°C** | **±0.5% 25 ppm/°C** |
| Nominal ROSC resistance ($ROSC_{nom}$) | 100 kΩ | | | |
| Maximum ROSC resistance (at 25°C) | 100.1 kΩ | 100.5 kΩ | 100.1 kΩ | 100.5 kΩ |
| Minimum ROSC resistance (at 25°C) | 99.9 kΩ | 99.5 kΩ | 99.9 kΩ | 99.5 kΩ |

**Table 4-1. SYSOSC Accuracy With FCL, by ROSC Tolerance, RSOC TCR, and Ambient Temperature ($T_A$) (continued)**

| Ambient Temperature ($T_A$) | -40 ≤ $T_A$ ≤ 125°C | | -40 ≤ $T_A$ ≤ 85°C | |
|---|---|---|---|---|
| **ROSC Resistor Parameters** | **±0.1% 25 ppm/°C** | **±0.5% 25 ppm/°C** | **±0.1% 25 ppm/°C** | **±0.5% 25 ppm/°C** |
| ROSC resistor TCR | 25 ppm/°C | | | |
| ROSC temperature drift | -0.16% to 0.25% | | -0.16% to 0.15% | |
| Maximum ROSC resistance (at high temperature) ($ROSC_{max}$) | 100.35 kΩ | 100.75 kΩ | 100.25 kΩ | 100.65 kΩ |
| Minimum ROSC resistance (at low temperature) ($ROSC_{min}$) | 99.74 kΩ | 99.34 kΩ | 99.74 kΩ | 99.34 kΩ |
| ROSC resistance error (high temperature) ($ROSC_{err+}$) | +0.35% | +0.75% | + 0.25% | +0.65% |
| ROSC resistance error (low temperature) ($ROSC_{err-}$) | -0.26% | -0.66% | -0.26% | -0.66% |
| SYSOSC circuit error ($SYSOSC_{err}$) | ±0.9% | | ±0.75% | |
| Total accuracy ($TOT_{err-}$, $TOT_{err+}$) | -1.2% to +1.3% | -1.6% to +1.7% | -1.0% to +1.0% | -1.4% to +1.4% |

## 4.2 External Clock Output (CLK_OUT)

A clock output unit is provided for pushing out digital clocks from the device to external circuits or to the frequency clock counter. This feature is useful for clocking external circuitry such as an external ADC that does not have a clock source. The clock output unit has a flexible set of sources to select from and includes a programmable divider.

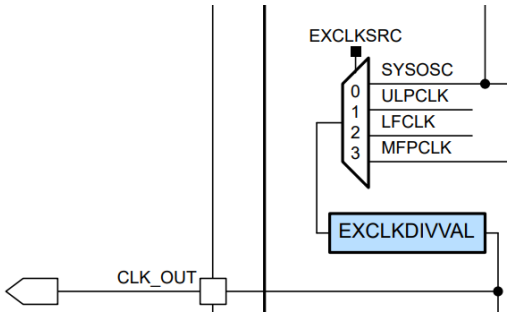


**Figure 4-3. MSPM0L Series External Clock Output**

Available clock sources for CLK_OUT:

- SYSOSC
- ULPCLK
- MFCLK
- LFCLK

The selected clock source is divided by 1, 2, 4, 8, 16, 32, 64, or 128 before being output to the pin or to the frequency clock counter.

## 4.3 Frequency Clock Counter (FCC)

The frequency clock counter (FCC) enables flexible in-system testing and calibration of a variety of oscillators and clocks on the device. The FCC counts the number of clock periods seen on the selected source clock within a known fixed trigger period (derived from a secondary reference source) to provide an estimation of the frequency of the source clock.

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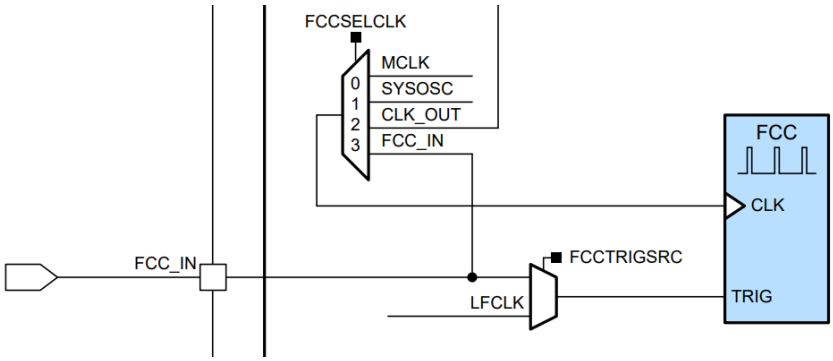


**Figure 4-4. MSPM0L Series Frequency Clock Counter Block Diagram**

Application software can use the FCC to measure the frequency of the following oscillators and clocks:

- MCLK
- SYSOSC
- CLK_OUT
- The external FCC input (FCC_IN)

**Note**

While the external FCC input (FCC_IN function) can be used as either the FCC clock source or the FCC trigger input, the input cannot be used for both functions during the same FCC capture. It must be configured as either the FCC clock source or the FCC trigger.

# 5 Debugger

The debug sub system (DEBUGSS) interfaces the serial wire debug (SWD) two-wire physical interface to multiple debug functions within the device. MSPM0L devices support debugging of processor execution, the device state, and the power state (using EnergyTrace technology).

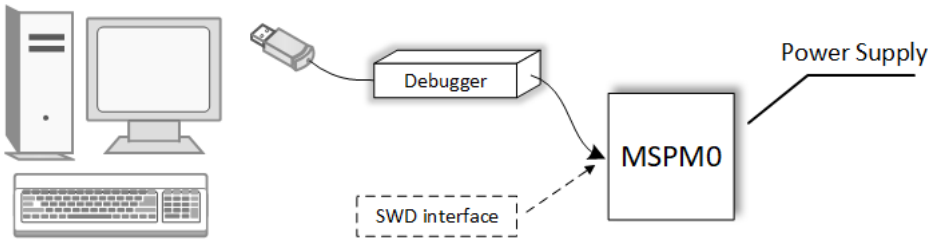


**Figure 5-1. Host to Target Device Connection**

## 5.1 Debug Port Pins and Pinout

The debug port contains SWCLK and SWDIO (see Table 5-1) which have internal pull-down and pull-up resistors (see Figure 5-2). The MSPM0L MCU family is offered in various packages with different numbers of available pins. Refer to the device-specific data sheet for details.

**Table 5-1. MSPM0L Debug Ports**

| Device Signal | Direction | SWD Function |
|---|---|---|
| SWCLK | Input | Serial wire clock from debug probe |
| SWDIO | Input/Output | Bi-directional (shared) serial wire data |

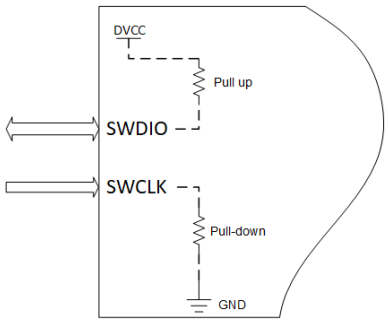


**Figure 5-2. MSPM0L SWD Internal Pull**

## 5.2 Debug Port Connection With Standard JTAG Connector

Figure 5-3 shows the connection between MSPM0L family MCU SWD debug port with the standard JTAG connector.

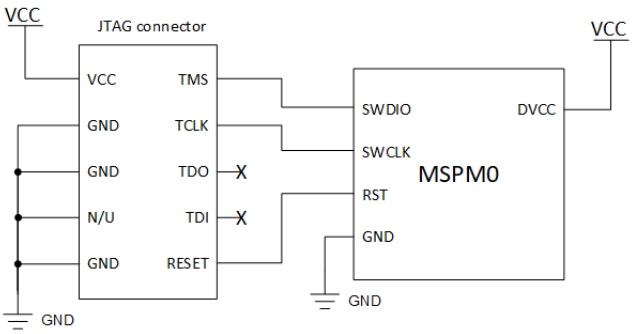


**Figure 5-3. JTAG and MSPM0L Connection**

For MSPM0L device, use XDS110 to implement debug/download function. Here, list the contents of the XDS110 and provides instruction on installing the hardware.

**Standard XDS110**

Purchase a standard XDS110 on ti.com. Figure 5-4 shows a high-level diagram of the major functional areas and interfaces of the XDS110 probe.

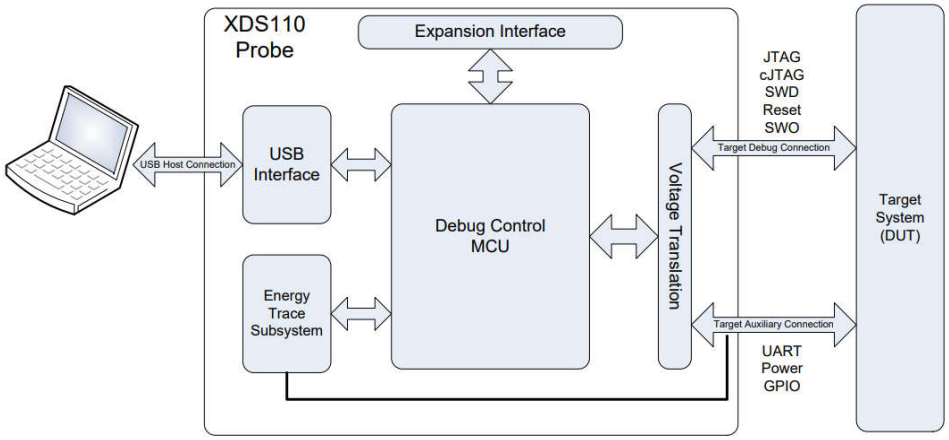


**Figure 5-4. XDS110 Probe High-Level Block Diagram**

More standard XDS110 information, see the XDS110 Debug Probe User's Guide.

**Lite XDS110 (MSPM0 LaunchPad™ kit)**

The MSPM0 LaunchPad kit include the XDS110-ET (Lite) circuit. Use this debugger to download the firmware into MSPM0 device. Figure 5-5 shows the XDS110-ET circuit.

There are two probes in XDS110-ET:

**2.54mm probe:** This port supports the SWD protocol and includes a 5V or 3.3V power supply. Connect the SWDIO SWCLK 3V3 GND to the board and download firmware into the MSPM0L device.

This probe supports EnergyTrace™ technology so a user can use this circuit to measure power consumption precisely in real time.

More information on EnergyTrace technology, visit the EnergyTrace Technology tool page.

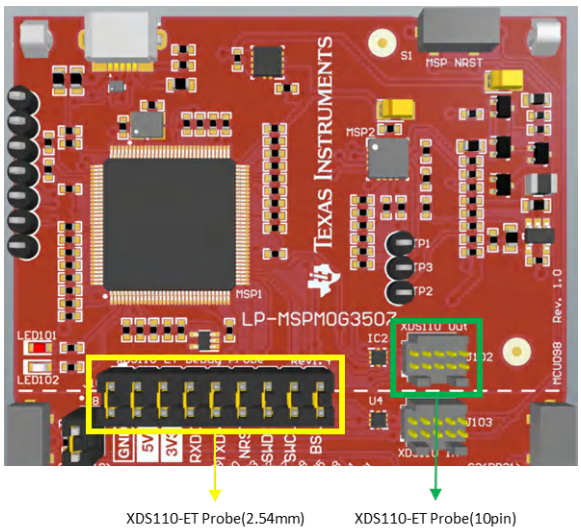


**Figure 5-5. XDS110-ET Circuit**

**10-pin probe:** This port supports the JTAG and SWD protocols and include a 3.3V power supply. Use the 10-pin cable to connect the board and XDS110-ET and download firmware into the MSPM0L device. Figure 5-6 show the 10-pin cable.

**Figure 5-6. Arm Standard 10-Pin Cable**

**Note**

- Standard XDS110 support level shift for debug ports, XDS110-ET just support 3.3V probe level.
- TI does not recommend using the XDS110 to power other devices except the MSPM0L MCU. The XDS110 integrates an LDO with limited current drive capability.
- XDS110-ET 2.54mm probe does not support the JTAG protocol.
- XDS110-ET 10-pin probe does not support EnergyTrace technology.

# 6 Key Analog Peripherals

The MSPM0L series MCU includes a wealth of analog peripheral resources, which can provide many analog signal conditioning functions inside the chip. To maximize the use of the MSPM0L analog peripheral performance, some considerations need to be made in the hardware design. This section discusses analog design considerations for many typical analog circuit configurations.

## 6.1 ADC Design Considerations

MSPM0L devices have a 12-bit, up to 1-Msps, analog-to-digital converter (ADC). The ADC supports fast 12-, 10-, and 8-bit analog-to-digital conversions. The ADC implements a 12-bit SAR core, sample/conversion mode control, and up to 4 independent conversion-and-control buffers.

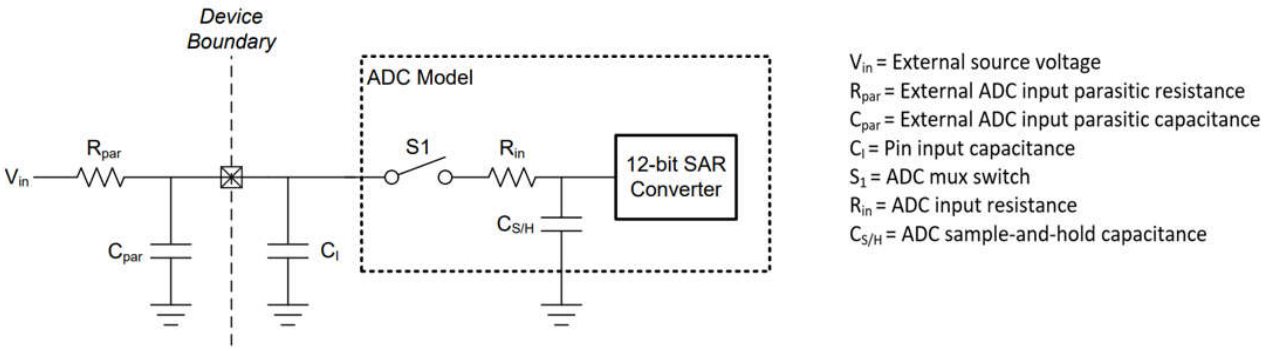


**Figure 6-1. ADC Input Network**

To achieve the desired conversion speed and keep high accuracy, set the proper sampling time in the hardware design. Sampling (sample-and-hold) time determines how long to sample a signal before digital conversion. During sample time, an internal switch lets the input capacitor charge. The required time to fully charge the capacitor is dependent on the external analog front-end (AFE) connected to the ADC input pin. Figure 6-1 shows a typical ADC model of an MSPM0L MCU. The $R_{in}$ and $C_{S/H}$ values can be obtained from the device-specific data sheet. It is critical to understand the AFE drive capability and calculate the minimum sampling time required to sample the signal. The resistance of $R_{Par}$ and $R_{in}$ affects $t_{sample}$. Equation 1 can be used to calculate a conservative value of the minimum sample time tsample for an n-bit conversion:

$$t_{sample} \geq (R_{par} + R_{in}) \times \ln(2^{n+2}) \times (C_{S/H} + C_1 + C_{Par}) \quad (1)$$

## 6.2 OPA Design Considerations

The MSPM0L OPA is a zero-drift chopper stabilized operational amplifier with a programmable gain stage. This can used for signal amplification and buffering. The OPA can work in General-purpose Mode, Buffer Mode and PGA mode.

When using the OPA in general-purpose mode, add an external resistor and capacitor to create the amplifier circuit. But when using buffer mode, the circuit can be configured in software. For PGA mode, software can configure up to 32x PGA gain.

**Note**

The PGA gain is only in the negative terminal.

When two or more OPAs are available on a device, the two can be combined to form a differential amplifier. The output equation for the differential amplifier is given by the Vdiff equation in Figure 6-2.

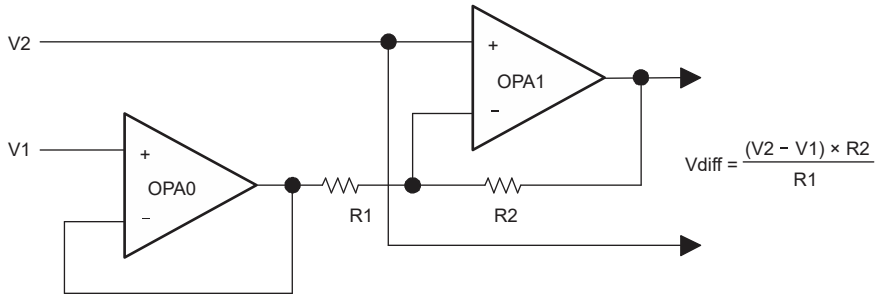


**Figure 6-2. Two OPA Differential Amplifier Block Diagram and Equation**

Alternately, when two or more OPAs are available on a device, the OPAs can be combined to form a multi-stage or cascaded amplifier. Using the programmable input muxes, all combinations of inverting and noninverting multi-stage amplifiers can be implemented. The output equation for the noninverting to noninverting cascaded amplifier is given by the Vout equation in Figure 6-3.

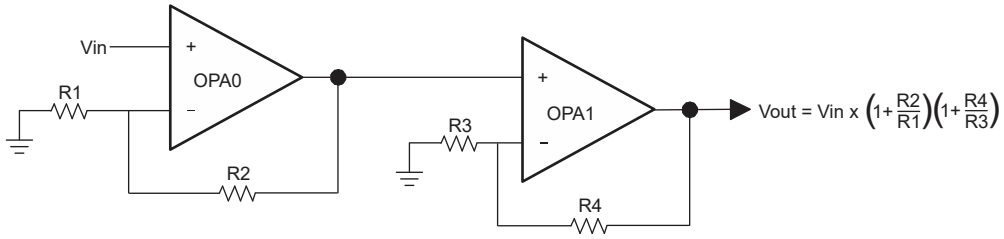


**Figure 6-3. Two OPA Noninverting to Noninverting Cascade Amplifier Block Diagram and Equation**

## 6.3 DAC Design Considerations

MSPM0L devices include 8-bit DAC modules. The DAC can be used as the reference voltage (Figure 6-4) and also can work with the OPA to drive the output pad directly (Figure 6-5). The 8-bit DAC module is typically used as internal reference voltage for OPA and COMP. To output to an external pad, the OPA must be configured into buffer mode to improve the drive strength.

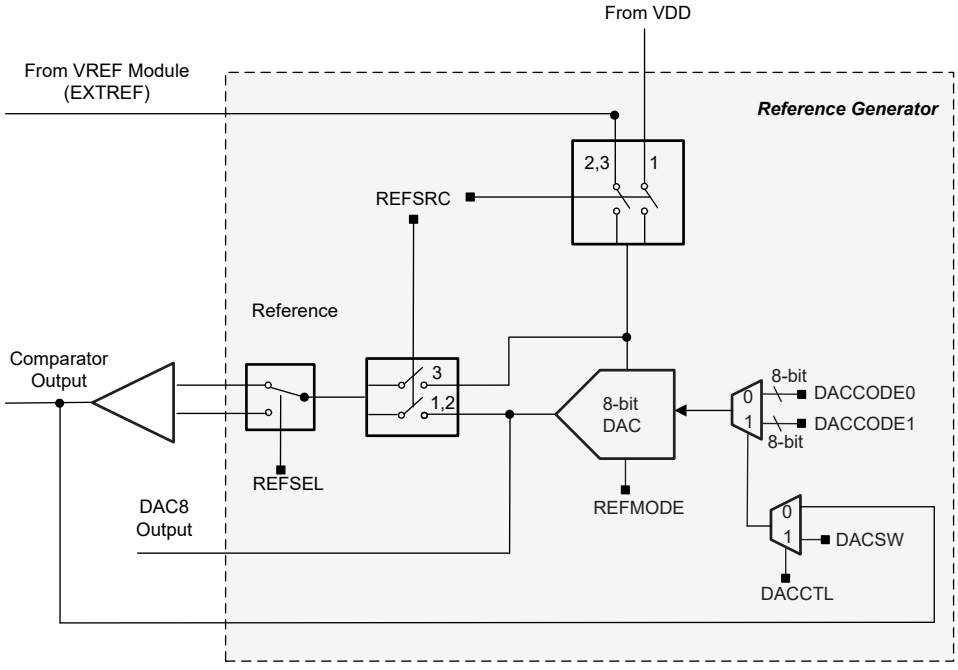


**Figure 6-4. 8-Bit DAC Block Diagram**

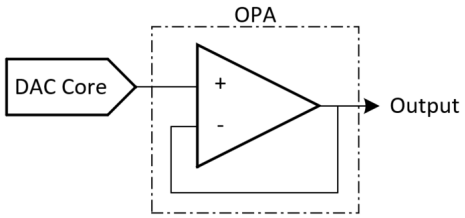


**Figure 6-5. 8-Bit DAC + OPA Output Connections**

## 6.4 COMP Design Considerations

MSPM0L comparator module (COMP) is an analog voltage comparator with general comparator functionality.

The MSPM0L Comparator module include internal and external input, you can use these structures flexibly to process the analog signals. The internal temperature sensor must be able to as the COMP input directly.

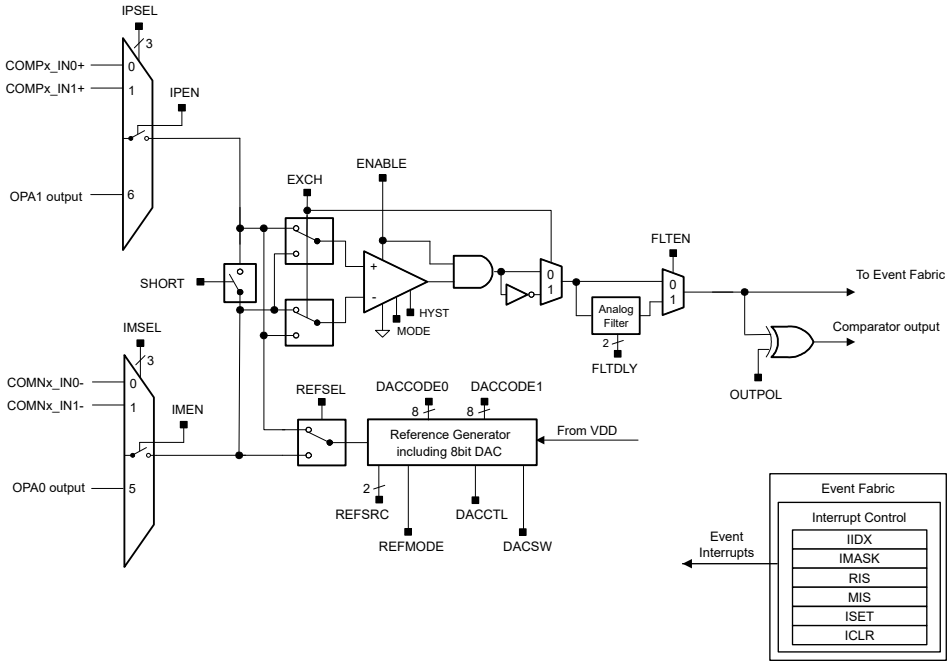


**Figure 6-6. Comparator Block Diagram**

The MSPM0L Comparator module also include a SHORT switch which can be used to build a simple sample-and-hold for the comparator.

As shown in Figure 6-7, the required sampling time is proportional to the size of the sampling capacitor (CS), the resistance of the input switches in series with the short switch (R), and the resistance of the external source (RS). The sampling capacitor CS must be greater than 100pF. The time constant, Tau, to charge the sampling capacitor CS can be calculated with Equation 2

$$T_{au} = (R_I + R_S)\text{x}C_S \quad (2)$$

Depending on the required accuracy, 3 to 10 Tau should be used as the sampling time. With 3 Tau the sampling capacitor is charged to approximately 95% of the input signals voltage level, with 5 Tau it is charged to more than 99%, and with 10 Tau the sampled voltage is sufficient for 12-bit accuracy.

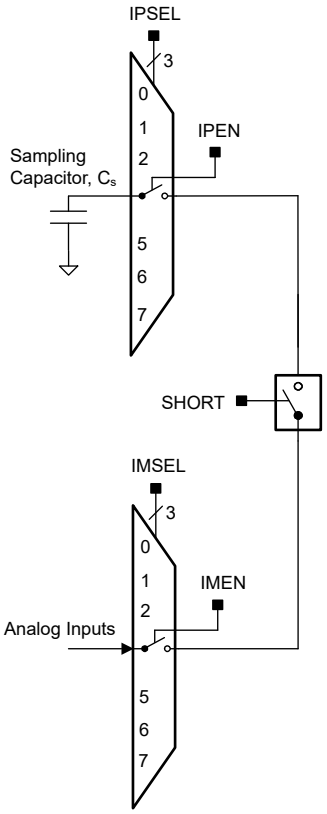


**Figure 6-7. Comparator Short Switch**

## 6.5 GPAMP Design Considerations

MSPM0L devices include GPAMP (General-Purpose Amplifier) modules that can used for signal amplification with some external resistors and capacitors, as seen in Figure 6-8.

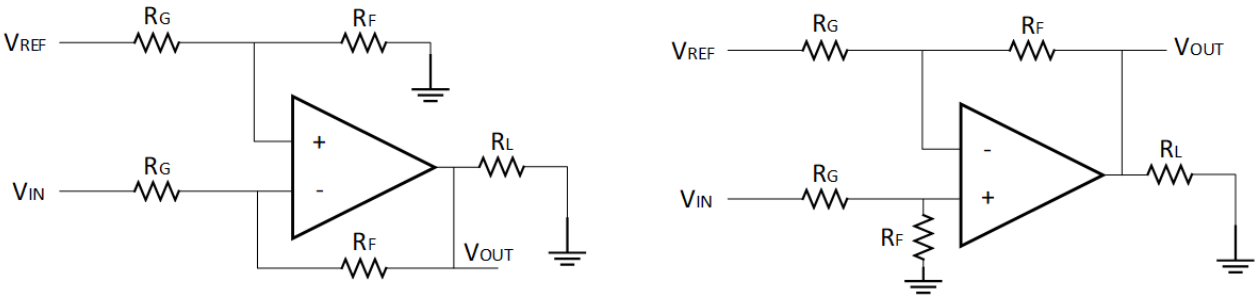


**Figure 6-8. GPAMP Circuit in Amplify Mode**

The GPAMP can also be used as a buffer for the internal ADC. Figure 6-9 shows an example of this configuration.

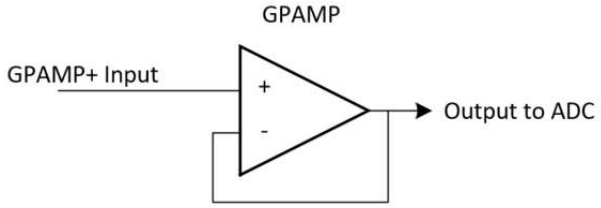


**Figure 6-9. GPAMP Circuit in Buffer Mode**

## 6.6 LCD Design Considerations

The Liquid Crystal Display (LCD) controller on MSPM0L directly drives LCD displays through segment (SEG) and COM voltage signals. This controller can support static and 2-mux to 8-mux mode LCD segment displays.

This section only discusses the key considerations on schematic and PCB design. For more instruction on the LCD design, see Designing With MSPM0™ MCUs and Segment LCDs.

For the schematic design, the LCD controller can directly drive the LCD without requiring additional components in common use cases. However, when utilizing a charge pump to generate a constant voltage (especially if VDD is battery-powered to prevent display fluctuations caused by VDD voltage variations), capacitors at LCDCAP0/1 and resistors R13, R24, R23, R33 can be required, as shown in Figure 6-10.

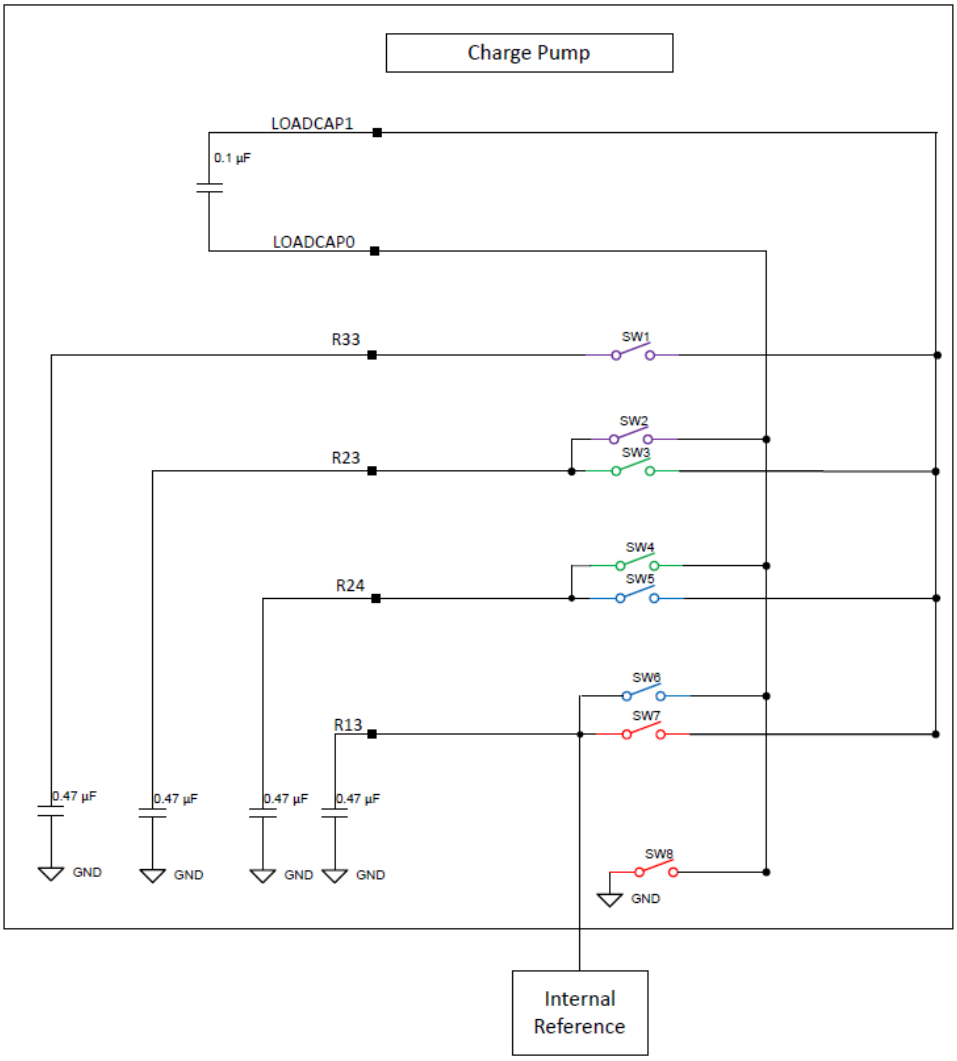


**Figure 6-10. LCD Capacitor Setting When using Charge Pump**

For the PCB design, here are the general layout rules:

LCD signal lines are constantly switching to keep the image on the display, keep them away from noise-sensitive lines (such as the external crystal connections). Use guard rings to shield noise-sensitive lines, such as the crystal connections or ADC inputs, from noise coupling. A ground plane underneath the LCD traces and guard traces also provide shielding. One good practice is to keep all LCD signal traces (segment and common lines) together, similar to a data bus. Keeping the LCD layout in a single layer is helpful so that there are not LCD traces running over or under potentially sensitive traces. Keep the charge pump capacitor on the LOADCAP pin as close as possible to the MCU with a short trace.

# 7 Key Digital Peripherals

The MSPM0 L series MCU includes digital peripheral resources including the Timer, UART, SPI, and LIN, among others, that provide rich communication capabilities. To maximize the use of the MSPM0L digital peripherals, some considerations need to be made in the hardware design. This section discusses design considerations for many typical digital peripheral configurations.

## 7.1 Timer Resources and Design Considerations

Timers are one of the most basic and important modules in any MCU, and this resource is used in all applications. This can be used to process tasks regularly, delay, output PWM waveforms to drive o devices, detect the width and frequency of external pulses, simulate waveform outputs, and more.

The MSPM0 L series MCU includes general propose timer module: TIMG. That can be used for a variety of functions, including measuring the input signal edge and period (capture mode) or generating output waveforms (compare mode output) like PWM signals. A summary of the different features and configurations of each timer is shown in the Table 7-1.

**Table 7-1. TIMG Instance Configuration**

| Instance | Power Domain | Counter Resolution | Prescaler | Repeat Counter | CCP Channels | Phase Load | Shadow Load | Pipelined CC | Dead band | Fault Handler | QEI |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TIMG0 | PD0 | 16-bit | 8-bit | - | 2 | - | - | - | - | - | - |
| TIMG1 | PD0 | 16-bit | 8-bit | - | 2 | - | - | - | - | - | - |
| TIMG2 | PD0 | 16-bit | 8-bit | - | 2 | - | - | - | - | - | - |
| TIMG3 | PD0 | 16-bit | 8-bit | - | 2 | - | - | - | - | - | - |
| TIMG4 | PD0 | 16-bit | 8-bit | - | 2 | - | Yes | Yes | - | - | - |
| TIMG5 | PD0 | 16-bit | 8-bit | - | 2 | - | Yes | Yes | - | - | - |
| TIMG6 | PD1 | 16-bit | 8-bit | - | 2 | - | Yes | Yes | - | - | - |
| TIMG7 | PD1 | 16-bit | 8-bit | - | 2 | - | Yes | Yes | - | - | - |
| TIMG8 | PD0 | 16-bit | 8-bit | - | 2 | - | - | - | - | - | Yes |
| TIMG9 | PD0 | 16-bit | 8-bit | - | 2 | - | - | - | - | - | Yes |
| TIMG10 | PD1 | 16-bit | 8-bit | - | 2 | - | - | - | - | - | Yes |
| TIMG11 | PD1 | 16-bit | 8-bit | - | 2 | - | - | - | - | - | Yes |

- First look at the device specific data sheet to check which TIMG instances are available on the device
- Need to check what features are available for each TIMG instance in Technical Reference Manual

## 7.2 UART and LIN Resources and Design Considerations

The MSPM0 L series MCU includes Universal Asynchronous Receiver-Transmitter (UART). As seen in Table 7-2, UART0 supports LIN, DALI, IrDA, ISO7816 Manchester Coding function.

**Table 7-2. UART Features**

| UART Features | UART0 (Extend) | UART1 (Main) |
|---|---|---|
| Active in Stop and Standby Mode | Yes | Yes |
| Separate transmit and receive FIFOs | Yes | Yes |
| Support hardware flow control | Yes | Yes |
| Support 9-bit configuration | Yes | Yes |
| Support LIN mode | Yes | - |
| Support DALI | Yes | - |
| Support IrDA | Yes | - |
| Support ISO7816 Smart Card | Yes | - |
| Support Manchester coding | Yes | - |

**Table 7-3. MSPM0L UART Specifications**

| PARAMETERS | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{UART}$ | UART input clock frequency | | | | 32 | MHz |
| $f_{BITCLK}$ | BITCLK clock frequency(equals baud rate in MBaud) | | | | 4 | MHz |
| $t_{SP}$ | Pulse duration of spikes suppressed by input filter | AGFSELx = 0 | 5 | 5.5 | 32 | ns |
| | | AGFSELx = 1 | 8 | 15 | 55 | ns |
| | | AGFSELx = 2 | 18 | 38 | 115 | ns |
| | | AGFSELx = 3 | 30 | 74 | 165 | ns |

The MSPM0L UART module can support up to 4MHz baud date, this can support almost all UART applications.

Local Interconnect Network (LIN) is a commonly used low-speed network interface that consists of a commander node communicating with multiple remote responder nodes. Only a single wire is required for communication and is commonly included in the vehicle wiring harness.

The TLIN1021A-Q1 transmitter supports data rates up to 20kbps. The transceiver controls the state of the LIN bus through the TXD pin and reports the state of the bus on the open-drain RXD output pin. The device has a current-limited wave-shaping driver to reduce electromagnetic emissions (EME).

The TLIN1021A-Q1 is designed to support 12V applications with a wide input voltage operating range. The device supports low-power sleep mode, as well as wake-up from low-power mode through the wake over LIN, the WAKE pin, or the EN pin. The device allows for system-level reductions in battery current consumption by selectively enabling the various power supplies that can be present on a node through the TLIN1021A-Q1 INH output pin. Figure 7-1 shows a typical interface implemented using the TI TLIN1021A LIN transceiver.

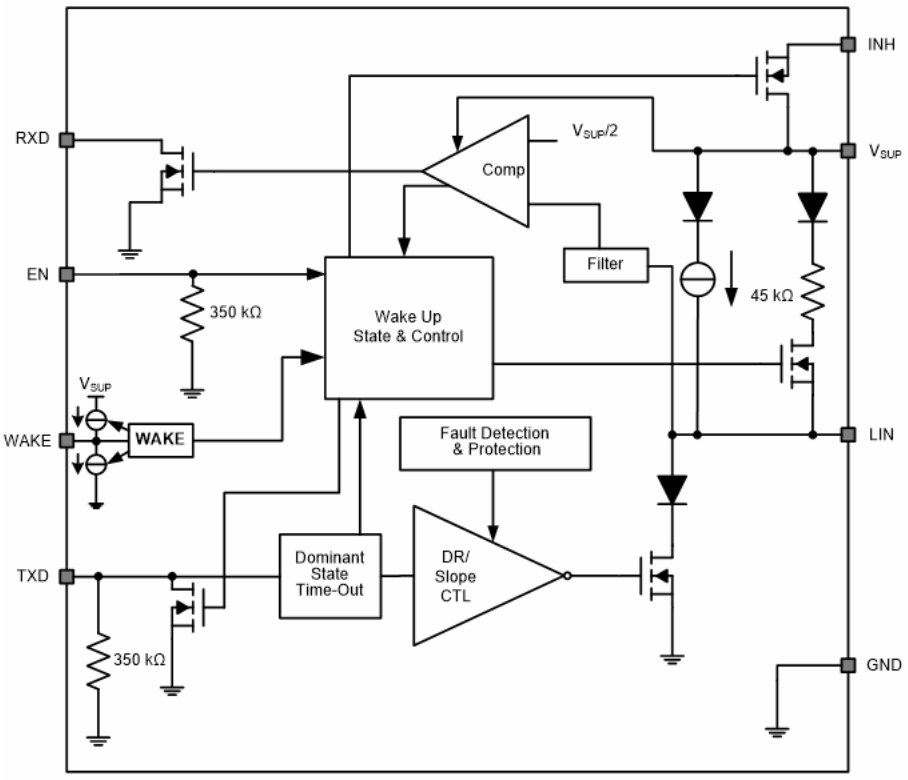


**Figure 7-1. Typical LIN TLIN1021A Transceiver**

Only a single wire is required for communication and is commonly included in the vehicle wiring harness. Figure 7-2 Figure 7-3 shows a typical interface implemented using the TI TLIN1021A LIN transceiver, for more details please refer to the TLIN1021 data sheet.

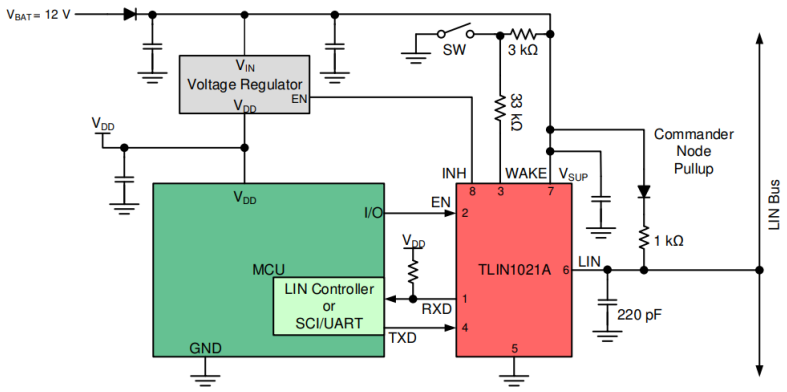


**Figure 7-2. Typical LIN Application(Commander) with MSPM0L**

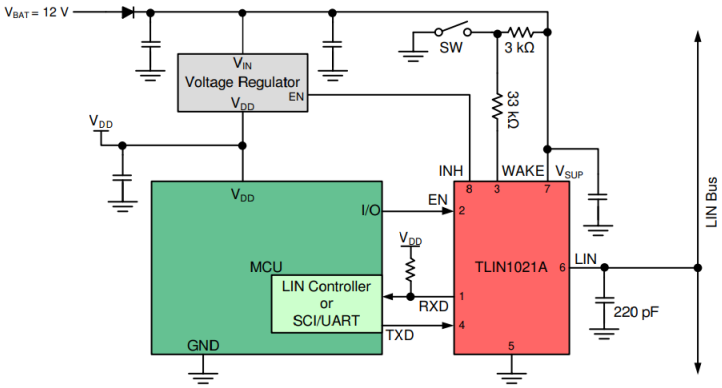


**Figure 7-3. Typical LIN Application(Responder) with MSPM0L**

## 7.3 I2C and SPI Design Considerations

SPI and I2C protocols are widely used in communication between devices or boards, such as data exchange between an MCU and a sensor. The MSPM0L series MCU includes up to 16MHz high-speed SPI and supports 3-wire, 4-wire, chip select, and command mode. See Figure 7-4 to design a system based on the requirements.

Some SPI peripheral devices require PICO (Peripherals Input Controller Output) keep high logic. In this case, add a pullup resistor to the PICO pin.

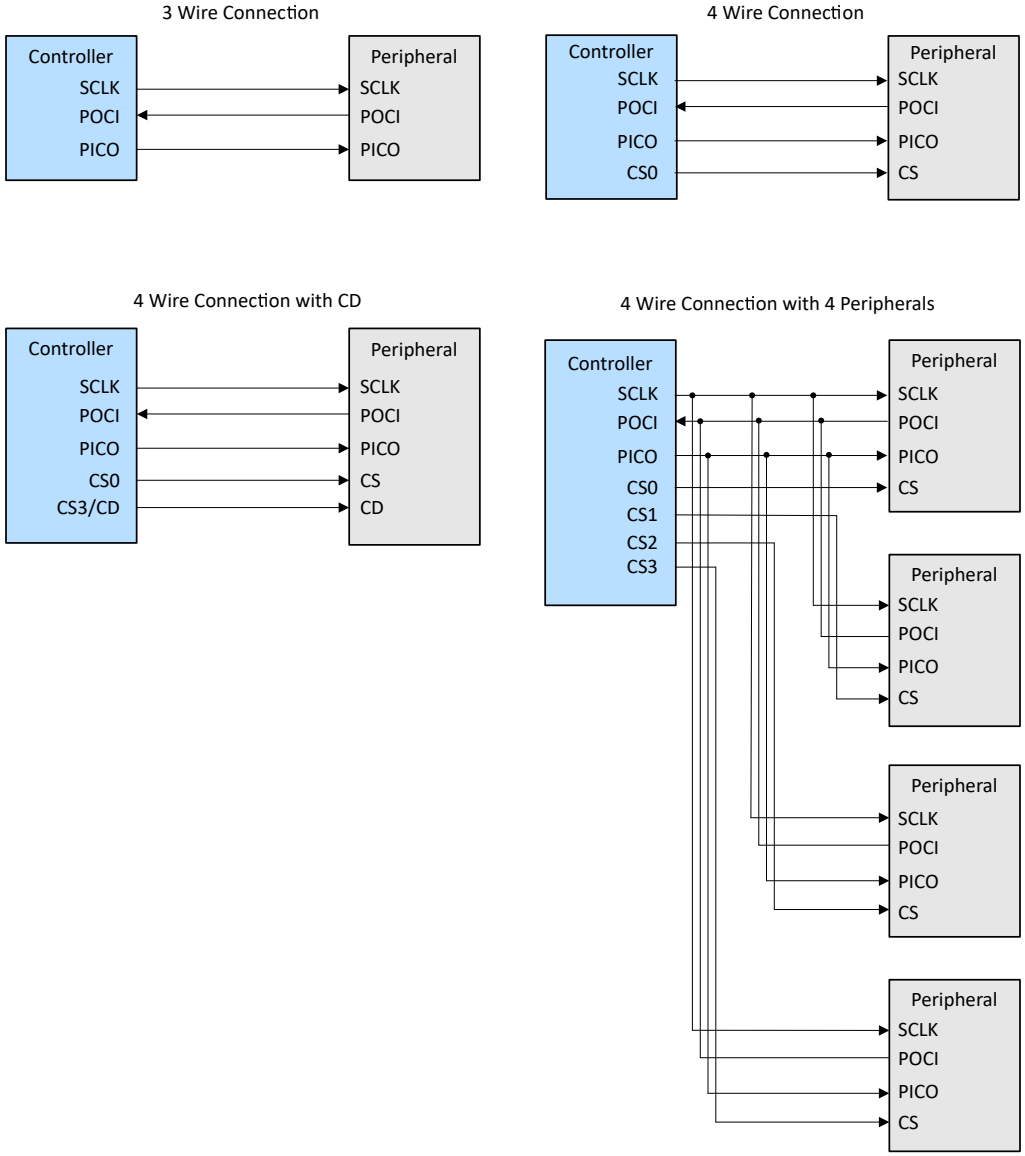


**Figure 7-4. External Connections for Different SPI Configurations**

For I2C bus, the MSPM0L device supports Standard, Fast and Fast plus mode, as shown in Table 7-4.

External pullup resistors are required when using I2C bus. The value of these resistors depends on the I2C speed - TI recommends 2.2k to support Fast mode+. For systems concerned with power consumption, large resistor values can be used. ODIO (see GPIOs) can be used to implement communication with a 5V device.

**Table 7-4. MSPM0L I2C Characteristics**

| PARAMETERS | | TEST CONDITIONS | Standard mode | | Fast mode | | Fast mode plus | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{I2C}$ | I2C input clock frequency | I2C in Power Domain0 | | 40 | | 40 | | 40 | MHz |
| $f_{SCL}$ | SCL clock frequency | | | 100K | | 400K | | 1M | MHz |
| $t_{HD,STA}$ | Hold time (repeated) START | | 4 | | 0.6 | | 0.26 | | us |
| $t_{LOW}$ | Low period of the SCL clock | | 4.7 | | 1.3 | | 0.5 | | us |
| $t_{HIGH}$ | High period of the SCL clock | | 4 | | 0.6 | | 0.26 | | us |
| $t_{SU,STA}$ | Setup time for a repeated START | | 4.7 | | 0.6 | | 0.26 | | us |
| $t_{HD,DAT}$ | Data hold time | | 0 | | 0 | | 0 | | us |
| $t_{SU,DAT}$ | Data setup time | | 250 | | 100 | | 50 | | us |
| $t_{SU,STO}$ | Setup time for STOP | | 4 | | 0.6 | | 0.26 | | us |
| $t_{BUF}$ | Bus free time between a STOP and START condition | | 4.7 | | 1.3 | | 0.5 | | us |
| $t_{VD;DAT}$ | Data valid time | | | 3.46 | | 0.9 | | 0.45 | us |
| $t_{VD;ACK}$ | Data valid acknowledge time | | | 3.46 | | 0.9 | | 0.45 | us |

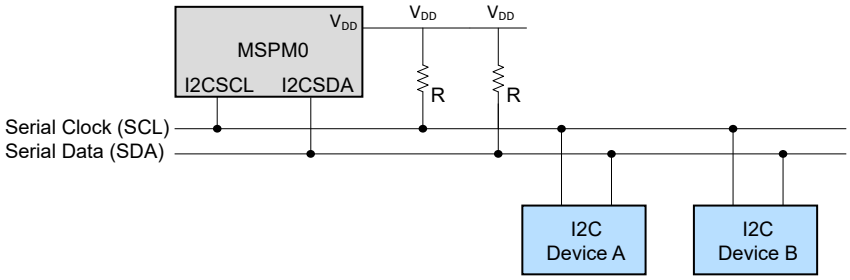


**Figure 7-5. Typical I2C Bus Connection**

# 8 GPIOs

MSPM0L series MCUs include Standard-Drive I/O(SDIO), High-Speed I/O(HSIO) and 5V tolerant Open-Drain I/O(ODIO). Users can flexibly choose the appropriate I/O type based on actual requirements. And the following characteristics need to be considered in hardware design.

## 8.1 GPIO Output Switching Speed and Load Capacitance

When using the GPIO as I/O, design considerations must be made to verify correct operation. As load capacitance becomes larger, the rise/fall time of the I/O pin increases. This capacitance includes pin parasitic capacitance (Ci = 5pF (Typical)) and the effects of the board traces. I/O characteristics are available in the device data sheet. Table 8-1 list the I/O output frequency characteristics of the MSPM0L device.

**Table 8-1. MSPM0L GPIO Switching Characteristics**

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{max}$ | Port output frequency | SDIO | VDD ≥ 1.71V, $C_L$ = 20pF | | | 16 | MHz |
| | | | VDD ≥ 2.7V, $C_L$ = 20pF | | | 32 | |
| | | HSIO | VDD ≥ 1.71V, DRV = 0, $C_L$ = 20pF | | | 16 | |
| | | | VDD ≥ 1.71V, DRV = 1, $C_L$ = 20pF | | | 24 | |
| | | | VDD ≥ 2.7V, DRV = 0, $C_L$ = 20pF | | | 32 | |
| | | | VDD ≥ 2.7V, DRV = 1, $C_L$ = 20pF | | | 40 | |
| | | ODIO | VDD ≥ 1.71V, $FM^+$, $C_L$= 20pF to 100 pF | | | 1 | |
| $t_r$,$t_f$ | Output rise or fall time | All output ports except ODIO | VDD ≥ 1.71V | | | 0.3 × $f_{max}$ | s |
| $t_f$ | Output fall time | ODIO | VDD ≥ 1.71V, $FM^+$, $C_L$= 20pF to 100pF | 20 × VDD / 5.5 | | 120 | ns |

**Note**

- The output voltage reaches at least 10% and 90% $V_{CC}$ at the specified toggle frequency.
- The output rise time of open-drain I/Os is determined by the pullup resistance and load capacitance.

## 8.2 GPIO Current Sink and Source

**Table 8-2. MSPM0L GPIO Absolute Maximum Ratings**

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| VDD | Supply voltage | 1.62 | | 3.6 | V |
| VCORE | Voltage on VCORE pin | | 1.35 | | V |
| $C_{VDD}$ | Capacitor placed between VDD and VSS | | 10 | | uF |
| $C_{VCORE}$ | Capacitor placed between VCORE and VSS | | 470 | | nF |
| $T_A$ | Ambient temperature, T version | –40 | | 105 | °C |
| | Ambient temperature, S version | –40 | | 125 | |
| $T_A$ | Ambient temperature, Q version | -40 | | 125 | °C |
| $T_J$ | Max junction temperature, T version | | | 125 | °C |
| $T_J$ | Max junction temperature, S and Q versions | | | 130 | °C |
| $f_{MCLK}$ | MCLK, CPUCLK, ULPCLK frequency with 1 flash wait state | | | 32 | MHz |
| | MCLK, CPUCLK, ULPCLK frequency with 0 flash wait states | | | 24 | |

**Note**

- The total current of I/O must be less than the maximum value of $I_{VDD}$.
- HSIO and ODIO are patched in a fixed pin; refer to the device data sheet.

SDIO and HSIO can sink or source a maximum current of 6 mA (typical), which is sufficient to drive a typical LED. The total combined current must be less than $I_{VDD}$ (80 mA typical).

## 8.3 High Speed GPIOs

HSIO can support up to 40MHz frequency, and this speed is related to bus clock, supply voltage, and load capacitance. Users can also select the output max frequency via the DRV bit in the DIO register.

## 8.4 Open-Drain GPIOs Enable 5-V Communication Without a Level Shifter

ODIO are tolerant to 5V input. Because the ODIOs are open drain, an external pullup resistor is needed for the pin to be able to output high. This I/O can used for UART or I2C interface with different voltage levels. To limit the current, a series resistor must be placed between the pin and the pullup resistor, and the RSERIES must be no less than 250Ω. As shown in Figure 8-1, TI recommends 270Ω. The value of the pullup resistor depends on the output frequency (see Section 7.3).

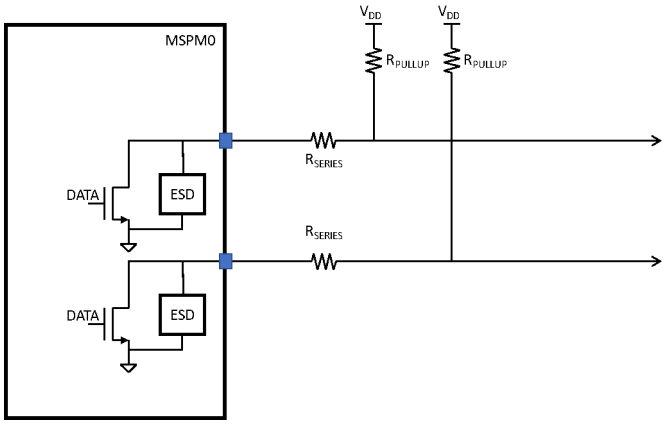


**Figure 8-1. Suggested ODIO Circuit**

## 8.5 Communicate With 1.8V Devices Without a Level Shifter

The MSPM0L series devices use a 3.3V logic level (excluding ODIO). To communicate with 1.8V devices without an external level shifter device, Figure 8-2 shows a suggested circuit for interfacing with a 1.8V device.

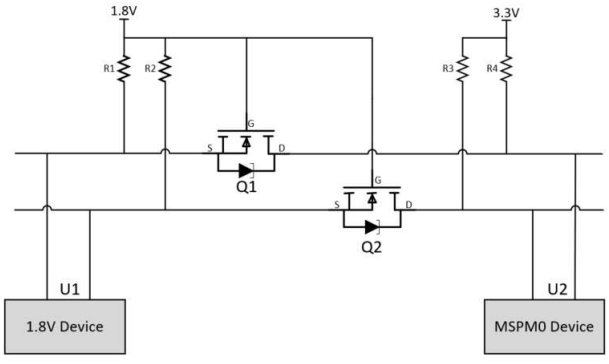


**Figure 8-2. Suggested Communication Circuit With 1.8V Device**

Two MOSFETs are used in this circuit. Check the VGS to verify this MOSFET be able to fully turn on with a low RDS(on): for a 1.8V device, use less than 1.8V VGS MOSFET. However, do not use a VGS MOSFET that is too low, as this causes the MOSFET to turn on at a very small voltage (MCU logic judges it as 0), resulting in a communication logic error.

### U1 output and U2 input

1. U1 output *1.8V high*, Q1 VGS around 0, thus Q1 turn off, U2 reads *3.3V high* with R4.
2. U1 output *low*, Q1 VGS near 1.8V, thus Q1 turn on, U2 reads *low*.

**U1 input and U2 output**

1. U2 output *3.3V high*, U1 keeps 1.8V with R1, and Q1 turns off, thus U1 reads *1.8V high*.
2. U2 output *low*, U1 keeps 1.8V with R1 at first, but the diode in the MOSFET pulls down U1 to 0.7V (diode voltage drops), and then causes VGS to be greater than the turn-on voltage, Q1 turns on, and U1 reads *low*.

## 8.6 Unused Pins Connection

All microcontrollers are designed for a variety of applications and often a particular application does not use 100% of the MCU resources.

To increase EMC performance, do not leave unused clocks, counters, and I/Os free or floating; for example, set I/Os to 0 or 1 (pullup or pulldown on unused I/O pins) and disable unused features.

**Table 8-3. Connection of Unused Pins**

| Pin | Potential | Comment |
|---|---|---|
| PAx | Open | Set corresponding pin functions to GPIO (PINCMx.PF = 0x1) and configure unsused pins to output low or input with internal pullup or pulldown resistor. |
| OPAx_IN0- | Open | This pin is high-impedance |
| NRST | VDD | NRST is an active-low reset signal; this must be pulled high to VCC or the device does not start. |

**Note**

- To reduce leakage, it is advisable to configure the I/O as an analog input or to push-pull and to set it to “0”.
- BSL invoke pin must be pulled down to avoid entering BSL mode after reset.

# 9 Layout Guides

## 9.1 Power Supply Layout

Figure 9-1 shows the typical parts placement and routing for the power supply layout; you must modify this appropriately for your MSPM0L part. Optionally connect a filter inductor in series with the VCC and MCU VDD pins. This inductor is used to filter the switching noise frequency of DCDC. For the value, see the data sheet of DCDC vendor. C1, C2, and C3 values and layout in the MSPM0L device data sheets.

**Note**

- Keep the smallest capacitance, closest to the MCU VDD pin (C1 < C2 < C3).
- All the traces must be direct without any vias.

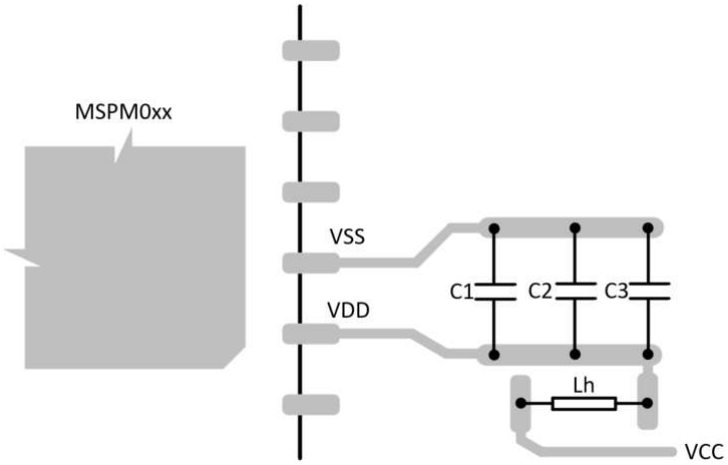


**Figure 9-1. Suggested Power Supply Layout**

## 9.2 Considerations for Ground Layout

System ground is the most critical area and foundation related to noise and EMI problems on the board. The most practical way to minimize these problems is to have a separate ground plane.

### What is Ground Noise?

Each signal originating from a circuit (driver) has a return current flow to the source through ground path. As the frequency increases, or even for simple but high-current switching like relays, there is a voltage drop due to line impedance generating interference in the grounding scheme. The return path is always via the least resistance. For DC signals, that is the lowest resistive path and for high frequency signals it is the lowest impedance path. This explains how a ground plane simplifies the issue and is the key to verifying signal integrity.

TI does not recommend that the digital return signals propagate inside the analog return (ground) area; therefore, split the ground plane to keep all the digital signal return loops within the ground area. This splitting should be done carefully. Many designs use a single (common) voltage regulator to generate a digital and analog supply of the same voltage level (for example, 3.3V). Isolate the analog rail and digital supply rails and the respective grounds from each other. Be careful while isolating ground, as both grounds have to be shorted somewhere. Figure 9-2 shows how possible return paths for digital signals are not allowed to form a loop passing through the analog ground. On each design, decide the common point considering the component placements and so forth. Do not add any inductors (ferrite bead) or resistors (not even zero Ω) in the series with any ground trace. The impedance increases due to associated inductance at a high frequency, causing a voltage differential. Do not route a signal referenced to digital ground over analog ground or the other direction.

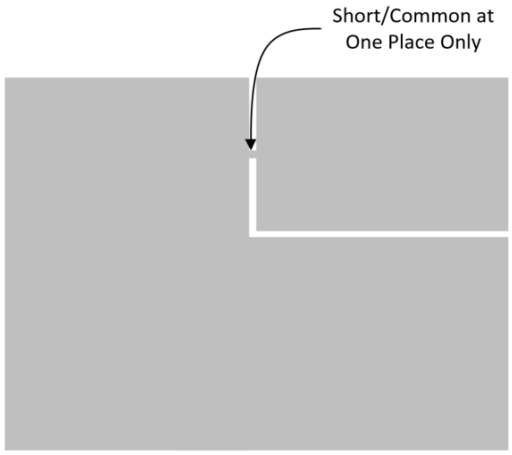


**Figure 9-2. Digital and Analog Grounds and Common Area**

## 9.3 Traces, Vias, and Other PCB Components

A right angle in a trace can cause more radiation. The capacitance increases in the region of the corner and the characteristic impedance changes. This impedance change causes reflections. Avoid right-angle bends in a trace and try to route them with at least two 45° corners. To minimize any impedance change, the best routing would be a round bend, as shown in Figure 9-3.

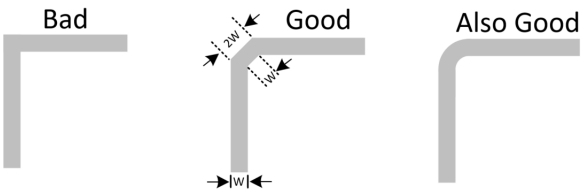


**Figure 9-3. Poor and Correct Way of Bending Traces in Right Angle**

To minimize crosstalk, not only between two signals on one layer but also between adjacent layers, route them 90° to each other. More complex boards need to use vias while routing; however, care must be taken when using vias as vias add additional inductance and capacitance, and reflections occur due to the change in the characteristic impedance. Vias also increase the trace length. When using differential signals, use vias in both traces or compensate the delay in the other trace as well.

For signal traces, pay more attention to the impact of high-frequency pulse signals, especially on relatively small analog signals (such as sensor signals). Too many crossovers couple the electromagnetic noise of the high-frequency signal to the analog signal, which will result in a low signal-to-noise ratio of the signal and affect the signal quality. Therefore, avoid crossing when designing. But if there is indeed an unavoidable intersection, TI recommends intersecting vertically to minimize the interference of electromagnetic noise. Figure 9-4 shows how to reduce this noise.

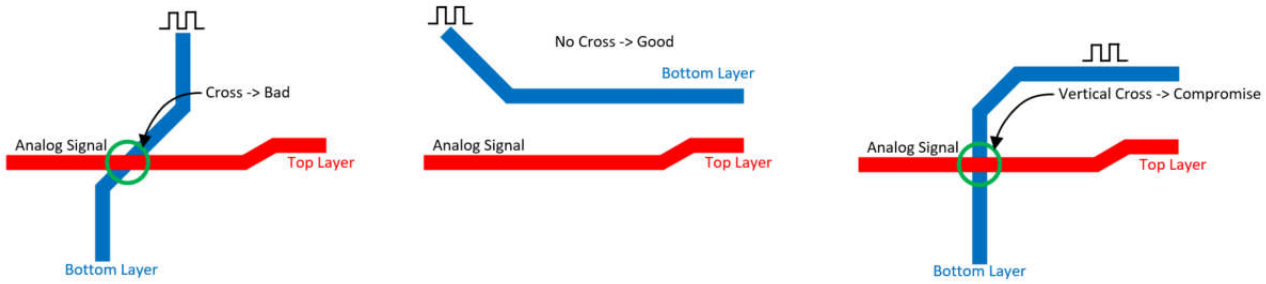


**Figure 9-4. Poor and Correct Cross Traces for Analog and High-Frequency Signals**

## 9.4 How to Select Board Layers and Recommended Stack-up

To reduce the reflections on high speed signals, match the impedance between the source, sink and transmission lines. The impedance of a signal trace depends on its geometry and its position with respect to any reference planes.

The trace width and spacing between differential pairs for a specific impedance requirement is dependent on the chosen PCB stack-up. As there are limitations in the minimum trace width and spacing which depend on the type of PCB technology and cost requirements, a PCB stack-up needs to be chosen which allows all the required impedances to be realized.

The minimum configuration that can be used is 2 stack-up. A 4- or 6-layer boards is required for very dense PCBs that have multiple high-speed signals.

The following stack-up (see Figure 9-5) is a 4-layer examples that can be used as a starting point for helping in a stack-up evaluation and selection. These stack-up configurations are using a GND plane adjacent to the power plane to increase the capacitance and reduce the gap between GND and power plane. So high speed signals on top layer have a solid GND reference plane which helps to reduce EMC emissions, as going up in number of layers and having a GND reference for each PCB signal layer improves further the radiated EMC performance.

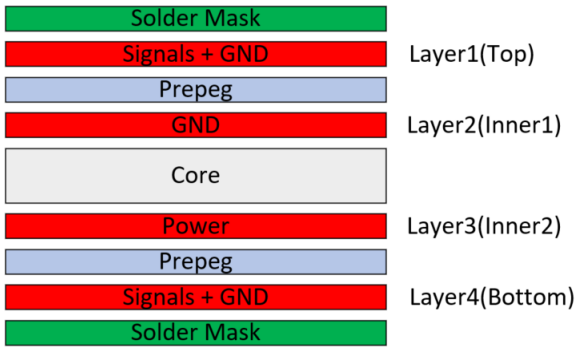


**Figure 9-5. Four-Layer PCB Stack-up Example**

If the system is not very complicated, there is no high-speed signal or some sensitive analog signal, then the 2 stack-up structure is sufficient.

# 10 Bootloader

## 10.1 Bootloader Introduction

A bootloader is a firmware IP (software shipped pre-programmed with the device) that can be used to program the memories of the SoC (Flash and SRAM) using serial interfaces such as UART and I2C. The bootloader is usually invoked after the bootcode has completed when the device is about to start the customer application. To support production programming use cases some bootloaders also offer more interfaces such as SPI or CAN. A bootloader can also be used for in-field updates.

## 10.2 Bootloader Hardware Design Considerations

### *10.2.1 Physical Communication interfaces*

The MSPM0L bootloader (BSL) is implemented on UART and I2C serial interfaces. In MSPM0L devices, the BSL can automatically select the interface used to communicate with the device. The BSL communication pins have been pre-defined in the ROM based bootloader. The specific instance of the peripheral interfaces that is used depends on the selected device and can be found in the device-specific data sheet. Please refer to the data sheet to find which pin has been assigned for BSL communication function before the hardware design.

**Note**

The BSL invoke pin must be pulled down to avoid entering BSL mode after reset.

### *10.2.2 Hardware Invocation*

The bootloader supports hardware invocation after a BOOTRST through the use of a GPIO. The BSL configuration in the NONMAIN flash memory contains the pad, pin, and polarity definition for the GPIO invocation. Devices come configured from TI for a specific GPIO and polarity, but software can change this default by modifying the GPIO pin configuration in the BSL configuration in NONMAIN flash memory. See the device specific data sheet to determine the default BSL invoke GPIO. Figure 10-1 shows an example for the GPIO pin PA18 with high level to trigger bootloader.

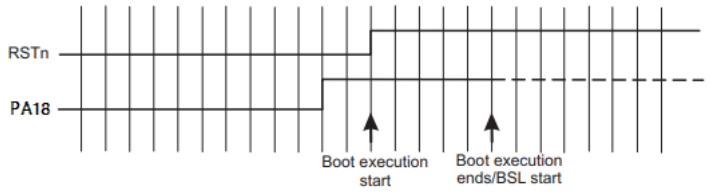


**Figure 10-1. BSL Entry Sequence at Configured GPIO Pin**

# 11 References

1. *MSPM0L130x Mixed-Signal Microcontrollers*, data sheet.
2. *MSPM0 L-Series 32MHz Microcontrollers*, technical reference manual.
3. *MSPM0 G-Series MCUs Hardware Development Guide*, application note.
4. *TLIN1021A-Q1 Fault-Protected LIN Transceiver with Inhibit and Wake data sheet (Rev. B)*, data sheet.

# 12 Revision History

| Changes from Revision A (March 2023) to Revision B (September 2025) | Page |
|---|---|
| • Updated the numbering format for tables, figures and cross-references throughout the document | 3 |
| • Updated Section 1 | 3 |
| • Added *LCD Design Considerations* | 18 |

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