Application Note

Make System Design Easy With MSPM0 Precision Analog

ABSTRACT

This application note provides a brief introduction for MSPM0 analog features. MSPM0 devices have a variety of integrated analog features that are not isolated peripherals in the device but instead support a number of options for the configuration of the internal connections. There is no need to add external components, and application software can easily configure the connections. The obvious benefits for the system design include BOM cost saving, smaller PCB size, ease of configuration, better reliability and flexibility.

Table of Contents

Trademarks

Arm® and Cortex® are registered trademarks of Arm Limited.
All trademarks are the property of their respective owners.

1 MSPM0 Family Overview

The MSPM0 family is the latest MSP system-on-chip (SoC) devices, that provides highly-integrated, ultra-low-power 32-bit MCUs based on Arm® Cortex®-M0+ 32-bit core platform. These cost-optimized MCUs offer high-performance analog peripheral integration, support extended temperature ranges from -40°C to 125°C and operate with supply voltages ranging from 1.62 V to 3.6 V. In the latest MSPM0 family, there are two series of devices: MSPM0G operates at up to 80-MHz frequency, and MSPM0L operates at up to 32-MHz frequency.

2 MSPM0 Main Analog Features

Both MSPM0L and MSPM0G devices provide a variety of analog features to support different system designs. MSPM0L devices offers a 12-bit 1.45-Msps ADC with configurable internal voltage reference, one dual-mode (fast mode and ultra-low-power mode) comparator with built-in reference DAC, two zero-drift zero-crossover operational amplifiers with programmable gain, one general-purpose amplifier, and an on-chip temperature sensor. MSPM0G devices offer high-performance analog peripherals such as two 12-bit 4-Msps ADCs, configurable internal shared voltage reference, one 12-bit 1-Msps DAC, three dual-mode (fast mode and ultra-low-power mode) comparators with built-in reference DACs, two zero-drift zero-crossover and rail-to-rail op-amps with programmable gain up to 32x, and one general-purpose rail-to-rail amplifier. Table 2-1 lists the analog features.

Table 2-1. MSPM0L and MSPM0G Analog Features

Feature	MSPM0G	MSPM0L
ADC	12-bit 4-Msps SAR	12-bit 1.45-Msps SAR
OPA	Two OPAs with 6-MHz gain bandwidth	Two OPAs with 6-MHz gain bandwidth
Comparator	Up to 3 with 8-bit DAC	1 with 8-bit DAC
12-bit DAC	1 Msps	Not supported
GPAMP	350-kHz gain bandwidth	350-kHz gain bandwidth

2.1 Best-in-Class 12-Bit ADC Integrated

The MSPM0 ADC provides best-in-class ENOB and SNR performance of any ADC in its MCU class. The ADC provides 12-bit 4-Msps sampling and 14-bit 250-ksps averaged sampling on MSPM0G devices and 12-bit 1.45-Msps sampling on MSPM0L devices. The hardware averaging feature is able to increase the effective resolution of the ADC without the need for software and CPU intervention. The ADC also operates at these high speeds in low-power modes with fast wakeup times. The ADC signals that can be sampled directly from onboard OPA, DACs, temperature sensors, and up to 16 external input channels. The reference voltage can be connected to VDD, an external reference, or internal references. Configurable 12-, 10-, and 8-bit resolutions also support faster sampling rates. Figure 2-1 shows the key attributes of the MSPM0 ADC.

:

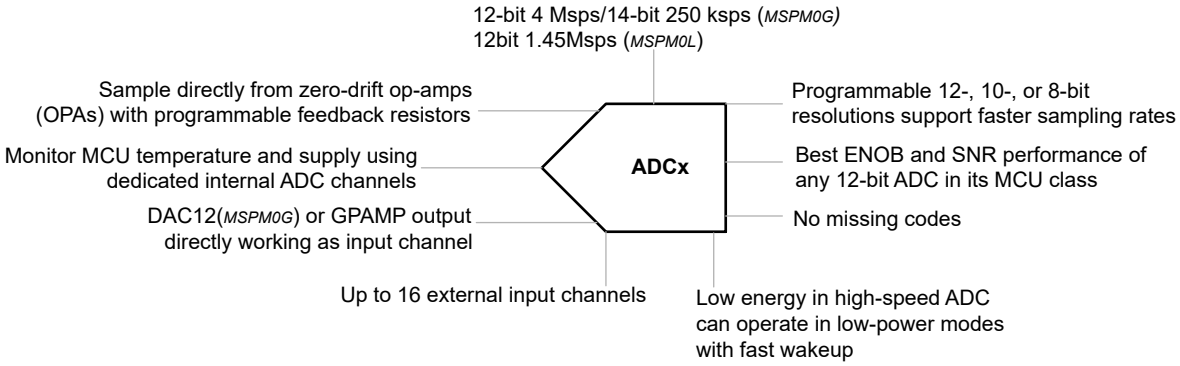

Figure 2-1. MSPM0 ADC Main Features

2.2 Dual Mode Comparator With Reference DAC

The MSPM0 comparator offers both ultra-low-power and fast modes of operation, MSPM0L have one comparator integrated and MSPM0G devices have up to 3 comparators integrated. The comparator offers the flexibility to support software-selectable analog filter for the comparator output, programmable hysteresis, and

two input codes in 8-bit DAC to configure reference voltage generator. In MSPM0G devices, two comparators can be combined to create a window comparator. Figure 2-2 shows the key attributes of the MSPM0 comparator.

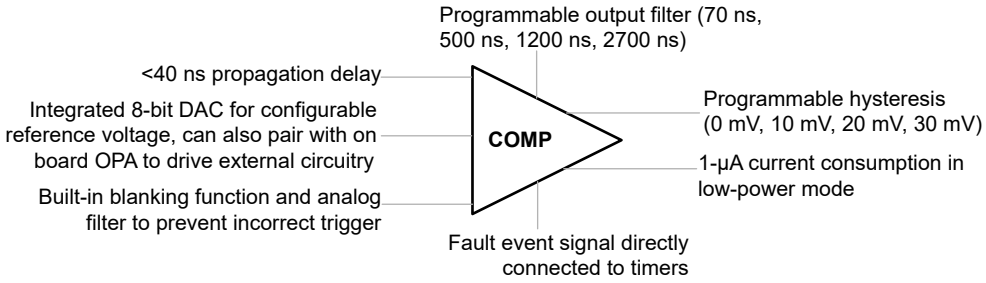

Figure 2-2. MSPM0 Comparator Main Features

2.3 Buffered 12-Bit 1-Msps DAC

In addition to the comparator with 8-bit DAC integration, MSPM0G devices also support an onboard 12-bit high-performance DAC, which can be configured as 8-bit or 12-bit voltage-output resolution. In the MSPM0G 12-bit DAC, a 4x12-bit internal FIFO and operation with the DMA controller are fully supported, and the DAC output is internally connected to the onboard OPA, ADC, and COMP. Figure 2-3 shows the key attributes of the MSPM0 DAC.

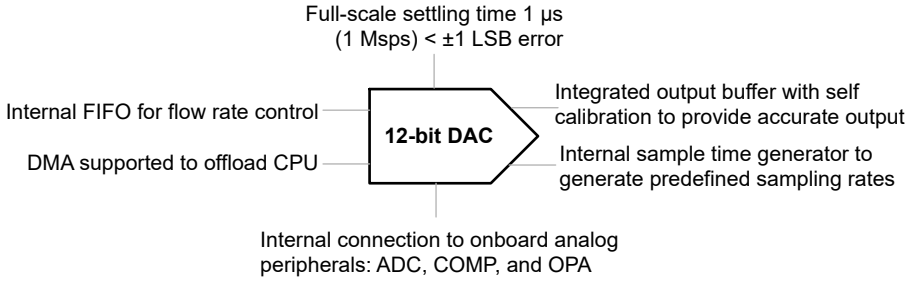

Figure 2-3. MSPM0 DAC Main Features

2.4 Zero-Drift and Zero-Crossover Chopper OPA

MSPM0L and MSPM0G devices integrate two high-performance OPAs, and a TIA is supported in MSPM0L134x variants. The MSPM0 OPA provides a variety of input channels for noninverting and inverting scenarios. The MSPM0 OPA supports chopping mode, which has standard chopping and ADC assistant chopping. The burnout current source (BCS) is supported to monitor the input signal of the sensor and detect if the sensor works well or not. Figure 2-4 shows the key attributes of the MSPM0 OPA.

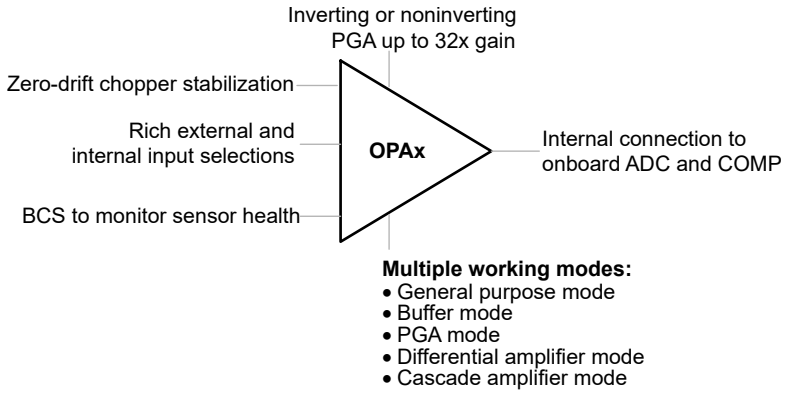

Figure 2-4. MSPM0 OPA Main Features

3 Easily and Flexibly Create the System With MSPM0 Analog Peripherals

MSPM0 devices support different scenarios for the individual analog features and flexible combinations of multiple analog peripherals. There is no need to add external devices to implement additional circuits to support those features – all of the configurations can easily be done in one device. The examples in the following section show the ease-to-use and the flexibility to build analog features with MSPM0 devices.

3.1 ADC Sample and Conversion

The sample-and-hold time determines how long to sample a signal before digital conversion. During the sample stage, an internal switch allows the input capacitor to be charged. The time required to fully charge the capacitor depends on the external capacitor to the ADC input pin. Figure 3-1 shows a model of the MSPM0 ADC.

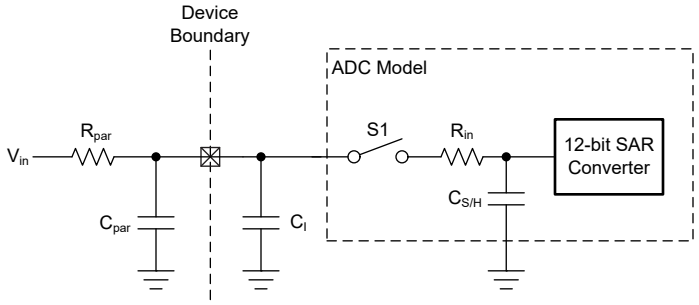

Figure 3-1. ADC Connection Diagram

The values of the ADC input impedance R_{in} and sample-and-hold capacitance $C_{S/H}$ can be found in the *ADC Electrical Characteristics* section of the device-specific data sheet. The values of the IO input capacitance C_{in} can be found in the *Digital IO Electrical Characteristics* section of the device-specific data sheet. The functions of R_{par} and $C_{par}|C_I$ in front of the ADC model are to provide a path for the charge injection and do some filtering between V_{in} and the ADC model. C_I is only specifically for IO input capacitance and is considered as a part of the RC filter.

3.2 Differential and Cascade OPA Configurations

Some MSPM0G and MSPM0L devices support two OPAs. If two OPAs are available on the device, they can be used as a differential amplifier or as cascaded mode.

Figure 3-2 shows an example of how to form a differential amplifier with two OPAs in an MSPM0 device.

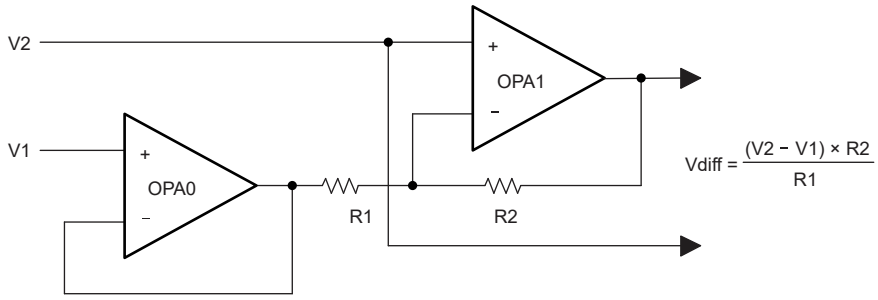

Figure 3-2. MSPM0 OPAs as a Differential Ampler

This circuit either adds or subtracts the voltages based on the resistors R1 and R2. The voltage difference can be calculated by the equation in the diagram, and the OPA output can also be measured by MSPM0 on board ADC or as an input to the comparator.

If the gain of one OPA is not enough, to obtain additional gain, the two OPAs can be configured as cascaded mode. Figure 3-3 shows a diagram of a cascaded amplifier. The total gain is based on the configurations of the resistors R1, R2, R3, and R4.

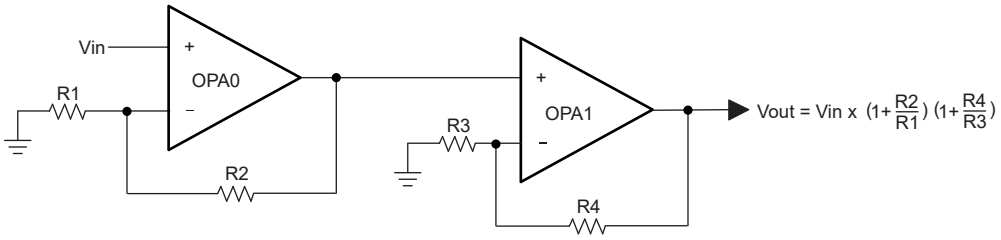

Figure 3-3. MSPM0 OPAs in Cascade Mode

3.3 Window Comparator Mode

MSPM0G devices support multiple comparators, and two comparators can be combined to create a window comparator. Two different threshold voltages are used in a window comparator. If the input signal is within the window, the comparator output is high. If the signal is outside of the window, the output is low. Figure 3-4 shows the window comparator mode.

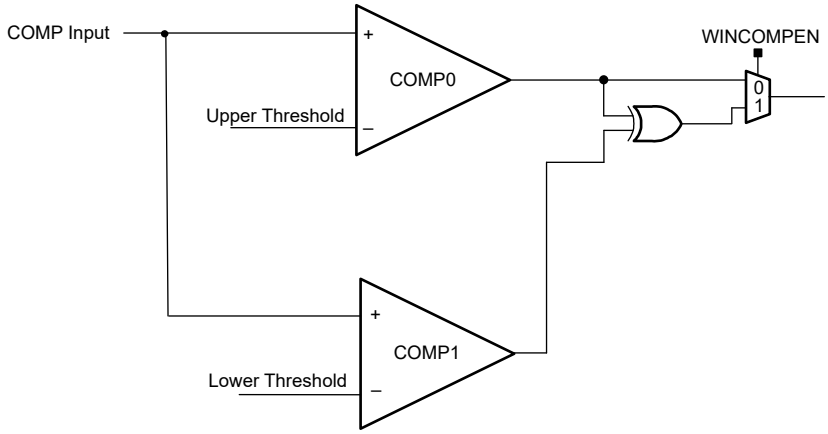

Figure 3-4. MSPM0 Window Comparator Mode

3.4 Internal Connections Between Different Analog Peripherals

Software can configure the internal analog connections in MSPM0 devices. The following examples show the internal paths inside MSPM0 devices to easily and flexibly create analog features for different use cases.

1. Route the OPA to the ADC and COMP to amplify the input signal (see Figure 3-5).

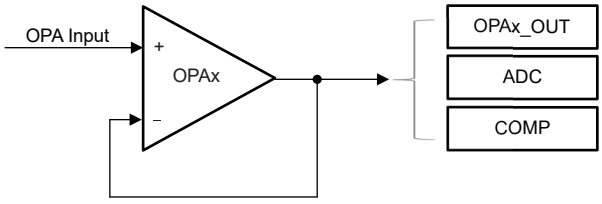

Figure 3-5. OPA Connection to ADC and Comparator

   OPA chopping mode can significantly improve the offset voltage and drift performance. When OPA connecting to ADC, if chopping mode is needed, besides standard chopping within OPA, there is ADC Assisted chopping mode can be supported.
2. Route the 8-bit DAC of the COMP or the 12-bit DAC to the OPA as bias generation.

   Some MSPM0G devices support the 12-bit DAC as a stand-alone peripheral in the device. This DAC can be directly connection to the OPA input to generate the bias voltage (see Figure 3-6).

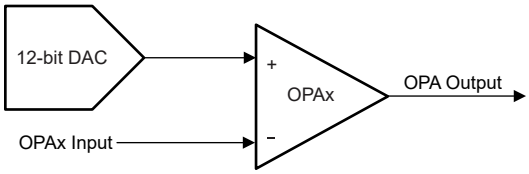

Figure 3-6. 12-bit DAC Connection to OPA

Not only the 12-bit DAC is able to generate the bias voltage. The 8-bit DAC in the comparator also has the connection to OPA (see Figure 3-7).

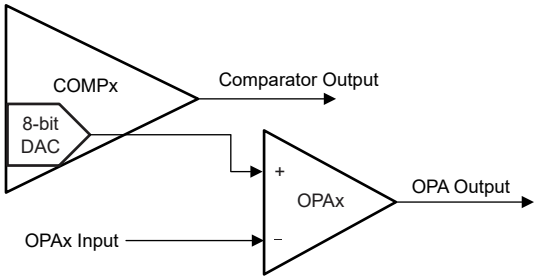

Figure 3-7. Comparator 8-bit DAC Connection to OPA

3. Connect the GPAMP output to the ADC and OPA to amplify the input signal.

   Direct connections from the GPAMP to other analog peripherals, like the OPA, are supported. When connecting to ADC, the standard and ADC assisted chopping modes are also supported in the GPAMP (see Figure 3-8).

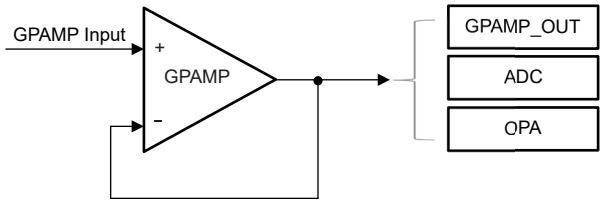

Figure 3-8. GPAMP Connection to ADC and OPA

4 Analog Comparison With STM32

The MSPM0 and STM32 are not identical devices in terms of features or pin count, however the device are similar and target similar applications. Table 4-1 lists the details of analog feature comparison between MSPM0 and STM32F0/G0/C0. There is no OPA support in STM32F0/G0/C0, and both MSPM0L and MSPM0G offer two zero-drift zero-crossover and rail-to-rail op-amps.

Table 4-1. MSPM0 vs STM32 Analog Features

Features		MSPM0G	MSPM0L	STM32F0	STM32G0	STM32C0
CPU		Cortex M0+ 80 MHz	Cortex M0+ 32 MHz	Cortex-M0 48 MHz	Cortex M0+ 64 MHz	Cortex M0+ 48 MHz
VDDA		1.62 V to 3.6 V	1.62 V to 3.6 V	2.4 V to 3.6 V	1.62 V to 3.6 V	2 V to 3.6 V
ADC	**Channel and sampling rate**	16 channels 12-bit 4 Msps	10 channels 12-bit 1.45 Msps	16 channels 12-bit 1 Msps	16 channels 12 bit 2.5 Msps	
	ENOB	11.2-bit	11.2-bit	Not provided	10.2 bit	
	SNR (Vref = VDD)	70 dB	70 dB	Not provided	64 dB	
	INL	±2 LSB	±2 LSB	±1.7 LSB	±1.5 LSB	
	DNL	±1 LSB	±1 LSB	±1.3 LSB	±3 LSB	
Comparator	**Input hysteresis**	0.4, 10, 20, 30 mV	0.4, 10, 20, 30 mV	0, 8, 15, 31 mV	0, 10, 20, 30 mV	Not supported
	Propagation delay	49 ns	49 ns	240 ns	50 ns	
	Startup time	1.2µs	1.2µs	60 µs	15 µs	
	Integrated DAC	8-bit DAC	8-bit DAC	Not supported	Not supported	
DAC	**Data rate**	12 bit 1 Msps	Not supported	1 Msps	12-bit	Not supported
	ENOB	11 bit		Not provided	11.5 bit	
	SNR	70 dB		Not provided	71.6 dB	
	INL	±4 LSB		±4 LSB	±4 LSB	
	DNL	±1LSB		±2LSB	±2LSB	
OPA	V_{CM}	-0.1 V to (VDD – 0.3 V)		Not supported		
	GBW	6 MHz				
	Slew rate	4 V/µs				
	THDN	0.005%				

For the performance of analog features, the noise is an unwanted signal, as it interferes with the original message signal and corrupts the parameters of the signal. For example, ADC noise errors strongly impact the ENOB (effective number of bits). MSPM0 devices provide 70-dB SNR (signal-to-noise ratio) so ENOB can reach 11.2-bit with the 12-bit SAR ADC.

5 References

1. MSPM0 G-Series 80-MHz Microcontrollers Technical Reference Manual
2. MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265