Application Note

Output Swings and Common-mode Settings in AC-coupled and DC-coupled DAC

Arash Loloee, Laxmi Vivek Tripurari

ABSTRACT

This application notes discusses the different output configurations of the TAD5212-Q1 DAC, such as single-ended, differential, and pseudo-differential, and the resulting output swings. Common-mode settings in AC-coupled and DC-coupled configurations, along with related registers to configure the DAC, are also briefly discussed. The TAD5212 has several features, including mixing external analog signals with DAC outputs or bypassing the DAC and routing the external analog signal to the outputs. The various type of load and the range of loads are discussed in this application note.

Table of Contents

Trademarks

1 Introduction

The TAD5212-Q1 is a high-performance stereo DAC which supports 2-VRMS differential-ended and 1-VRMS single-ended input, as well as differential, pseudo-differential, and single-ended output.

The device consists of two pairs of analog output pins (OUTxP and OUTxM) that can be configured as differential outputs or single-ended outputs for playback channel. The device supports simultaneous playback of up to four channels of single-ended output or up to two channels of fully-differential or pseudo-differential output using the high-performance multichannel DAC.

The source of OUT1P and OUT1M can be selected with register 100 in Page 0. There are three bits (OUT1x_SRC[2:0]) that control the source for a specific path, for example code 011 is used for mixing of DAC output with analog bypass signal chains, and code 100 selects OUT1P of the DAC, and OUT1M for the analog bypass signal chain. These examples are among several available options. See also the TAD5212-Q1 data sheet for a complete list of available options for selection of the source for signal chain path for OUT1P and OUT1M. Similar to OUT1P and OUT1M, the OUT2x_SRC[2:0] bits in register 107 can be used to set the source for OUT2P and OUT2M.

The output channels for playback can be enabled or disabled by using register 118 (CH_EN) and the input channels for the audio serial interface can be enabled or disabled by using the PASI_RX_CHx_CFG or SASI_RX_CHx_CFG bits.

The TAD5212-Q1 device supports simultaneous power-up and power-down of all active channels for simultaneous playback. However, based on the application needs, if some channels must be powered-up or

powered-down dynamically when the other channel playback is on, then that use case is supported by setting the DYN_PUPD_CFG register. Figure 1-1 shows the functional block diagram of internal components of the DAC.

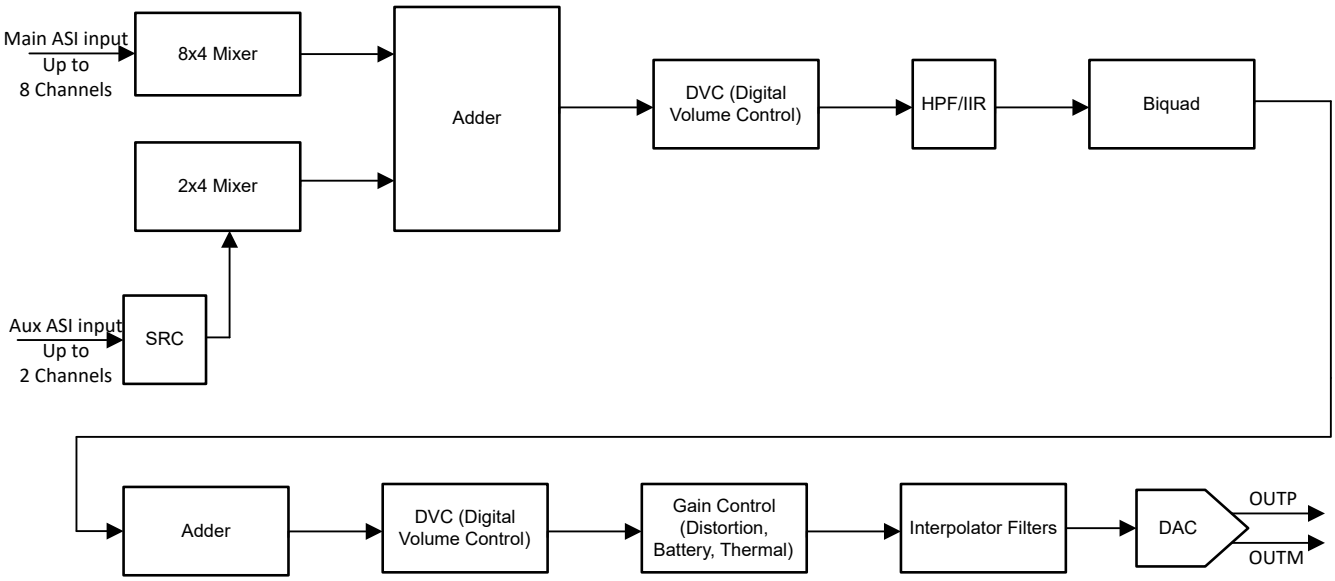

Figure 1-1. Functional Block Diagram of Internal Components of the DAC

2 Output Configuration

There are two buffers following the output of the DAC in Figure 2-1, each buffer provides negative feedback. One negative input of the buffer is connected to the output of the DAC, while the positive input is connected to the common-mode node. The output of each buffer is connected to one of the output pins. Depending on the application, one or both of these buffers can be used. The TAD5212-Q1 supports up to two channels of differential output, up to two channels of pseudo-differential output, and up to four channels of single-ended output. Each of the output channels can be independently configured for differential- or single-ended output.

Register 100 and 107 are used to configure the output connections, such as differential output, or single-ended, and so on for OUTxP and OUTxM, where *x* is the channel number corresponding to channel one or two. Each configuration and the allowable swing are discussed further in this section.

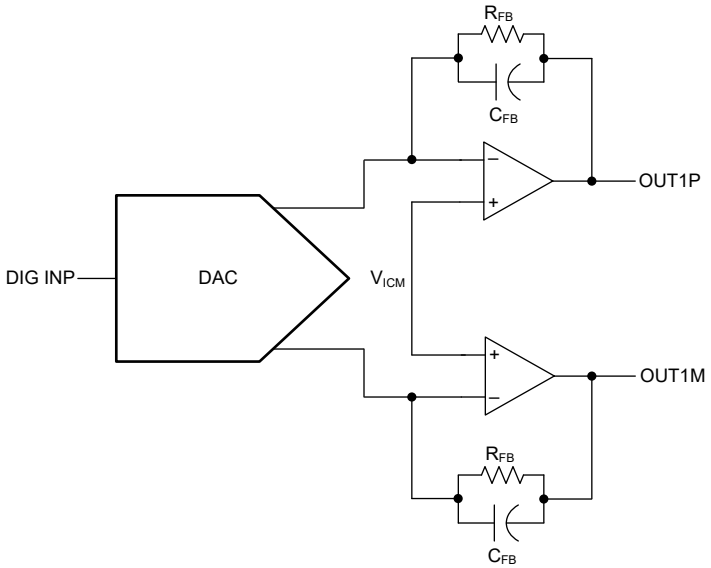

Figure 2-1. General Structure of DAC and Output Buffer Amplifiers

In fully-differential configuration, the DAC data is available differentially at both output pins. In this configuration, the load is attached between the two output pins. In differential mode, the load can be AC coupled, with a capacitor at the output before the load. Or the load can be DC coupled, connecting the outputs directly to the load. Figure 2-2 and Figure 2-3 show the AC and DC coupling in fully-differential mode. The maximum swing for the fully-differential configuration is 2Vrms. This maximum swing is 2Vrms because one output is 180 degrees out of phase with respect to the other output, effectively doubling the resulting swing, shown in Figure 2-4.

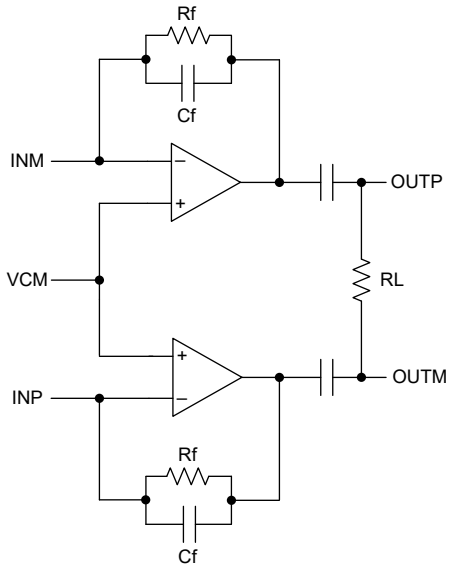

Figure 2-2. Fully-differential AC Coupling

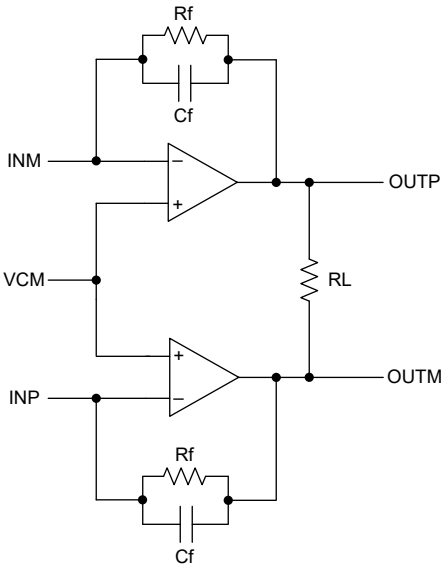

Figure 2-3. Fully-differential DC Coupling

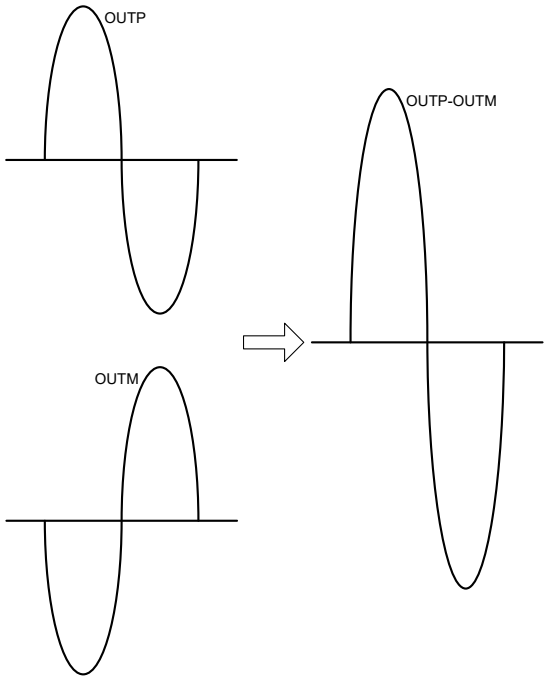

Figure 2-4. Signal Amplitude and Phase for Each Output and the Resulting Differential Signal

In single-ended configuration, the output can be on one output pin OUTP or OUTM) but needs to be AC-coupled because without the capacitor, a current draw can result. The current drawn depends on the load connected. Figure 2-5 shows an example of the single-ended configuration with AC coupling. The maximum swing for single-ended configuration is half of that the fully-differentiated configuration at 1Vrms.

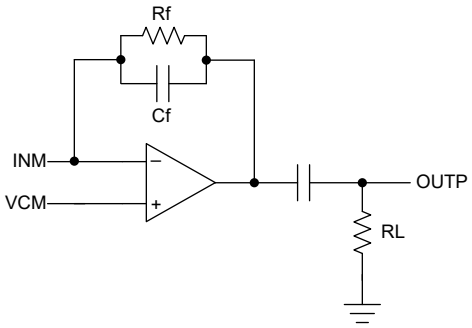

Figure 2-5. Single-ended Configuration With Needed AC Coupling

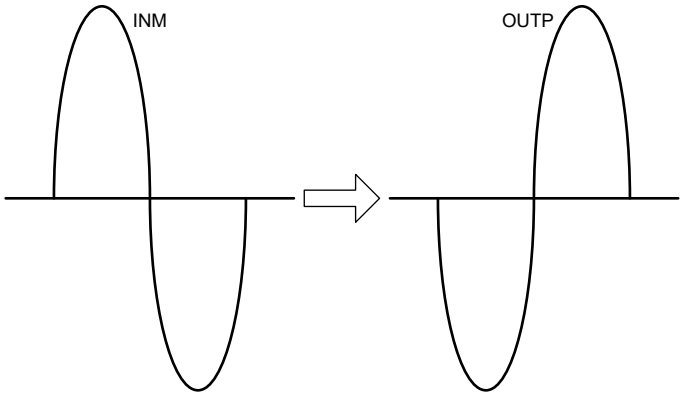

Figure 2-6. Inversion of Signal in Single-ended Configuration

The pseudo-differential configuration is similar to fully-differential configuration but in this case the DAC output is on one pin while the other pin is connected to the common-mode voltage. The primary use-case of the pseudo-differential configuration is to avoid the AC-coupling capacitor. Similar to the fully-differential configuration, pseudo-differential configuration allows use of the load with or without the AC coupling capacitor. The maximum swing for the pseudo-differential configuration is 1Vrms. Figure 2-7 shows the pseudo-differential configuration with DC load coupling.

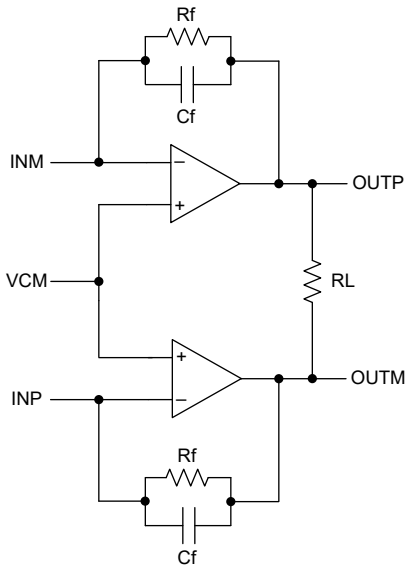

Figure 2-7. Pseudo-differential Configuration With DC Coupling

The TAD5212 can have a combination of drivers used in each mode. Typically, single-ended outputs use four channels, whereas fully-differential and pseudo-differential configurations use two channels. However, one

distinct feature of this DAC is the capability to use all four channels, even in single-ended configuration, because the DAC acts as two half-DACs.

The DAC works off either a nominally 3.3V, 3V, or 1.8V supply. For a 3.3V supply, the internally-generated reference is 2.75V, which permits a 2Vrms swing differentially or 1Vrms swing in single-ended configuration.

When a 1.8V supply is used, then the reference drops to 1.65V with a common-mode voltage of 0.9V so that the output can swing 5V above and below the common-mode voltage without saturating the drivers.

In general, the headroom reduces as the supply voltage is reduced to be able to drive the load with the existing supply. Table 2-1 shows the supply voltages with the resulting reference voltage and output swing.

Table 2-1. Supply Voltages, internal references, and Output Swings

Supply	Internal Reference	FD Swing (Vrms)	SE Swing (Vrms)
3.3V	2.75V	2V	1V
3.3V	2.5V	1.818V	0.919V
1.8V	1.375V	1V	0.5V

2.1 Common-mode Generation

The TAD5212 features Pseudo diff with external Common Mode sense to get rid of crosstalk on the output common mode. For this, HPL and HPR pins are referenced to HPCOM Common Mode with HPCOM_FB as star connection that results in reduction of channel to channel crosstalk.

There are two different methods to generate the internal common-mode. One method is to use the supply voltage as the reference and generate a common-mode voltage, which is typically half of the VDD, as shown in Figure3a. While this method is a straight-forward approach, this common-mode voltage carries the unwanted frequency components present in the supply voltage, showing up at the output. The second method to generate common-mode voltage is to use the internal reference, such as VREF, and generate the common-mode voltage from the reference voltage, providing a better power supply rejection ratio for single-ended configuration. This second method is shown in Figure 2-8.

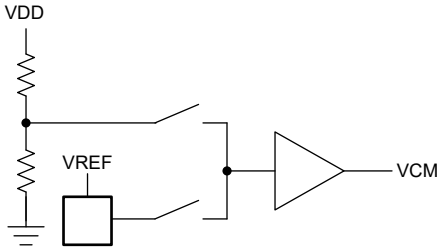

Figure 2-8. Internal Generation of VCM Using Supply Voltage or Reference Voltage

2.2 Output Load Range for Line Output And Headphone

The TAD5212-Q1 supports a variety of loads, including headphone, lineout, and receiver amplifiers. Load drive configurations are available for each pin independently. OUT1P_DRIVE[1:0] (OUT1x_CFG[7:6]) configures the load drive capability for the OUT1P pin. OUT1M_DRIVE[1:0], OUT2P_DRIVE[1:0], and OUT2M_DRIVE[1:0] are the output drive control for OUT1M, OUT2P, and OUT2M, respectively.

The output is configurable as either *Line Out* or *Head Phone Load*. The range of the load for Line Out is from 600Ω to infinity (an open) with a wide capacitor range (0 to 2nF) with nominal value of 10kΩ. The range of load for Headphone is from 4Ω to 600Ω with a nominal value of 16Ω with the wide capacitor range (0 to 2nF). The TAD5212-Q1 is capable of driving a wide range of loads, extending from 4Ω to infinity (an open). With a 4Ω load, there is stability concern and thus need to increase the bias current to increase the bandwidth. This can be done by adjusting the respective register map.

The Output Stage is designed to support a maximum power of 62.5mW on the single-ended 16Ω configuration (1 VRMS) and 125mW on the fully-differential 32Ω configuration (2 VRMS).

Setting the diver strength is also possible to drive higher load at the expense of degraded bandwidth. In general, the driver strength can have four distinct options, as shown in Table 2-2.

Table 2-2. Driver Strength Options

Value	Application
b'00	For Line out driver with minimum 300Ω impedance
b'01	For Headphone driver with minimum 4Ω impedance
b'10	For 4Ω load
b'11	Fully-differential Receiver and Debug

2.3 Mixing and Bypass

In applications like karaoke, where overlaying voice while music is streamed, mixing the external analog microphone input with the stored and recorded digital input is required. The mixed output needs to be played on the analog output of the DAC.

The TAD5212 supports mixing the DAC output with external analog inputs as well as routing external analog signals to the output.

In Figure 2-9, there are two independent paths to the output of the chip. One path is the output of the DAC that is connected through the buffers to output pins. The second path can be connected to external analog inputs.

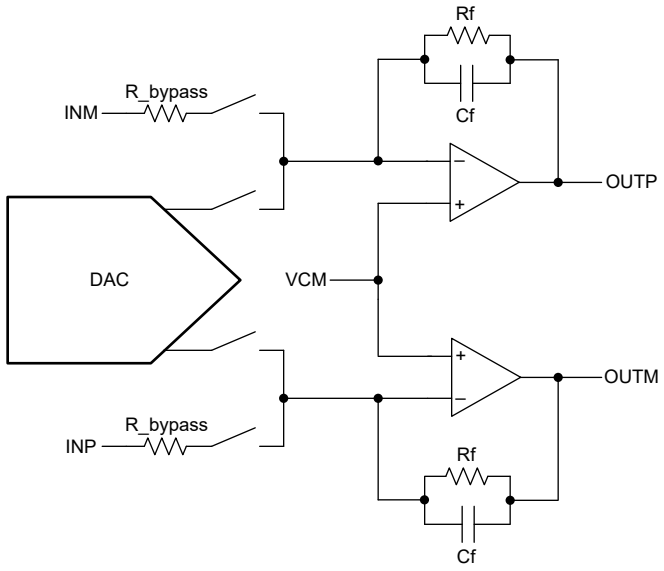

Figure 2-9. DAC and External Analog Signal Full Path

The TAD5212 supports multiple data mixing options with up to eight input channels from Main ASI, two Input Channels from Aux ASI, and a tone generator that can be mixed with flexible gain options for each path before playback on DAC output. By default, these mixers are disabled and channels are configured for only one channel data. Table 2-3 summarizes the DAC defaults and configurations of the mixer. In Stereo Single Ended mode (SSE) the device can support up to four independent single-ended outputs. SSE is configured through OUT1x_CFG (B0_P0_R100_D[4:2]) and OUT2x_CFG (B0_P0_R107_D[4:2])

Table 2-3. DAC Mixer Defaults and Configurations

DAC_CONFIG	MIXER DEFAULT
(DIFF/SE/PDIFF)	ASI_RX_CH1 → LDAC/RDAC
	ASI_RX_CH2 → LDAC2/RDAC2
SSE	ASI_RX_CH1 → LDAC
	ASI_RX_CH2 → RDAC
	ASI_RX_CH3 → LDAC2
	ASI_RX_CH4 → RDAC2

Mixers can be configured by setting ASI_DIN_Mixers in Page 17 of register map. If the DAC and analog input are both enabled, the user must verify that the combination of analog bypass and digital DAC signal chain does not cross the full scale value. There are independent gain knobs for the digital DAC signal chain (Book0, Page 0_Rregister 103 and 110) that can be adjusted as long as the end output is not beyond full scale.

A feature of the TAD5212 is the ability to bypass the DAC and send an analog input signal directly to the DAC output. This feature is accessed by using register 100 (0h64) and register 107 (0h6B) for VOUT1x and VOUT2x, respectively. If the output signal needs to be received from OUTP, then the analog signal needs to be applied at INM input and due to the negative feedback connection, the output signal is the inverted version of the input signal.

The input impedance of the analog input for single-ended use-cases has the option for 4.4kΩ or 20kΩ impedance. For fully-differential configurations, the options are 8.8kΩ or 40kΩ.

In Figure 2-9, the switches in the analog input signal path close, while the switches in the DAC output open up to route the analog signal to the output buffers and then to the output pins.

The OUT1x_CFG0 register (Address = 0x64) can be used for different configuration to direct the DAC and analog inputs to OUT2P and OUT2M. Similarly, the OUT2x_CFG0 register (Address = 0x6B) can be used for different configurations to direct the DAC and analog inputs to OUT2P and OUT2M.

As an example, the device can be programed to route the input from the DAC signal chain or the input from the analog bypass path to the DAC outputs. Similarly the device can independently route the DAC output to OUT2P, IN2P to OUT2M, the DAC output to OUT2M, or the analog input at IN2M to OUT2P, among many other options, including disabling output drivers. Table 2-4 summarizes the variety of options to route the analog or DAC output to the output pins.

Table 2-4. Path Selection Reference

OUTxx_CFG[2:0] Input	OUT1P/OUT1M Pin Configuration
000	OUTxP/OUTxM as a differential pair (default)
001	OUTxP and OUTxM as independent single-ended outputs
010	Mono single-ended output on OUTxP only
011	Mono single-ended output on OUTxM only
100	Pseudo-differential output with OUTxP as signal and OUTxM as VCOM
101	Pseudo-differential output with OUTxP as signal, OUTxM as VCOM and OUTxM as VCOM sense
110	Pseudo-differential output with OUTxM as signal and OUTxP as VCOM
111	Reserved. Do not use this setting

The TAD5212 supports ±100mV common-mode voltage on the analog pins in bypass mode. In pseudo-differential configuration, the input and the common-mode voltage need to be applied to ANA_P and ANA_M, respectively, to get the output at OUT1P. This same rule applies to OUT2P, when the other channel is being used.

3 Available Settings for Hardware-Controlled Devices

Several settings are available for hardware control devices using the MDx pin. The MD0 to MD6 pins allow the device to be controlled by either pullup or pulldown resistors. Dedicated tables in data sheet of pin controlled devices, for instance, show the configuration table for setting word length and AVDD supply voltage using MD1 and MD2. For non PDM mode, MP4 and MP5 can be used to set the analog input output configuration modes such as Differential, Single ended or Pseudo differential output, with Receiver or Headphone or Lineout load according to the table for Analog Output Configurations.Bits B0_P254_R41_D<2:0> are used to remap the different configurations based on the value of this register. For example, a zero value on this register can result the default functionality according to the tables mentioned previously. If remapped bits are made 1, then all these MD pins can be mapped to new functionality, For example a ONE written in bit D2 of register 41, can change the functionality based on the voltage applied to MD3 pin. In this case, when MD3 is 0, then IC is set for AVDD=1.8V operation and when MD3 is set to High, the IC is set for AVDD=3.3V operation.

4 Summary

The TAD5212 supports different output configurations as well as different output swings. This application note provides a brief review of the output load ranges for the line and headphone as well as features for mixing or bypassing the DAC output with related registers to configure the DAC.

5 References

- Texas Instruments, *TAD5212-Q1 High-performance Stereo Audio DAC With 119-dB Dynamic Range DAC*, data sheet

6 Revision History

Changes from Revision * (November 2023) to Revision A (July 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added *Available Settings for Hardware-Controlled Devices* section	8

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