Application Note

MSPM0 ADC Noise Analysis and Application

ABSTRACT

This document provides analog-to-digital converter (ADC) noise analysis and introduces the MSPM0 MCU ADC application.

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Trademarks

1 ADC Introduction

1.1 SAR ADC Principle

Figure 1-1 shows the system schematic diagram of SAR ADC. SAR ADC controls the switching of multiple switches (12 switches in this case) to perform capacitive voltage division on VREF and obtain different analog voltage output results. Compare the analog voltage with the input sampling signal, and the output of the comparator is used to adjust the on/off state of the switch, ultimately making the simulated voltage obtained by VREF voltage division as close as possible to the input voltage. The actual comparison process is achieved by using the binary method to approximate VREF division for the VIN, thus requiring 12 cycles for data conversion. When considering the ADC triggering, signal sampling and holding time, the actual SAR ADC conversion process takes more than 12 cycles (It takes 14 conversion cycles in MSPM0 G-Series).

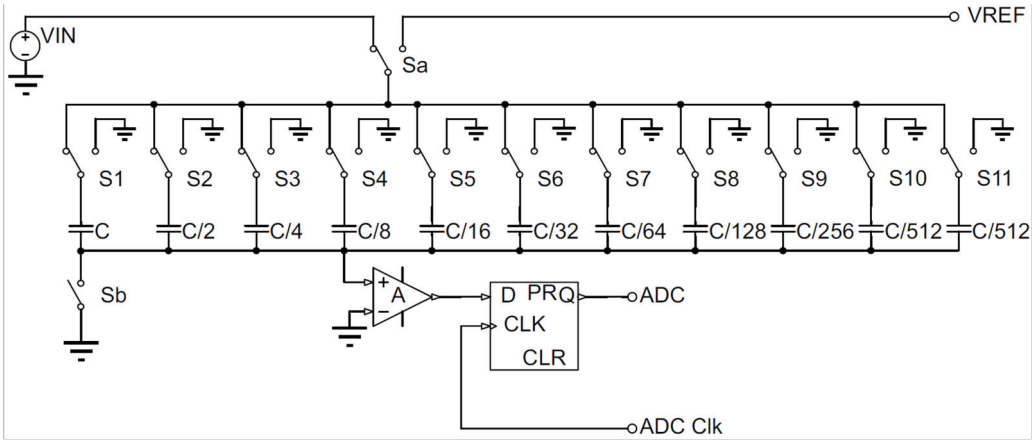

Figure 1-1. Principle Block Diagram of SAR ADC Based on CDAC

1.2 ADC Parameters

1.2.1 Static Parameters

- Differential Nonlinearity Error (DNL)

  Differential nonlinearity error is the maximum deviation between the actual step and the ideal step during the ADC analog-to-digital conversion process, where the ideal step refers to 1LSB. DNL exceeding 1LSB results in missing codes in the ADC digital result, meaning that a certain digital code will disappear in the output result.

$$\mathrm{DNL} = \mathrm{Actual}\quad \mathrm{Step} - 1\mathrm{LSB} \tag{1}$$

- Integral Nonlinearity Error (INL)

  Integral nonlinear error is the deviation between a certain conversion voltage and the ideal conversion voltage during the ADC conversion process, which reflects the integration of DNL. The measurement of this value was carried out after compensating for offset error and gain error. By measuring the conversion voltage of each digital code, the INL of each code point can be obtained. Only the maximum INL value is provided in the ADC data manual.

$$\mathrm{INL} = \mathrm{the}\quad \mathrm{kth}\quad \mathrm{actual}\quad \mathrm{conversion}\quad \mathrm{voltage} - (\mathrm{k} - 0.5)\mathrm{LSB} \tag{2}$$

- Offset Error (EO)

  Offset error is the deviation between the voltage at the first actual conversion and the first ideal conversion when the ADC increases from a low voltage. The first conversion occurs when the digital ADC output changes from 0 to 1. For an ideal ADC, when the analog input is between 0.5 LSB and 1.5 LSB, the digital output should be 1, thus the first ideal conversion occurs at 0.5 LSB. So offset error calculation formula is:

$$\mathrm{EO} = \text{the first actual conversion voltage} - 0.5\mathrm{LSB} \tag{3}$$

- Gain Error (EG)

  Gain error is the voltage deviation between the last actual conversion voltage and the last ideal conversion voltage, and this value is measured after correcting the offset error. Taking a 12-bit ADC as an example, the last actual conversion occurs when output digital result changes from 0xFFE to 0xFFF, which corresponding to a voltage of *VREF+* - 0.5 LSB. Therefore, the calculation formula is:

$$\mathrm{EG} = \text{the last actual conversion voltage} - \left(\mathrm{VREF}_{+} - 0.5\mathrm{LSB}\right) \tag{4}$$

1.2.2 Dynamic Parameters

1.2.2.1 AC Parameters

Measurement conditions: Input a sinusoidal AC voltage between the positive and negative terminals of the ADC and observe the sampling output results of the ADC. By analyzing the frequency spectrum of the output signal through Fourier transform, to obtain the signal fundamental frequency, harmonic, and noise components. ADC dynamic AC parameter are calculated based on these components.

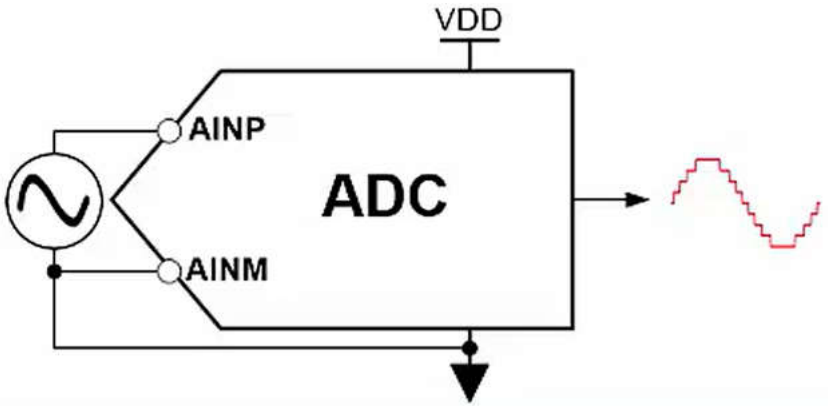

Figure 1-2. Diagram of ADC AC Test

- Total Harmonic Distortion (THD)

  Total harmonic distortion refers to the ratio of the total power of all harmonic components in an AC signal to the power of the fundamental frequency signal. The calculation formula in decibel form is as follows.

$$\mathrm{THD} = 20\log_{10}\left(\frac{\Sigma \mathrm{V}_{\mathrm{Harmonics}}}{\mathrm{V}_{\mathrm{Signal(RMS)}}}\right)\left(\mathrm{dB}\right) \tag{5}$$

  In the experiment of ADC communication parameter measurement, *THD* is caused by the nonlinearity of the ADC transmission characteristic curve, which means that the output and input of the ADC do not meet strict linear relationship within the sampling range (caused by the static error *DNL*/*INL*/*E* **O**/*E* **G** of the ADC), resulting in the harmonics in the output signal. Generally, the harmonic order is taken from 2 to 10 during calculation.

- Signal-to-Noise Ratio (SNR)

  The signal-to-noise ratio is the ratio of the effective value of the signal to the effective value of the noise. The noise mentioned here is high-frequency noise such as ADC quantization noise and 1/f noise, excluding the harmonic components of the input signal in *THD* calculation. The calculation formula is as follows.

$$\mathrm{SNR} = 20\log_{10}\left(\frac{V_{\mathrm{Signal(RMS)}}}{V_{\mathrm{Noise(RMS)}}}\right)\left(\mathrm{dB}\right) \tag{6}$$

- Signal-to-Noise and Distortion (SINAD)

  There is always distortion of the signal caused by internal errors of the ADC, *SINAD* is used to measure the ratio of the signal to the sum of harmonics and noise, indicating the overall proportion of the effective signal in the ADC output.

$$\mathrm{SINAD} = 20\log_{10}\left(\frac{V_{\mathrm{Signal(RMS)}}}{\Sigma\left(V_{\mathrm{Harmonics}}\right) + V_{\mathrm{Noise(RMS)}}}\right)\left(\mathrm{dB}\right) \tag{7}$$

- Effective Number of Bits (ENOB)

  ENOB is the effective number of bits of ADC, which represents the actual resolution of ADC and its ability to distinguish small amplitude signals. It can be directly calculated by *SINAD*.

  The above formula provides the calculation method of *ENOB* when the input signal is assigned the ADC maximum range. When the input signal is less than the maximum range, the calculation of *ENOB* is adjusted to:

$$\mathrm{ENOB} = \frac{\mathrm{SINAD}_{\mathrm{MEASURED}} - 1.76\mathrm{dB} + 20\log_{10}\left(\frac{\mathrm{Fullscale\ \ Amplitude}}{\mathrm{(Input\ \ Amplitude}}\right)}{6.02} \tag{8}$$

1.2.2.2 DC Parameters

Measurement conditions: Connect a constant DC voltage between the positive and negative terminals of the ADC input, and observe the distribution of the output digital results.

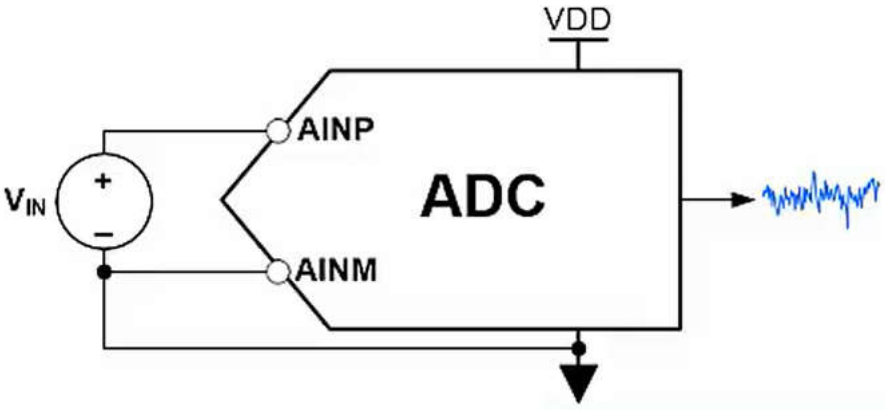

Figure 1-3. Schematic Diagram of ADC DC Test

In theory, when the quantity of the sampled data is large enough, the noise superimposed on the DC signal approximates a normal distribution. The effective value of noise is the standard deviation σ of the data sample. The probability of data distribution within the range of u-3σ~u+3σ is 99.73%, so the peak to peak value of a DC signal is approximately 6σ.

- Effective Resolution

  The effective resolution of ADC under DC input can be obtained by dividing the full-scale range (FSR) of ADC by the effective value of noise and taking the logarithm of 2. This resolution is of great significance in DC signal sampling scenarios or low-frequency signal sampling scenarios, and can reflect the effective number of ADC digital results in practical applications.

$$\text{Effective} \quad \text{resolution} = \log_2\left(\frac{\text{FSR}}{\text{V}_{\text{N, RMS}}}\right)\left(\text{bits}\right) \tag{9}$$

  The above formula represents the effective resolution calculation method when the DC input is at full scale. When the input is not at full scale, the calculation formula is modified to:

$$\text{Effective} \quad \text{resolution} = \log_2\left(\frac{\text{V}_{\text{IN}}}{\text{V}_{\text{N, RMS}}}\right)\left(\text{bits}\right) \tag{10}$$

  That is to say, the effective resolution is related to the voltage input. In theory, the larger the input voltage, the higher the DC effective resolution. Therefore, for small input signals, they are usually amplified to close to FSR through a preamplifier, to get a large effective resolution. It should be noted that the amplified noise (1/f noise and broadband band noise) should not be introduced too much.
- Noise-free resolution

  By dividing the full range of ADC by the peak to peak value of noise and taking the logarithm of the two, the noise free resolution of ADC under DC input can be obtained. It reflects the number of digits bit that can maintains stability under constant input.

$$\text{Noise} \quad \text{free} \quad \text{resolution} = \log_2\left(\frac{\text{FSR}}{\text{V}_{\text{N, PP}}}\right)\left(\text{bits}\right) \tag{11}$$

2 ADC Noise Analysis

2.1 ADC Noise Classification

The following figure shows the block diagram of an ADC system, which shows the signal chain of ADC sampling data and the necessary signal inputs for the operation of the ADC module. Each link may introduce noise to the ADC system, so the sources of ADC system noise include sensor noise, operational amplifier noise, ADC noise, power supply noise, reference voltage noise, and clock jitter noise.

The sensor noise and operational amplifier usage vary greatly depending on the application scenario, and are greatly affected by the layout. This article classifies them as input noise of the ADC. Figure 2-1introduces the sources of noise in each stage separately.

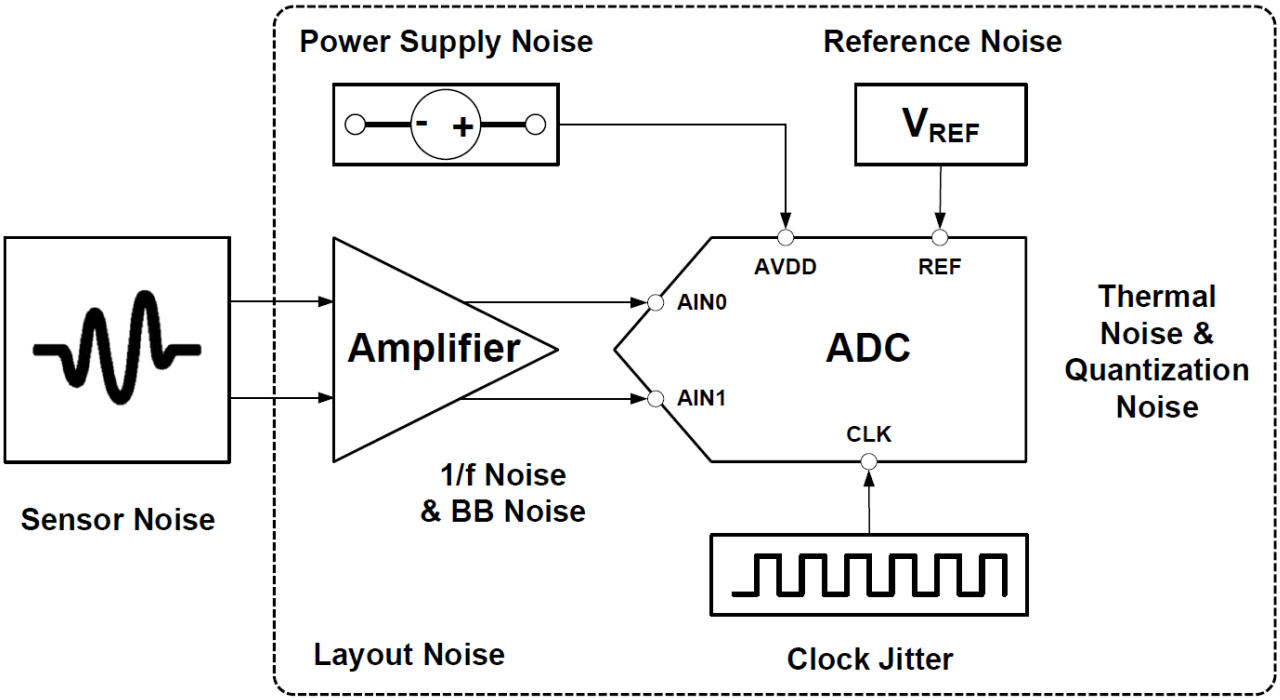

Figure 2-1. Schematic Diagram of ADC Noise Sources

2.1.1 ADC Noise

ADC internal noise includes quantization noise and thermal noise.

- Quantization noise

  The quantization noise of ADC refers to the noise caused by quantization errors between the input analog signal and the output digital signal, and its magnitude is determined by the resolution of ADC. The peak to peak value of quantization noise is 1 LSB, and the higher the resolution of ADC, the smaller the quantization error.
- Thermal noise

  Thermal noise is an inherent phenomenon in all electrical components, and it still exists even without ADC input. The sum of all noise inside the ADC, except for quantization noise, is usually referred to as thermal noise. Usually, thermal noise exhibits a Gaussian distribution, and since it is not related to quantization noise, the total noise within the ADC can be calculated using Root Sum Squares.

$$N_{ADC,\,Total} = \sqrt{N_{ADC,\,Thermal}^{2} + N_{ADC,\,Quantization}^{2}} \tag{12}$$

  According to the calculation formula of the total noise inside the ADC, it can be seen that the ADC noise is determined by the larger one of quantization noise and thermal noise. For low resolution ADCs, the quantization noise is much greater than the thermal noise, in which case, the method to reduce ADC noise is to select a smaller reference voltage to reduce quantization noise. For high-resolution ADC, due to its small LSB and low quantization noise, the full-scale range can be increased by increasing the reference voltage of the ADC, thereby reducing the proportion of thermal noise in the signal and increasing the signal-to-noise ratio.

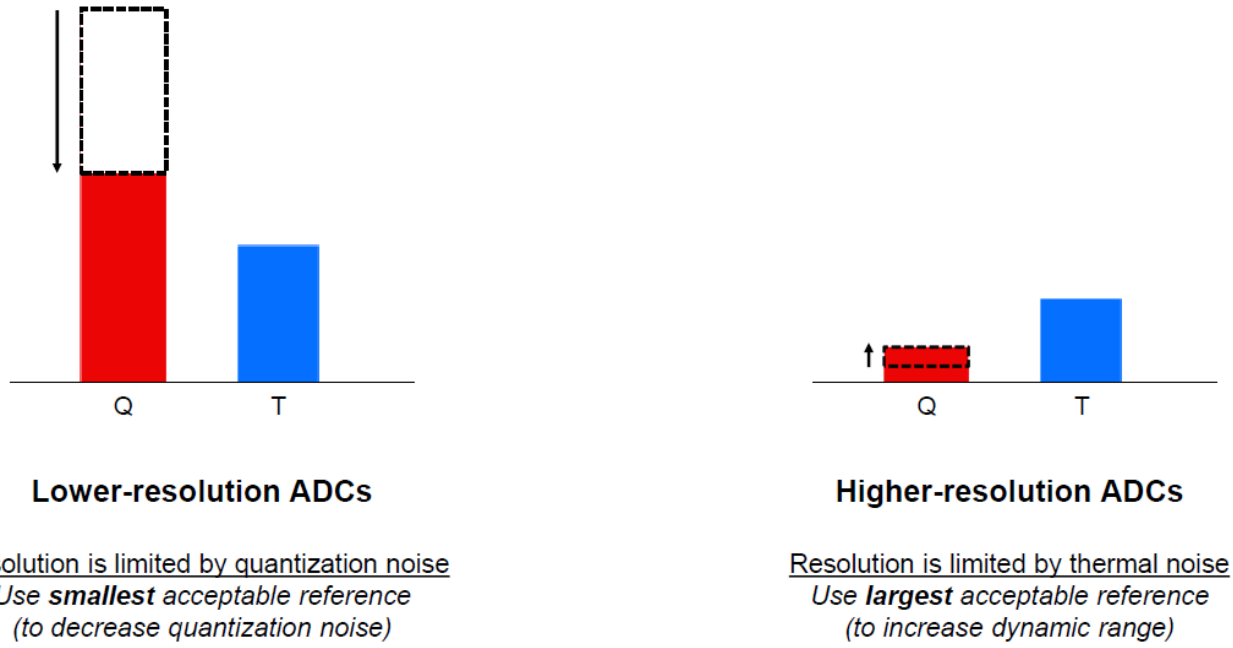

Figure 2-2. Quantization Noise and Thermal Noise of ADC With Different Resolutions

2.1.2 Reference Noise

The usual calculation formula for ADC output is

Therefore, the noise superimposed on the reference voltage will have a direct impact on the output voltage. The reference voltage noise can be transformed to the form accumulated on the output voltage:

$$\text{Output}\quad \text{Code} = V_{IN(RMS)} * \frac{2^N}{V_{REF} + V_{N,\,REF(RMS)}} \tag{13}$$

- Divide the numerator and denominator by V_{REF} to get:

$$\text{Output}\quad \text{Code} = \frac{V_{IN(RMS)}}{V_{REF}} * \frac{2^N}{1 + \frac{V_{N,\,REF(RMS)}}{V_{REF}}} \tag{14}$$

- Simplify and obtain:

$$\text{Output}\quad \text{Code} = \frac{V_{IN(RMS)} * 2^N}{V_{REF}} * \left(1 - \frac{V_{N,\,REF(RMS)}}{V_{REF}}\right) \tag{15}$$

- Separate the above formula into summation form:

$$\text{Output}\quad \text{Code} = \frac{V_{IN(RMS)} * 2^N}{V_{REF}} - \frac{V_{IN(RMS)} * 2^N * V_{N,\,REF(RMS)}}{{V_{REF}}^2} \tag{16}$$

Therefore, the voltage form of the noise superimposed on the output voltage is:

$$V_{N,\,REF} = \frac{V_{IN(RMS)}}{V_{REF}} * V_{N,\,REF(RMS)} \tag{17}$$

It is related to the ratio of input voltage to reference voltage, which is the utilization rate at full-scale. The higher the full-scale utilization of the input, the greater the reference voltage noise superimposed on the ADC output.

Considering the impact of noise on the effective resolution of ADC, as Vin in the effective resolution is reduced from Vin in the reference noise, and the internal noise of ADC is usually constant and not related to the ADC input, an increase in ADC input voltage can improve the effective resolution under the influence of ADC noise, but cannot affect the effective resolution under the influence of reference voltage noise.

One way to reduce reference voltage noise is to add an RC filtering stage before adding the reference voltage to the ADC, filtering out some high-frequency noise. On the other hand, the influence of reference voltage noise can be reduced by selecting external or internal reference voltages reasonably.

Table 2-1 provides a comparison of the advantages and disadvantages of several different reference voltages.

Table 2-1. Advantages and Disadvantages of Different ADC Reference Voltages

Reference Voltage	Advantages	Disadvantages
Internal	• Reduces PCB area + power consumption and cost • Suitable for many applications	• Higher (relative) noise • Higher (relative) drift
External	• Lower reference noise and drift • Reduce the impact of ground on power and reference voltages by directly connecting REFN and AIRN and single point grounding	• Generally higher power • Added cost and board space • REF and ADC noise are uncorrelated

2.1.3 Power Supply Noise

Due to the power supply supplying power to multiple components of the system, the operation of ADC and other circuit components (such as MCU) can cause voltage fluctuations in the power supply, resulting in power noise. This noise may affect the output results of ADC through various coupling ways. The stability of power supply can be ensured by selecting a power supply with good load regulation ability and paralleling decoupling capacitors at the output end of the power supply and the MCU power supply end.

2.1.4 ADC Input Noise

ADC input noise refers to the noise that is superimposed on the original signal during the process of collecting, amplifying, and transmission to the ADC analog input terminal. The input noise can be measured by an oscilloscope. Due to the numerous links involved in signal input, it is easy to receive various interferences. In the design of input links, reasonable layout and wiring, as well as the addition of RC filtering, can be used to minimize the interference on the input signal and filter out high-frequency noise as much as possible.

2.1.5 Clock Jitter

Clock jitter causes fluctuations in the sampling points used to sample the input signal based on the clock edge, resulting in jitter in the sampled signal value. The higher the signal frequency, the greater the jitter in the sampled value caused by clock jitter. If sampling high-frequency signals, it is necessary to select a clock source with a higher voltage swing rate to shorten the ADC sampling time and reduce the root mean square jitter introduced into the system.

2.2 How to Reduce Noise

It is generally believed that the noise in each link of the ADC system is not correlated, so the calculation method for the total noise of the ADC system is the root mean square method, which takes the sum of squares of the noise in each link first and then gets the square root.

Therefore, the noise of the ADC system depends on the link with the highest effective noise value. In order to effectively reduce system noise, it is necessary to evaluate the noise level of each link through measurement or referring data sheet, and then try to suppress the maximal noise source to reduce system noise.

2.2.1 Reducing Input Noise Through RC Filtering

RC filters are low-pass filters that can filter out high-frequency noise in the ADC input by selecting an appropriate filter bandwidth. On the one hand, it is hoped that the bandwidth will be as low as possible to cut off high-frequency noise, but on the other hand, excessive bandwidth limitations will prolong the establishment time of the sampling signal and cause input signal distortion. Therefore, it is necessary to design appropriate RC values to filter out high-frequency noise while ensuring timely response to high-frequency signals. Specific reference: Theoretical calculation method of filter RC selection

2.2.2 Layout Suggestions

- Power supply
  - Using LDO or switching power supply with good load regulation rate, and parallel filtering capacitors at the output end to provide stable power supply to the load;
  - Parallel connect a large capacitor (10uF) to the power pins of the MCU/ADC chip to filter out low-frequency noise and a small capacitor (0.1uF) to filter out high-frequency noise;
  - Isolate the digital power supply from the analog power supply, and isolate the digital ground from the analog ground to prevent high-frequency digital signals from affecting the analog signal input. At the same time, it is recommended to connect the analog ground and digital ground with a star network to minimize their mutual interference;
- Reference voltage
  - It is recommended to directly connect the negative terminal of the reference voltage to the negative terminal of the input signal, and then ground it at a single point (star network connecting);
  - When using an external reference voltage, connect small capacitors in parallel to filter out high-frequency noise on the voltage.

2.2.3 Improving Signal-to-Noise Ratio

- Signal amplification

  For ADC with fixed resolution and reference voltage, the ADC noise is fixed, and the effective resolution of the ADC can be improved by reducing the proportion of noise in the signal. The signal can be amplified to approach the full range of the ADC as closely as possible to improve effective resolution.
- Reduce the reference voltage value

  Another way to improve signal-to-noise ratio is to choose an appropriate reference voltage (close to the maximum value of the input signal), which reduces ADC noise by reducing quantization noise, and improves signal-to-noise ratio.

2.2.4 Choose a Suitable Reference Voltage Source

- For application scenarios where ratiometric sampling can be used, it is recommended to use an external voltage source as the reference voltage. In this scenario, the noise on the voltage source theoretically will not affect the digital output, and can achieve very low reference voltage noise and deviation;
- For applications with low cost requirements and do not require high accuracy, an internal reference voltage can be selected;
- For scenarios with high requirements for reference voltage accuracy, it is recommended to select external reference voltages with high precision and low temperature drift;

2.2.5 Software Methods for Reducing Noise

The most direct way to reduce signal noise by software is to increase the sampling frequency for oversampling, collect more samples than needed, and reduce noise in the signal by taking the average, thereby improving effective resolution and signal-to-noise ratio. The mean process also helps to eliminate the DNL error of the ADC transfer function. For the code lost in the ADC output due to the large DNL error, taking the average can make the code appear again, so oversampling can be used to effectively improve the dynamic range of the ADC. There are several points to note about oversampling:

- If an accuracy higher than 1LSB is required, hardware averaging cannot take the average of the actual sample size. For example, when oversampling and collecting 16 data points, you cannot directly average the 16 points on hardware, which results in a result of 12 bits resolution and a maximum quantization error of ½ LSB. It is possible to average every 4 out of 16 sampled data to obtain a 14-bit quantization result. In this case, it is then converted into a 12-bit floating-point data by software. The maximum quantization error in this case is 1/8 LSB;
- Appropriate noise can improve the noise reduction effect of hardware averaging. If the input signal with very low noise (noise peak to peak value less than 1LSB), due to the ADC resolution is only 12 bits in hardware, the output result remains constant regardless of the number of oversampled samples, and higher resolution cannot be achieved by oversampling. Therefore, an appropriate amount of noise exceeding 1LSB can improve the effectiveness of averaging;
- Usually, the more noise there is, the more samples are needed to obtain high precision through oversampling, which results in lower effective sampling frequency for actual input signal.

3 ADC Oversampling

3.1 Sampling Rate

The Nyquist theorem states that in order to reconstruct an analog input signal, the signal must be sampled at a sampling frequency f_S greater than twice the maximum frequency component of the input signal. Not complying with Nyquist's theorem can lead to frequency aliasing effects, and analog signals cannot be completely reconstructed from input samples. Therefore, for most applications, a low-pass filter is required at the ADC input to filter frequencies below half the sampling frequency. And oversampling samples the input analog signal at a rate higher than the Nyquist frequency limit, and reduces the sampling rate through extraction after sampling.

Assuming that quantization noise is superimposed on the signal in the form of white noise, its power density is uniformly distributed within the Nyquist frequency limit, and this power density is independent of the sampling frequency. When sampling at a rate higher than the Nyquist frequency limit, due to the constant quantization noise power and increased sampling bandwidth, the noise power falling within the signal bandwidth is greatly attenuated, and the signal-to-noise ratio and effective bit of the ADC are improved.

3.2 Extraction

The traditional meaning of averaging is to add *m* samples and divide the result by *m*. Average several data from ADC measurements using a low-pass filter that attenuates signal fluctuations and noise. It should be noted that normal averaging does not increase the resolution of the conversion, as the average of *m* N-bit samples are still the N-bit resolution representation. Extraction is an averaging method, which takes the average of a number less than m to get a larger resolution than N-bit. When combined with oversampling, extraction improves the resolution of the ADC, as explained in Software methods for reducing noise

3.3 Application Conditions

In order for oversampling and extraction methods to work properly, the following requirements must be met:

- There should be some noise in the input signal appropriately. The noise must be approximated as white noise with uniform power spectral density.
- The noise amplitude must be sufficient to randomly switch the input signal from one quantization bit to another, that is, the peak to peak value of noise must be at least 1 LSB. Otherwise, the input samples will have the same quantization result, and the sum and average operations will not increase the effective resolution of the ADC. For most applications, the internal thermal noise of ADCs and the input signals noise can meet this condition.

4 ADC Application Based on MSPM0

4.1 ADC Configuration of MSPM0

- Clock

Figure 4-1. ADC Clock Sysconfig Configuration

  - ADC Clock (ADCCLK)
    - SYSOSC (max 32MHz)
    - HFCLK (max 48MHz)
    - ULPCLK (max 40MHz, PD0)
  - ADC Sampling Clock (SAMPCLK) ：divided by ADCCLK
  - Conversion Clock (Conversion clock) ：ADC IP internal 80MHz crystal oscillator
    - The conversion time for 12-bit ADC data is approximately 14 conversion clock cycles
- Sampling mode

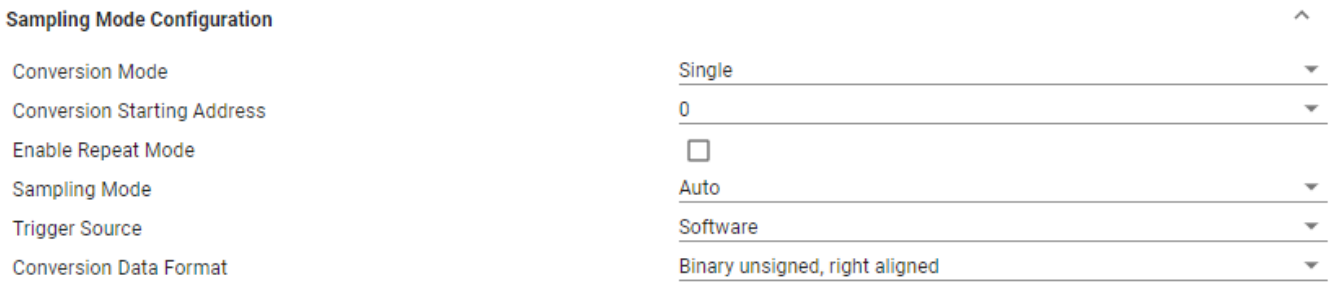

Figure 4-2. ADC Sampling Mode Sysconfig Configuration

- Conversion mode
  - *Single conversion*: Only a single point is converted during each sampling and conversion process, and the MEMCTL number used is determined by configuring the conversion start address STARTADD;
  - *Sequence conversion*: By defining the starting address STARTADD and ending address ENDADD of the MEMCTL number used for conversion, a sequence of data conversion can be defined (MEMCTL0-11 corresponds to MEMRES0-11), and ADC channels can be configured separately for each MEMCTLx;
- Enable repeat mode
  - *Non-repetitive mode*: After each round of conversion is completed, conversion enable bit (ENC) automatically resets to zero;
  - *Repetitive mode*: The conversion process will continue to be enabled until the conversion enable bit (ENC) is cleared by the software;
- Sampling trigger source
  - *Software*: Software setting CTL1.SC bit trigger sampling;
  - *Event*: Event rising edge triggering sampling;
- Sampling mode
  - *Automatic sampling*: After the sampling trigger signal is generated, the sampling signal SAMPLE is automatically raised, with a sampling time of several SAMPCLK clock cycles defined by SCOMP;
  - *Manual sampling* (only supports software triggering, does not support repetitive mode and sequence conversion, does not support hardware oversampling): The sampling signal SAMPLE is synchronized pulling up with the software triggering signal CTL1.SC. The sampling time is determined by determining the pulling up time of the SC, and triggering and sampling are completed synchronously;
- Trigger mode
  - In the repetition and sequence conversion modes, the trigger mode (TRIG) needs to be selected to determine whether the next round of conversion requires a trigger signal.

- Conversion memory configuration

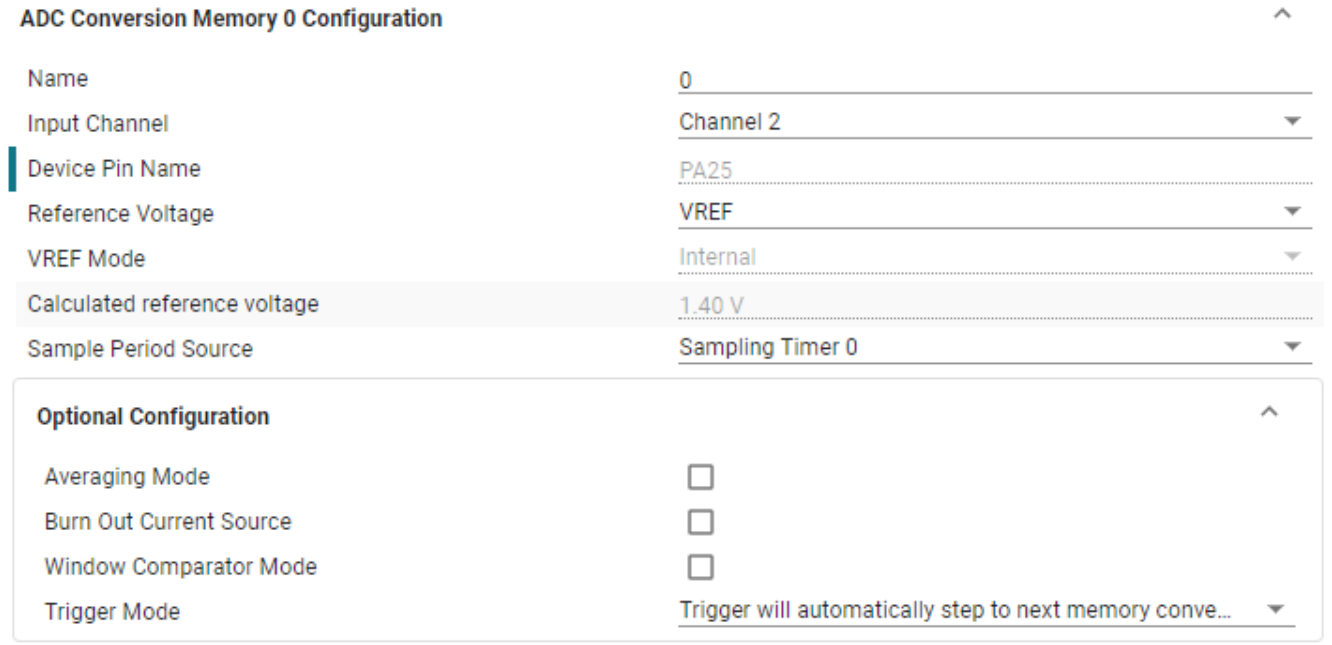

Figure 4-3. ADC Conversion Memory Sysconfig Configuration

- The amount of conversion memory that needs to be configured is determined by the MEMCTL start and end numbers defined in the conversion mode:
  - Sampling input channel
  - Reference voltage
    - VDDA：Internal power supply (3.3V)
    - VREF
      - Internal：2.5V/1.4V
      - External：0~3.3V

    Sampling Timer Source: Select the timer used for sampling time counting in automatic sampling mode
  - Others
    - Oversampling
      - sampling result multiple = number of sampling points/average denominator
    - Interrupt
      - Not using DMA: enable MEMx result loading interrupt, and read data in the interrupt after each sampling result is generated;
      - Using DMA: Enable DMA completion interrupts, and trigger DMA data transfer based on the ADC MEMx result loading, and set the amount of DMA transfer data. Once the DMA transfer is completed, enter DMA interrupts to process ADC sampling data at once.
    - CPU poll
      - CPU poll MEMx result loading register, corresponding CPU_INT RIS bit is set to 1 when ADC conversion is done and result is loaded into MEMx.
      - CPU poll ADC status register, ADC status busy bit is cleared when ADC conversion is done.

Note

For the device listed below, busy will be set after 14 ULPCLK cycles after ADC start conversion bit is set in CTL1 register. This 14 ULPCLK need to take CPU delay to wait for busy bit set, then CPU can poll the busy bit to wait for busy bit clear. Recommend to use MEMx result loading register to poll the ADC conversion done status.

MSPM0C110x, L1x0x, L111x, L134x, Lx22x, Gx10x, Gx50x, Gx51x, H321x.

4.2 ADC DC Test Based on MSPM0G3507 ADC EVM Board

To evaluate ADC performance in MSPM0 G-series and compare the precision of different reference voltage under DC input, our team designed an ADC EVM board based on MSPM0G3507 and conducted this test.

4.2.1 Software/Hardware Configuration

4.2.1.1 Hardware

The MSPM0G3507 ADC EVM board is consist of four parts:

- MCU minimum system

  MCU adopts MSPM0G3507SDGS28, which is 28pin package. In the test, PA25 is used for ADC input and PA23 is used for external reference VREF+ input, while VREF- is connected to ground through a 0R resister.

- 2.5V voltage generation

  REF7025QDGKR is a high precision series voltage references whose output voltage is 2.5V. And it could be used for ADC external reference voltage.
- 1.25V voltage generation

  REF35125QDBVR is used to generate 1.25V voltage, which could provide stable DC input for MSPM0 ADC.
- ADC input and reference voltage selection

  ADC input could be selected among 1.25V, 2.5V, VDD and GND and ADC external reference could be selected among VDD, 2.5V and 1.25V by 0R resister.

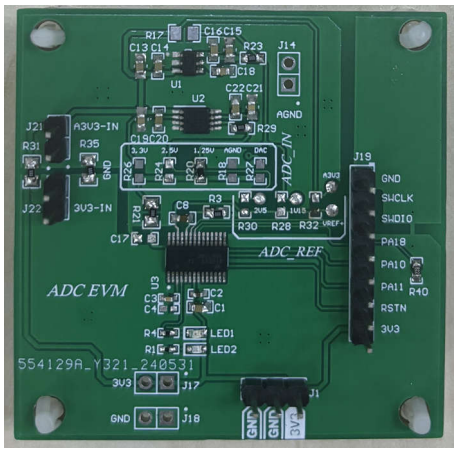

Figure 4-4. MSPM0G3507 ADC EVM

4.2.1.2 Software

The method of the test is: Tigger ADC sampling and conversion by timer event every 1ms and the ADC result is automatically transported by DMA to an array. The DMA transport size is set to 1024. Every time DMA transport finished, enter DMA interrupt to analyze ADC results and calculate some parameters (average value, peak-peak value, stand deviation, and so on). After that, repeat the progress above for 1000 times, and get the average value or maximum value of each time.

Figure 4-5 shows the basic configuration of ADC in sysconfig. Change reference voltage configuration and oversampling configuration to make comparison of different situation.

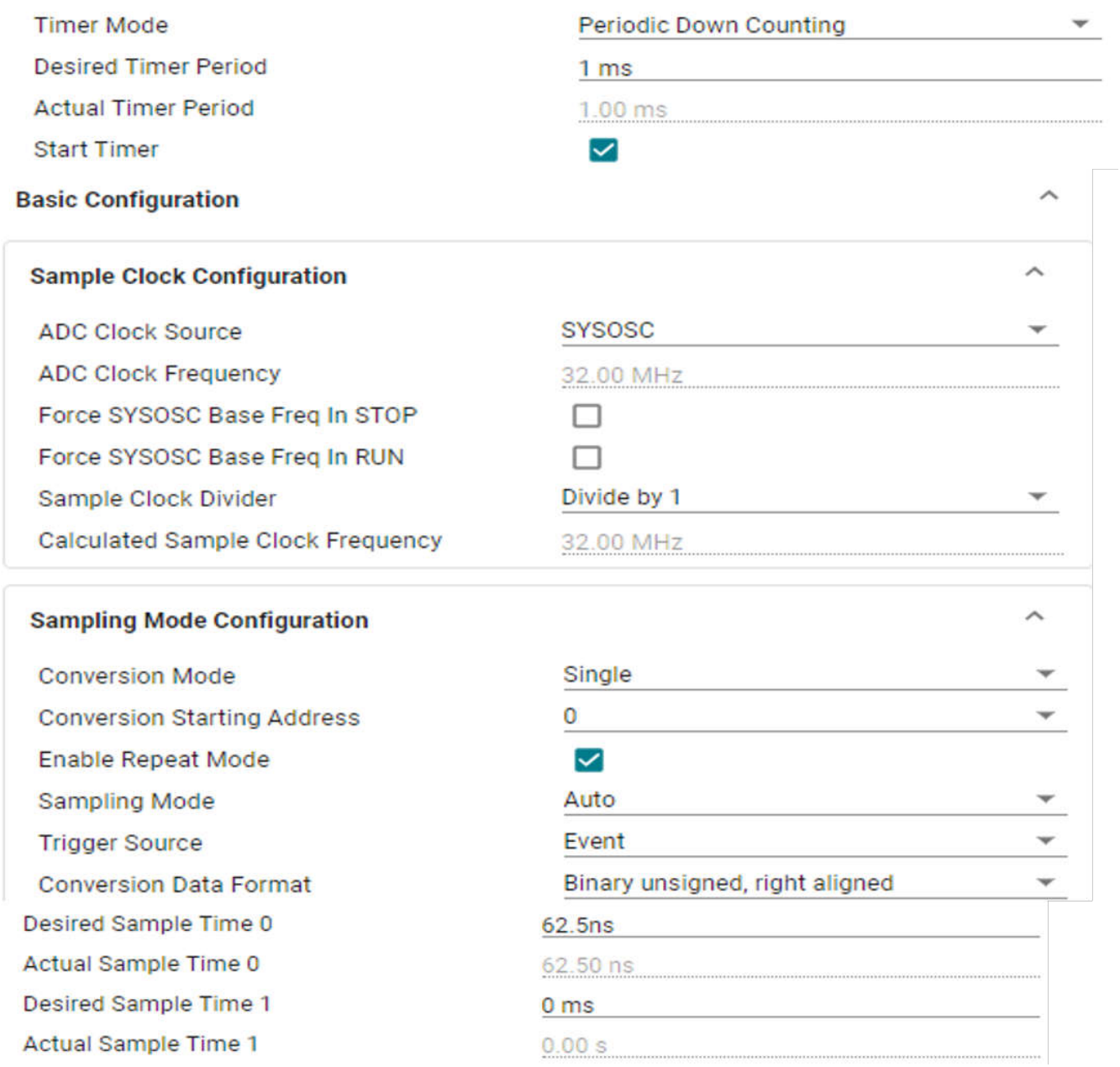

Figure 4-5. ADC DC Test Software Configuration

Here lists the explanation of some parameters that are calculated based on ADC results:

- *ttlAveAnalog* (V): the average value of analog calculation result based on ADC digital results and the formula below: $N_{ADC} = \left(2^n - 1\right) * \frac{(V_{IN} + 0.5LSB)}{V_{R+}}$
- *ttlDeltaSample* (LSB): the average value of ADC 1024 samples digital results' peak-peak value;
- *ttlMaxDelta* (LSB): the maximum value of ADC 1024 samples digital results' peak-peak value;
- *ttlAveSample* (LSB): the average value of ADC 1024 samples digital results' average value;
- *ttlStdErr* (LSB): the average value of ADC 1024 samples digital results' standard deviation;
- *NoiseStd* (V): the average value of ADC 1024 samples digital results' noise RMS value, which is equal to the samples standard deviation in voltage.
- *SNR* (1): the average of ADC 1024 samples digital results' signal-to-noise ration.

4.2.2 Test Result

Table 4-1 shows how the test results are organized. The key parameter you should pay attention to is *ttlDeltaSample* and SNR. The former represents the average level of ADC data peak-peak value (in the table it is transferred to mV unit based on reference voltage), and the latter shows ADC overall precision with the same input voltage.

Table 4-1. Test Results

Reference Voltage	Oversampling Num/Den	Peak-Peak Value based on ttlDeltaSample (mV)	Effective Resolution(bits)
Internal VDDA	1/1	10.5	10.598
	4/2	4.8	11.53
	16/4	1.6	12.935
	128/8	0	16.440
Internal 2.5V	1/1	10.4	10.526
Internal 1.4V	1/1	11.3	9.770
External VDD	1/1	11.3	11.521
External 2.5V	1/1	7.3	10.925

4.2.3 Result Analysis and Conclusion

- Analysis and conclusion

  The information can be found with the following test result:
- Observe peak-peak value based on *ttlDeltaSample* value of different reference voltage without oversampling, except “external 2.5” is much lower, others have close peak-peak voltage. The peak to peak voltage is caused by spikes on the ADC input. As it is much larger than ADC internal noise and reference noise (also larger than the peak-peak value calculated by 6*standard deviation), they have similar results in different voltage refence and it cannot reflect the performance differences of different reference voltages;
- Oversampling could effectively reduce input noise and improve ADC output SNR. The more samples oversampling collects, the larger SNR is. But it will also cause the decrease of valid sampling frequency.
- By compare effective resolution of different reference voltage, we could get the conclusion about the reference performance with the same DC input:

  External VDD 3.3V > External 2.5V > Internal VDDA > Internal 2.5V > Internal 1.4V

  – The external reference generally has better performance than internal reference, while it means more cost and PCB area.
  – When "signal noise > quantization noise", a higher reference could result in higher resolution, where signal noise includes reference noise, thermal noise and other noises added in input signal.
  – When "signal noise < quantization noise", a lower reference means lower quantization noise, and it could result in higher resolution and better accuracy. And ADC LSB determines the upper limit of ADC accuracy.
- Statement
- The above test results only reflect the results on the MSPM0G3507 ADC EVM board. The actual ADC application performance of customers are closely related to the accuracy and layout of the external reference voltage. The above results are not guaranteed to be reproducible, and better results may also be achieved in actual ADC application situation;
- The above results only reflect the ADC test results under DC input, and the effective resolution is not the same concept as ENOB, which is inconsistent with the AC parameters on the device-specifc data sheet;
- When selecting a lower precision reference voltage source, or having a poor layout and wiring, the sampling accuracy of the external reference ADC may not be as good as the internal reference.

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from October 31, 2024 to November 30, 2025 (from Revision * (October 2024) to Revision A (November 2025)) **Page**

- Added ADC CPU poll method.....11

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