Application Note

TAC5x1x and TAC5x1x-Q1 Digital Channel Mixers - Configurations and Applications

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ABSTRACT

Audio systems make use of mixing functions for applications such as channel summation to improve the ADC dynamic range, mixing multiple sources of audio inputs, and so on. This application note describes the operation of these digital mixers. The application note also shows how the mixers can be configured based on the different use cases. The configurable mixers described in this application note are available in the following ADC, DAC, and Codec families:

- TAC5212, TAC5112, TAC5211, TAC5111
- TAC5112-Q1, TAC5111-Q1
- TAA5212
- TAD5212, TAD5112
- TAD5212-Q1, TAD5112-Q1
- TAC5412-Q1, TAC5312-Q1, TAC5311-Q1
- TAA5412-Q1
- TAC5301-Q1

The TAC devices have digital mixers on both recording and playback paths, whereas the TAA devices feature these mixers only on the recording path, and TAD devices feature the mixers only on the playback path.

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Trademarks

1 Introduction

The TAC5x1x and TAC5x1x-Q1 family of audio codecs have separate signal chains for recording (through analog and or digital microphones) and for playback (through DAC) of audio signals.

Each channel of the recording path follows the signal chain shown in Figure 1-1. The mixers described in Recording Path Mixers mixes up to four signals which can be selected from two ADC channels and four PDM microphone channels through a 6-to-4 mux.

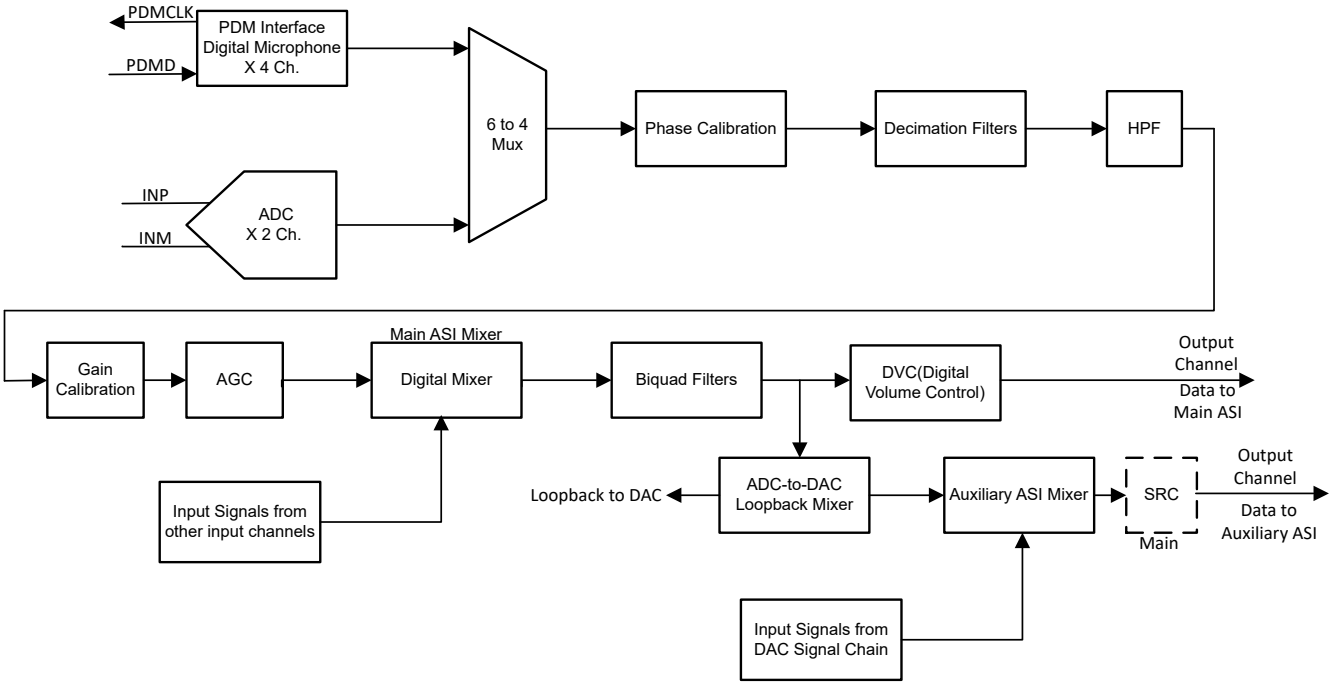

Figure 1-1. Recording Path Signal Chain

Similarly each channel of the playback path follows the signal chain shown in Figure 1-2. The mixers described in Playback Path Mixers mix up to eight digital input signals from the main Audio Serial Interface (ASI) path along with two digital signals from the auxiliary ASI path, which is further processed down the signal chain.

When the Sample Rate Converter (SRC) is bypassed in the device, the *Main ASI* refers to the Primary ASI (PASI), and the *Auxiliary ASI* refers to the Secondary ASI (SASI) bus. When the SRC is active, the *Main ASI* refers to the ASI bus which is at the faster sampling rate. For more details on the sampling rate converter, see *TAx5x1x Synchronous Sample Rate Conversion*.

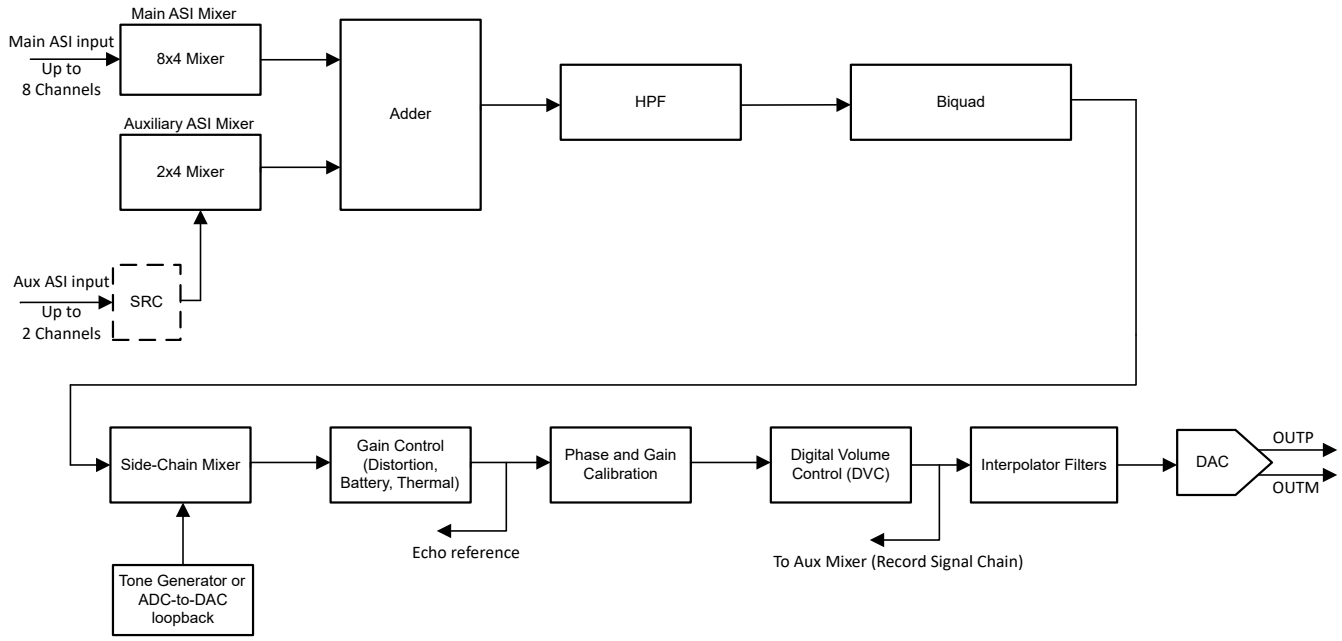

Figure 1-2. Playback Path Signal Chain

This application note describes how to configure the different mixers to get the desired signal output, and also describes the following key applications:

1. ADC Channel summation, which can be used to improve the dynamic range by 3dB, described in Application: ADC Channel Summation to Improve TAC5212 Dynamic Range.
2. Mixing the analog input signal of the TAC5412-Q1 with the digital input signal and play the resulting signal on the analog outputs, described in Application: Analog Input to Analog Output Signal Flow in TAC5412-Q1.

2 Recording Path Mixers

The recording path signal chain consists of four recording channels:

1. Channel 1 input can be from ADC or PDM path (Selected through B0_P0_R19[7])
2. Channel 2 input can be from ADC or PDM path (Selected through B0_P0_R19[6])
3. Channel 3 and 4 inputs are from PDM path

Each of these four inputs are transmitted through a signal chain, and can be mixed at multiple nodes in the signal chain and transmitted to other signal processing blocks. There are three mixers in the recording path:

1. The *Main ASI Mixer* described in Main ASI Mixer mixes four inputs (muxed from 2 ADC/4 PDM) and provides four digital outputs to the High-Pass Filter.
2. The *Auxiliary ASI Mixer* described in Auxiliary ASI Mixer which the two channels from the ADC-to-DAC loopback path along with two channels from the playback path before sending the mixed data to the Auxiliary ASI bus. (optionally through a Sample Rate Converter (SRC)).
3. The *Loopback Mixer* described in ADC-to-DAC Loopback Mixer mixes the four signals from the biquad filters, and provides two digital signal to the playback path.

2.1 Main ASI Mixer

As shown in Figure 2-1, the main ASI mixer mixes the four ADC/PDM signals from the ADC block in the recording path signal chain. and provides an output based on the mixer coefficients.

While the inputs 3 and 4 to the recording path channels are sourced from the PDM microphone path, the inputs 1 and 2 can be selected to be sourced from either the ADC or the PDM microphone, by configuring the PDM_CH1_SEL/PDM_CH2_SEL fields in the INTF_CFG4 register (B0_P0_R29).

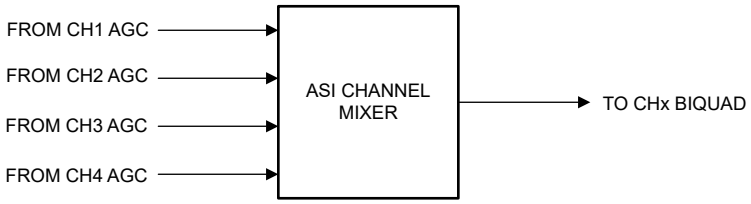

Figure 2-1. Recording Path Main ASI Mixer

The output of the main ASI mixer is then sent to the digital biquad filters in each signal path of the channel.

The mixer mixes the four digital inputs per Equation 1

$$Input\ \ for\ \ CH_x\ \ Biquad\ \ =\ \ a_x \times\ \ (ADC/PDM\ CH1)\ \ +\ \ b_x \times\ \ (ADC/PDM\ CH2)\ \ + c_x \times\ \ (PDM\ CH3)\ \ +\ \ d_x \times\ \ (PDM\ CH4) \quad (1)$$

The coefficients [a_x, b_x, c_x, d_x] are programmed as 32-bit signed values in 1.31 format into the Page 10 registers which are described in Table 2-1.

Table 2-1. Page 10 Registers for Main ASI Mixer

Register Address	Register	Register Description	Reset Value	Coefficient
0x08	ADC_MIX1_CH1_BYT1[7:0]	Digital mixer 1, ADC channel 1 coefficient byte[31:24]	0x7F	a_1
0x09	ADC_MIX1_CH1_BYT2[7:0]	Digital mixer 1, ADC channel 1 coefficient byte[23:16]	0xFF	
0x0A	ADC_MIX1_CH1_BYT3[7:0]	Digital mixer 1, ADC channel 1 coefficient byte[15:8]	0xFF	
0x0B	ADC_MIX1_CH1_BYT4[7:0]	Digital mixer 1, ADC channel 1 coefficient byte[7:0]	0xFF	

Table 2-1. Page 10 Registers for Main ASI Mixer (continued)

Register Address	Register	Register Description	Reset Value	Coefficient
0x0C	ADC_MIX1_CH2_BYT1[7:0]	Digital mixer 1, ADC channel 2 coefficient byte[31:24]	0x00	b_1
0x0D	ADC_MIX1_CH2_BYT2[7:0]	Digital mixer 1, ADC channel 2 coefficient byte[23:16]	0x00	
0x0E	ADC_MIX1_CH2_BYT3[7:0]	Digital mixer 1, ADC channel 2 coefficient byte[15:8]	0x00	
0x0F	ADC_MIX1_CH2_BYT4[7:0]	Digital mixer 1, ADC channel 2 coefficient byte[7:0]	0x00	
0x10	ADC_MIX1_CH3_BYT1[7:0]	Digital mixer 1, ADC channel 3 coefficient byte[31:24]	0x00	c_1
0x11	ADC_MIX1_CH3_BYT2[7:0]	Digital mixer 1, ADC channel 3 coefficient byte[23:16]	0x00	
0x12	ADC_MIX1_CH3_BYT3[7:0]	Digital mixer 1, ADC channel 3 coefficient byte[15:8]	0x00	
0x13	ADC_MIX1_CH3_BYT4[7:0]	Digital mixer 1, ADC channel 3 coefficient byte[7:0]	0x00	
0x14	ADC_MIX1_CH4_BYT1[7:0]	Digital mixer 1, ADC channel 4 coefficient byte[31:24]	0x00	d_1
0x15	ADC_MIX1_CH4_BYT2[7:0]	Digital mixer 1, ADC channel 4 coefficient byte[23:16]	0x00	
0x16	ADC_MIX1_CH4_BYT3[7:0]	Digital mixer 1, ADC channel 4 coefficient byte[15:8]	0x00	
0x17	ADC_MIX1_CH4_BYT4[7:0]	Digital mixer 1, ADC channel 4 coefficient byte[7:0]	0x00	
0x18	ADC_MIX2_CH1_BYT1[7:0]	Digital mixer 2, ADC channel 1 coefficient byte[31:24]	0x00	a_2
0x19	ADC_MIX2_CH1_BYT2[7:0]	Digital mixer 2, ADC channel 1 coefficient byte[23:16]	0x00	
0x1A	ADC_MIX2_CH1_BYT3[7:0]	Digital mixer 2, ADC channel 1 coefficient byte[15:8]	0x00	
0x1B	ADC_MIX2_CH1_BYT4[7:0]	Digital mixer 2, ADC channel 1 coefficient byte[7:0]	0x00	
0x1C	ADC_MIX2_CH2_BYT1[7:0]	Digital mixer 2, ADC channel 2 coefficient byte[31:24]	0x7F	b_2
0x1D	ADC_MIX2_CH2_BYT2[7:0]	Digital mixer 2, ADC channel 2 coefficient byte[23:16]	0xFF	
0x1E	ADC_MIX2_CH2_BYT3[7:0]	Digital mixer 2, ADC channel 2 coefficient byte[15:8]	0xFF	
0x1F	ADC_MIX2_CH2_BYT4[7:0]	Digital mixer 2, ADC channel 2 coefficient byte[7:0]	0xFF	
0x20	ADC_MIX2_CH3_BYT1[7:0]	Digital mixer 2, ADC channel 3 coefficient byte[31:24]	0x00	c_2
0x21	ADC_MIX2_CH3_BYT2[7:0]	Digital mixer 2, ADC channel 3 coefficient byte[23:16]	0x00	
0x22	ADC_MIX2_CH3_BYT3[7:0]	Digital mixer 2, ADC channel 3 coefficient byte[15:8]	0x00	
0x23	ADC_MIX2_CH3_BYT4[7:0]	Digital mixer 2, ADC channel 3 coefficient byte[7:0]	0x00	
0x24	ADC_MIX2_CH4_BYT1[7:0]	Digital mixer 2, ADC channel 4 coefficient byte[31:24]	0x00	d_2
0x25	ADC_MIX2_CH4_BYT2[7:0]	Digital mixer 2, ADC channel 4 coefficient byte[23:16]	0x00	
0x26	ADC_MIX2_CH4_BYT3[7:0]	Digital mixer 2, ADC channel 4 coefficient byte[15:8]	0x00	
0x27	ADC_MIX2_CH4_BYT4[7:0]	Digital mixer 2, ADC channel 4 coefficient byte[7:0]	0x00	
0x28	ADC_MIX3_CH1_BYT1[7:0]	Digital mixer 3, ADC channel 1 coefficient byte[31:24]	0x00	a_3
0x29	ADC_MIX3_CH1_BYT2[7:0]	Digital mixer 3, ADC channel 1 coefficient byte[23:16]	0x00	
0x2A	ADC_MIX3_CH1_BYT3[7:0]	Digital mixer 3, ADC channel 1 coefficient byte[15:8]	0x00	
0x2B	ADC_MIX3_CH1_BYT4[7:0]	Digital mixer 3, ADC channel 1 coefficient byte[7:0]	0x00	

Table 2-1. Page 10 Registers for Main ASI Mixer (continued)

Register Address	Register	Register Description	Reset Value	Coefficient
0x2C	ADC_MIX3_CH2_BYT1[7:0]	Digital mixer 3, ADC channel 2 coefficient byte[31:24]	0x00	b_2
0x2D	ADC_MIX3_CH2_BYT2[7:0]	Digital mixer 3, ADC channel 2 coefficient byte[23:16]	0x00	
0x2E	ADC_MIX3_CH2_BYT3[7:0]	Digital mixer 3, ADC channel 2 coefficient byte[15:8]	0x00	
0x2F	ADC_MIX3_CH2_BYT4[7:0]	Digital mixer 3, ADC channel 2 coefficient byte[7:0]	0x00	
0x30	ADC_MIX3_CH3_BYT1[7:0]	Digital mixer 3, ADC channel 3 coefficient byte[31:24]	0x7F	c_3
0x31	ADC_MIX3_CH3_BYT2[7:0]	Digital mixer 3, ADC channel 3 coefficient byte[23:16]	0xFF	
0x32	ADC_MIX3_CH3_BYT3[7:0]	Digital mixer 3, ADC channel 3 coefficient byte[15:8]	0xFF	
0x33	ADC_MIX3_CH3_BYT4[7:0]	Digital mixer 3, ADC channel 3 coefficient byte[7:0]	0xFF	
0x34	ADC_MIX3_CH4_BYT1[7:0]	Digital mixer 3, ADC channel 4 coefficient byte[31:24]	0x00	d_3
0x35	ADC_MIX3_CH4_BYT2[7:0]	Digital mixer 3, ADC channel 4 coefficient byte[23:16]	0x00	
0x36	ADC_MIX3_CH4_BYT3[7:0]	Digital mixer 3, ADC channel 4 coefficient byte[15:8]	0x00	
0x37	ADC_MIX3_CH4_BYT4[7:0]	Digital mixer 3, ADC channel 4 coefficient byte[7:0]	0x00	
0x38	ADC_MIX4_CH1_BYT1[7:0]	Digital mixer 4, ADC channel 1 coefficient byte[31:24]	0x00	a_4
0x39	ADC_MIX4_CH1_BYT2[7:0]	Digital mixer 4, ADC channel 1 coefficient byte[23:16]	0x00	
0x3A	ADC_MIX4_CH1_BYT3[7:0]	Digital mixer 4, ADC channel 1 coefficient byte[15:8]	0x00	
0x3B	ADC_MIX4_CH1_BYT4[7:0]	Digital mixer 4, ADC channel 1 coefficient byte[7:0]	0x00	
0x3C	ADC_MIX4_CH2_BYT1[7:0]	Digital mixer 4, ADC channel 2 coefficient byte[31:24]	0x00	b_4
0x3D	ADC_MIX4_CH2_BYT2[7:0]	Digital mixer 4, ADC channel 2 coefficient byte[23:16]	0x00	
0x3E	ADC_MIX4_CH2_BYT3[7:0]	Digital mixer 4, ADC channel 2 coefficient byte[15:8]	0x00	
0x3F	ADC_MIX4_CH2_BYT4[7:0]	Digital mixer 4, ADC channel 2 coefficient byte[7:0]	0x00	
0x40	ADC_MIX4_CH3_BYT1[7:0]	Digital mixer 4, ADC channel 3 coefficient byte[31:24]	0x00	c_4
0x41	ADC_MIX4_CH3_BYT2[7:0]	Digital mixer 4, ADC channel 3 coefficient byte[23:16]	0x00	
0x42	ADC_MIX4_CH3_BYT3[7:0]	Digital mixer 4, ADC channel 3 coefficient byte[15:8]	0x00	
0x43	ADC_MIX4_CH3_BYT4[7:0]	Digital mixer 4, ADC channel 3 coefficient byte[7:0]	0x00	
0x44	ADC_MIX4_CH4_BYT1[7:0]	Digital mixer 4, ADC channel 4 coefficient byte[31:24]	0x7F	d_4
0x45	ADC_MIX4_CH4_BYT2[7:0]	Digital mixer 4, ADC channel 4 coefficient byte[23:16]	0xFF	
0x46	ADC_MIX4_CH4_BYT3[7:0]	Digital mixer 4, ADC channel 4 coefficient byte[15:8]	0xFF	
0x47	ADC_MIX4_CH4_BYT4[7:0]	Digital mixer 4, ADC channel 4 coefficient byte[7:0]	0xFF	

2.1.1 Q-31 Formatting for Mixer Coefficients

The coefficients of the recording path mixers [like a_x, b_x, c_x, d_x] are programmed as 32-bit twos-complement values, each occupying four consecutive registers in the register space of the device. These mixer coefficients are in either 1.31 format with a range from –1 (0x80000000) to 0.9999999995 (0x7FFFFFFF), or 2.30 format with a range from – 2(0x80000000) to 1.9999999991 (0x7FFFFFFF). These representations are shown in Figure 2-2.

- To convert a floating point number to the corresponding Q31 format, multiply the floating point mixer coefficient by 2^{31} (for 1.31) or 2^{30} (for 2.30) and truncate to the nearest integer.
  - For example, a coefficient of 0.4 corresponds to an integer value of 858993459 in 1.31 format.
  - Similarly, a coefficient of 1.25 corresponds to an integer value of 1288490189 in 2.30 format
- For positive integers, convert directly to hexadecimal format.
- For negative integers, take the absolute value of the coefficient, convert the value to binary, negate the value, add one, and convert to hex. For example, to represent -135 in 32-bit two's complement hexadecimal format:
  - Absolute value of -135 is 0000 0000 0000 0000 0000 0000 1000 0111 in binary (or 0x00000087 in hex)
  - Negating the binary results in 1111 1111 1111 1111 1111 1111 0111 1000 in binary (or 0xFFFFFF78 in hex). This is the twos-complement representation of the negative integer.

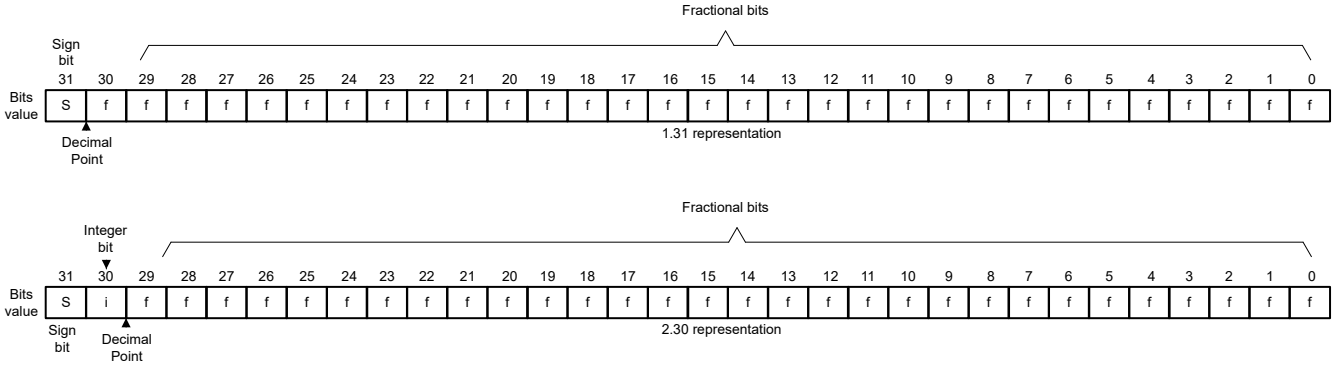

Figure 2-2. Q-31 Representation of Floating-Point Numbers (1.31/2.30)

2.1.2 Recording Path Main ASI Mixer: Example

This section describes an example implementation of the main ASI mixer on the recording path. The following sample code was executed on a TAC5112EVM-K evaluation module using a PurePath™Console 3. Four input signals are provided to the device for the main ASI mixer:

- A 1kHz, 0.2Vrms differential analog sinusoidal signal on IN1P/IN1M.
- A 1kHz, 0.5Vrms differential analog sinusoidal signal on IN2P/IN2M.
- A 100Hz, 0.1FS (Full-Scale) PDM sinusoidal tone on PDM Channel 3.
- A 5kHz, 0.2FS (Full-Scale) PDM sinusoidal tone on PDM Channel 4.

The resulting outputs on the DOUT of the Main ASI bus are captured and shown in Figure 2-3.

```
#FS refers to Full-Scale
w a0 00 00 #Page 0
w a0 01 01 #SW Reset
d 01

w a0 00 00 #Page 0
w a0 02 09 #Exit Sleep Mode with DREG and VREF Enabled
d 10

w a0 1a 30 #PASI on TDM protocol with 32-bit word length
w a0 4d 00 #VREF set to 2.75V for 2Vrms differential fullscale input
w a0 50 00 #ADC Channel 1 configured for AC-coupled differential input with 5kOhm input impedance
and audio bandwidth
w a0 55 00 #ADC Channel 2 configured for AC-coupled differential input with 5kOhm input impedance
and audio bandwidth
w a0 0a 41 #Configure GPIO1 as PDMCLK
w a0 0b 10 #Configure GPIO2 as GPI
w a0 13 12 #Source PDM CH3/CH4 data from GPIO2; CH3 on PDMCLK rising edge, CH4 on PDMCLK falling
edge
w a0 35 00 #PDMCLK = 3.072MHz

w a0 1e 20 #PASI TX Channel 1 on TDM Slot 0
w a0 1f 21 #PASI TX Channel 2 on TDM Slot 0
w a0 20 22 #PASI TX Channel 3 on TDM Slot 2
w a0 21 23 #PASI TX Channel 4 on TDM Slot 3

w a0 00 01 #Page 1
w a0 2c 20 #Enable ADC Channel Mixer


#IN1 = ADC CH1 = 0.2Vrms, 1kHz analog signal (0.1FS)
#IN2 = ADC CH2 = 0.5Vrms, 1kHz analog signal (0.25FS)
#IN3 = PDM CH3 = 0.1FS, 100Hz PDM signal (0.1FS)
#IN4 = PDM CH4 = 0.2FS, 5kHZ PDM signal (0.2FS)

w a0 00 0a #Page 10
#Configure Mixer for OUT1 = 0.3*IN1 + 0.5*IN3
w a0 08 26 66 66 66 #a1 = 0.3
w a0 0c 00 00 00 00 #b1 = 0
w a0 10 40 00 00 00 #c1 = 0.5
w a0 14 00 00 00 00 #d1 = 0

#Configure Mixer for OUT2 = 0.5*IN2 + 0.3*IN4
w a0 18 00 00 00 00 #a2 = 0
w a0 1c 40 00 00 00 #b2 = 0.4
w a0 20 00 00 00 00 #c2 = 0
w a0 24 26 66 66 66 #d2 = 0.3

#Configure Mixer for OUT3 = 0.2*IN1 + 0.5*IN2 + 0.4*IN3 + 0.3*IN4
w a0 28 19 99 99 9a #a3 = 0.2
w a0 2c 40 00 00 00 #b3 = 0.5
w a0 30 33 33 33 33 #c3 = 0.4
w a0 34 26 66 66 66 #d3 = 0.3


#Configure Mixer for OUT4 = 0.5*IN1 + 0.2*IN2 + 0.3*IN3 + 0.4*IN4
w a0 38 40 00 00 00 #a4 = 0.5
w a0 3c 19 99 99 9a #b4 = 0.2
w a0 40 26 66 66 66 #c4 = 0.3
w a0 44 33 33 33 33 #d3 = 0.4

w a0 00 00 #Page 0
```

```
w a0 76 f0 #ADC Channels 1-4 Enabled
w a0 78 80 #ADC Powered Up
```

Mixer Inputs:
IN1 – 1kHz, 0.2Vrms Sine (0.1FS analog, IN1P/M)
IN2 – 1kHz, 0.5Vrms Sine (0.25FS analog, IN2P/M)
IN3 – 100Hz Sine (0.1FS PDM CH3)
IN4 – 5kHz Sine (0.2FS PDM CH4)

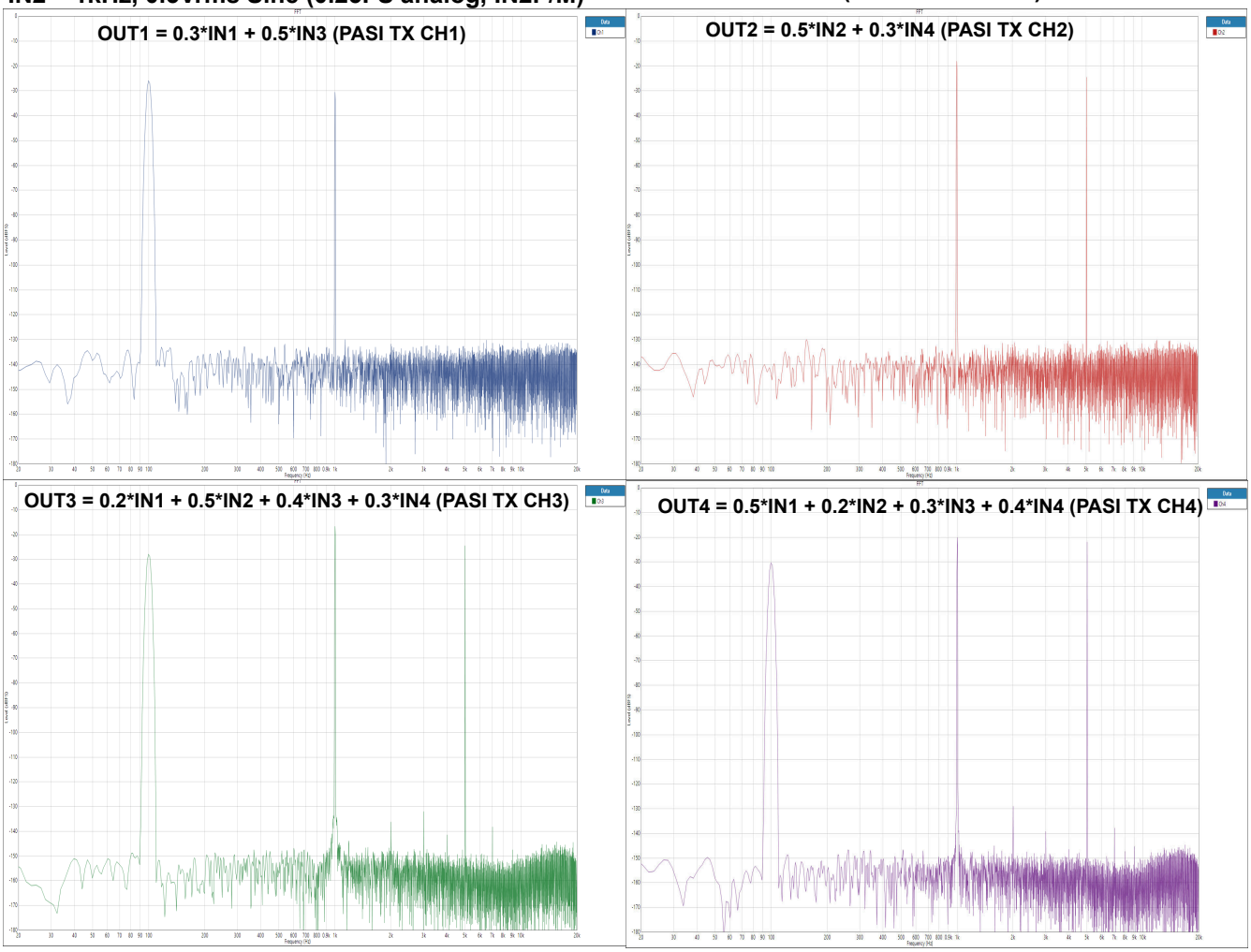

Figure 2-3. Recording Channel Outputs for Main ASI Mixer

2.2 Auxiliary ASI Mixer

The auxiliary mixer can be used when transmitting data to the auxiliary ASI's data output.

This can optionally be done through a Sample Rate Converter (SRC) when the auxiliary ASI is sampling data at a rate which is an integral sub-multiple of the sampling rate of the main ASI.

As shown in Figure 2-4, the auxiliary ASI mixer mixes the two signals from the ADC-to-DAC loopback mixer (A2D_LBx) with the output of the digital volume (DVOL) block of the CH3 and CH4 playback signal chains.

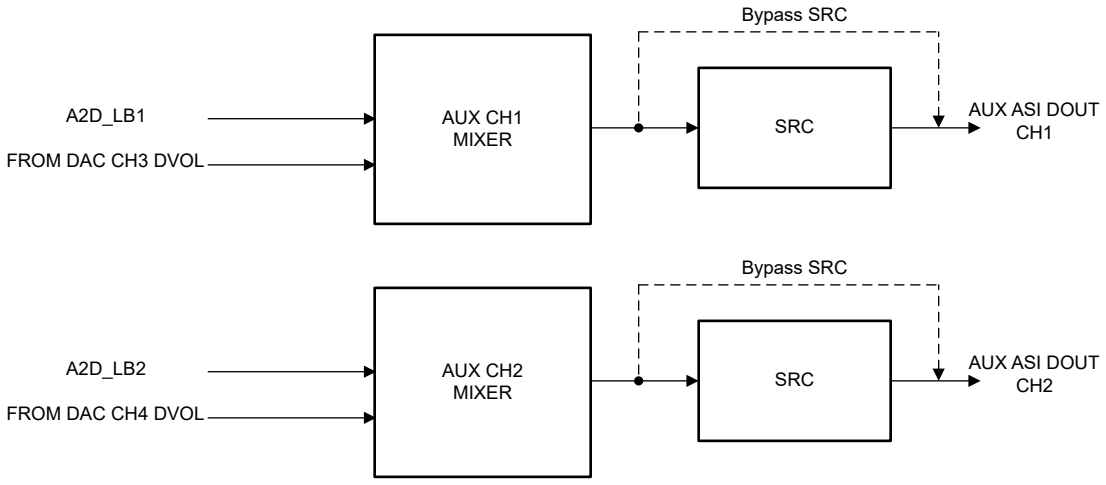

Figure 2-4. Recording Path Auxiliary ASI Mixer

The mixer then outputs this signal to the DOUT of the Auxiliary ASI bus either directly or through a Sample Rate Converter (SRC).

The auxiliary ASI mixer mixes the signals according to Equation 2

$$AUX\ ASI\ DOUT\ CH1 = x1 \times (MAIN\ ASI\ RX\ CH3) + (1 - x1) \times (A2D\ LOOPBACK\ CH1) \quad (2)$$
$$AUX\ ASI\ SDOUT\ CH2 = x2 \times (MAIN\ ASI\ RX\ CH4) + (1 - x2) \times (A2D\ LOOPBACK\ CH2)$$

The coefficients x_1 and x_2 are programmed as 32-bit signed values into the Page 11 registers which are described in Table 2-2. These coefficients are written in the 2.30 format described in Section 2.1.1.

Table 2-2. Page 11 Registers for Auxiliary ASI Mixer

Register Address	Register	Register Description	Reset Value	Coefficient
0x30	ADC_AUX_MIX_CH1_BYT1[7:0]	ADC Auxiliary Mixer CH1 coefficient byte[31:24]	0x00	x_1
0x31	ADC_AUX_MIX_CH1_BYT2[7:0]	ADC Auxiliary Mixer CH1 coefficient byte[23:16]	0x00	
0x32	ADC_AUX_MIX_CH1_BYT3[7:0]	ADC Auxiliary Mixer CH1 coefficient byte[15:8]	0x00	
0x33	ADC_AUX_MIX_CH1_BYT4[7:0]	ADC Auxiliary Mixer CH1 coefficient byte[7:0]	0x00	
0x34	ADC_AUX_MIX_CH2_BYT1[7:0]	ADC Auxiliary Mixer CH2 coefficient byte[31:24]	0x00	x_2
0x35	ADC_AUX_MIX_CH2_BYT2[7:0]	ADC Auxiliary Mixer CH2 coefficient byte[23:16]	0x00	
0x36	ADC_AUX_MIX_CH2_BYT3[7:0]	ADC Auxiliary Mixer CH2 coefficient byte[15:8]	0x00	
0x37	ADC_AUX_MIX_CH2_BYT4[7:0]	ADC Auxiliary Mixer CH2 coefficient byte[7:0]	0x00	

2.2.1 Recording Path Auxiliary ASI Mixer - Example

This section describes an example implementation of the auxiliary ASI mixer on the recording path. The following sample code was executed on a TAC5112EVM-K evaluation module using PurePath™ Console 3. Four input signals are provided to the device for the auxiliary ASI mixer:

- A 1kHz, 0.2Vrms differential analog sinusoidal signal on IN1P/IN1M.
- A 1 kHz, 0.5Vrms differential analog sinusoidal signal on IN2P/IN2M.
- A 500Hz, 0.5FS (Full-Scale) digital sinusoidal tone on PASI RX Channel 3.
- A 1.3kHz, 0.6FS (Full-Scale) PDM sinusoidal toneon PASI RX Channel 4.

Two analog input signals on the recording path, along with two digital input signals on the playback paths were used as inputs. The output of the mixer was sent on the DOUT of the Auxiliary ASI bus.

In this examples, both ASI buses were running at 48kHz, and hence the SRC was bypassed. The results are shown in Figure 2-5.

```
#FS refers to Full-Scale
w a0 00 00 #Page 0
w a0 01 01 #SW Reset
d 01

w a0 00 00 #Page 0
w a0 02 09 #Exit Sleep Mode with DREG and VREF Enabled
d 10

w a0 1a 30 #PASI in TDM protocol with 32-bit word length
w a0 4d 00 #VREF set to 2.75V for 2Vrms differential fullscale input
w a0 50 00 #ADC Channel 1 configured for AC-coupled differential input with 5kOhm input impedance
and audio bandwidth
w a0 55 00 #ADC Channel 2 configured for AC-coupled differential input with 5kOhm input impedance
and audio bandwidth

w a0 28 20 #Assign Slot 0 to RX CH1
w a0 29 21 #Assign Slot 1 to RX CH2
w a0 2a 22 #Assign Slot 2 to RX CH3
w a0 2b 23 #Assign Slot 3 to RX CH4

w a0 00 01 #Page 1
w a0 2c 30 #Enable ADC Channel Mixer, Loopback Mixer

#Default ADC Loopback mixer coefficients used
#ADC LB1 = ADC IN1 = 0.2Vrms, 1kHz analog signal (0.1FS)
#ADC LB2 = ADC IN2 = 0.5Vrms, 1kHz analog signal (0.25FS)
#DAC IN3 = 0.5FS, 500Hz signal (0.5FS)
#DAC IN4 = 0.6FS, 1.3kHz signal (0.6FS)

w a0 00 0b #Page 11
#Configure AUX Mixer for OUT1 = 0.3 * ADC LB1 + 0.7 * DAC IN3
w a0 30 2c cc cc cd #x = 0.7

#Configure AUX Mixer for OUT2 = 0.6 * ADC LB2 + 0.4 * DAC IN4
w a0 34 19 99 99 9a #x = 0.4

w a0 00 00 #Page 0
w a0 0a 10 #Configure GPIO1 as GPI
w a0 0b 10 #configure GPIO2 as GPI
w a0 0c 71 #Configure GPIO3 as SASI DOUT
w a0 11 94 #Configure GPIO1 as SASI FSYNC, GPIO2 as SASI BCLK
w a0 18 20 #Enable SASI; Same configurations as PASI

w a0 00 03 #Page 0
w a0 1e 20 #SASI Channel 1 is Channel 1 data
w a0 1f 21 #SASI Channel 2 is Channel 2 data

w a0 00 00 #Page 0
w a0 76 c3 #ADC Channels 1,2 and DAC Channels 3,4 enabled
w a0 78 c0 #ADC, DAC Powered Up
```

Mixer Inputs:
IN1 = A2D_LB1 = ADC IN1 = 1kHz, 0.2Vrms Sine (0.1FS Analog, IN1P/M)
IN2 = A2D_LB2 = ADC IN2 = 1kHz, 0.5Vrms Sine (0.25FS Analog, IN2P/M)
IN3 = DAC CH3 = 500Hz Sine (0.5FS ASI Input, PASI RX CH3)
IN4 = DAC CH4 = 1.3kHz Sine (0.6FS ASI Input, PASI RX CH4)

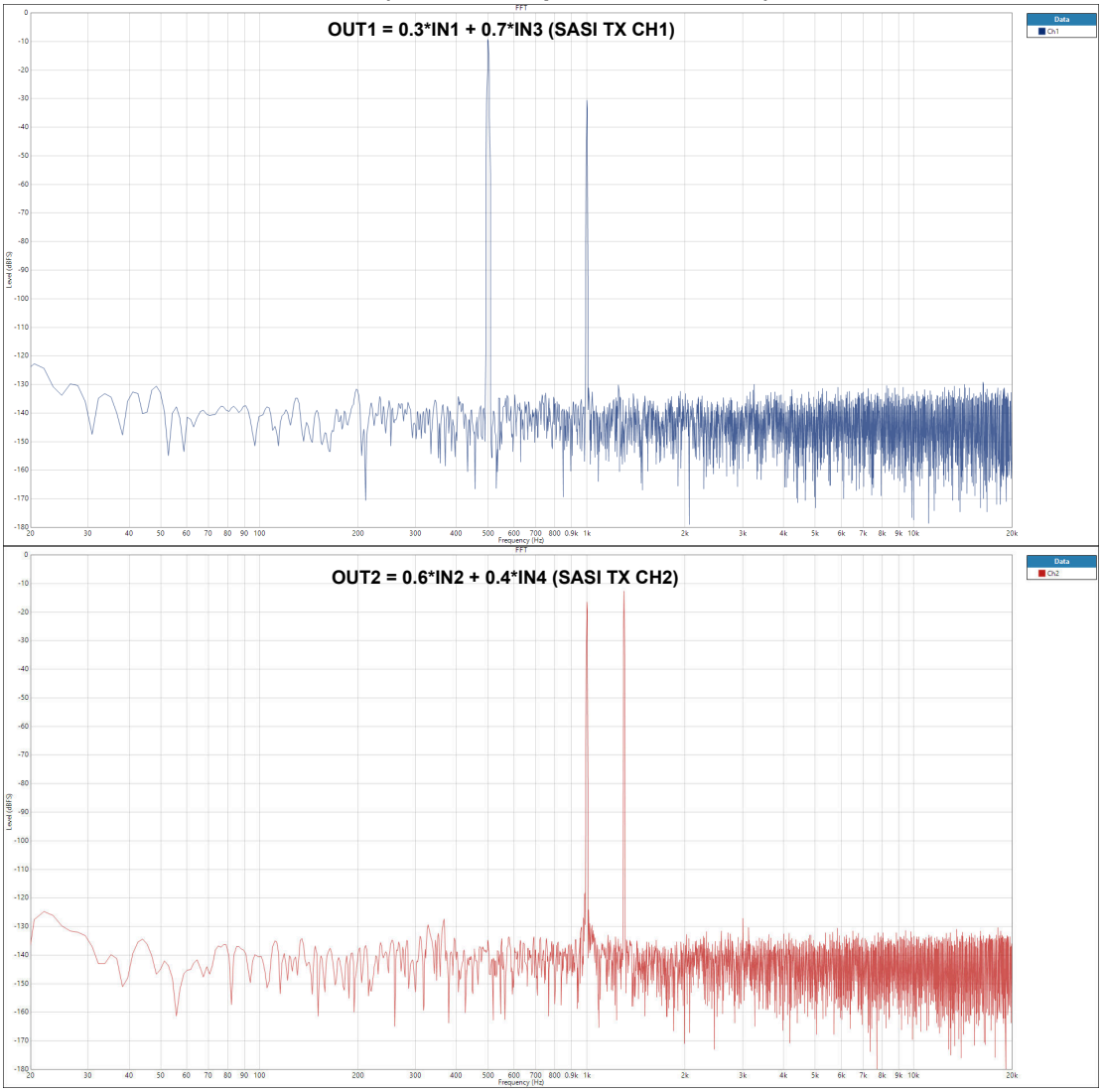

Figure 2-5. Recording Channel Outputs for Auxiliary ASI Mixer

2.3 ADC-to-DAC Loopback Mixer

As shown in Figure 2-6, the ADC-to-DAC loopback mixer mixes the output of the biquad filter path on all four recording signal chains and provides two separate digital outputs (A2D_LBx).

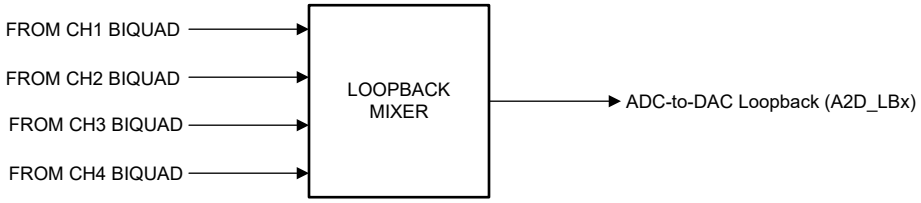

Figure 2-6. Loopback Mixer

The mixer then outputs the resulting signal into the signal chain of the playback path at the side chain mixer.

The mixing is per Equation 3.

$$A2D\_LB_x = a_x \times (CH1 \ \ signal) + b_x \times (CH2 \ \ signal) + c_x \times (CH3 \ \ signal) + d_x \times (CH4 \ \ signal) \quad (3)$$

The coefficients [a_x, b_x, c_x, d_x] are programmed as 32-bit signed values into the Page 10 registers which are described in Table 2-3. These coefficients are written in the 1.31 format described in Section 2.1.1.

Table 2-3. Page 10 Registers for Loopback Mixer

Register Address	Register	Register Description	Reset Value	Coefficient
0x48	ADC_LB_MIX1_CH1_BYT 1[7:0]	Digital loopback (ADC to DAC) mixer 1, ADC channel 1 coefficient byte[31:24]	0x7F	a_1
0x49	ADC_LB_MIX1_CH1_BYT 2[7:0]	Digital loopback (ADC to DAC) mixer 1, ADC channel 1 coefficient byte[23:16]	0xFF	
0x4A	ADC_LB_MIX1_CH1_BYT 3[7:0]	Digital loopback (ADC to DAC) mixer 1, ADC channel 1 coefficient byte[15:8]	0xFF	
0x4B	ADC_LB_MIX1_CH1_BYT 4[7:0]	Digital loopback (ADC to DAC) mixer 1, ADC channel 1 coefficient byte[7:0]	0xFF	
0x4C	ADC_LB_MIX1_CH2_BYT 1[7:0]	Digital loopback (ADC to DAC) mixer 1, ADC channel 2 coefficient byte[31:24]	0x00	b_1
0x4D	ADC_LB_MIX1_CH2_BYT 2[7:0]	Digital loopback (ADC to DAC) mixer 1, ADC channel 2 coefficient byte[23:16]	0x00	
0x4E	ADC_LB_MIX1_CH2_BYT 3[7:0]	Digital loopback (ADC to DAC) mixer 1, ADC channel 2 coefficient byte[15:8]	0x00	
0x4F	ADC_LB_MIX1_CH2_BYT 4[7:0]	Digital loopback (ADC to DAC) mixer 1, ADC channel 2 coefficient byte[7:0]	0x00	

Table 2-3. Page 10 Registers for Loopback Mixer (continued)

Register Address	Register	Register Description	Reset Value	Coefficient
0x50	ADC_LB_MIX1_CH3_BYT 1[7:0]	Digital loopback (ADC to DAC) mixer 1, ADC channel 3 coefficient byte[31:24]	0x00	c_1
0x51	ADC_LB_MIX1_CH3_BYT 2[7:0]	Digital loopback (ADC to DAC) mixer 1, ADC channel 3 coefficient byte[23:16]	0x00	
0x52	ADC_LB_MIX1_CH3_BYT 3[7:0]	Digital loopback (ADC to DAC) mixer 1, ADC channel 3 coefficient byte[15:8]	0x00	
0x53	ADC_LB_MIX1_CH3_BYT 4[7:0]	Digital loopback (ADC to DAC) mixer 1, ADC channel 3 coefficient byte[7:0]	0x00	
0x54	ADC_LB_MIX1_CH4_BYT 1[7:0]	Digital loopback (ADC to DAC) mixer 1, ADC channel 4 coefficient byte[31:24]	0x00	d_1
0x55	ADC_LB_MIX1_CH4_BYT 2[7:0]	Digital loopback (ADC to DAC) mixer 1, ADC channel 4 coefficient byte[23:16]	0x00	
0x56	ADC_LB_MIX1_CH4_BYT 3[7:0]	Digital loopback (ADC to DAC) mixer 1, ADC channel 4 coefficient byte[15:8]	0x00	
0x57	ADC_LB_MIX1_CH4_BYT 4[7:0]	Digital loopback (ADC to DAC) mixer 1, ADC channel 4 coefficient byte[7:0]	0x00	
0x58	ADC_LB_MIX2_CH1_BYT 1[7:0]	Digital loopback (ADC to DAC) mixer 2, ADC channel 1 coefficient byte[31:24]	0x00	a_2
0x59	ADC_LB_MIX2_CH1_BYT 2[7:0]	Digital loopback (ADC to DAC) mixer 2, ADC channel 1 coefficient byte[23:16]	0x00	
0x5A	ADC_LB_MIX2_CH1_BYT 3[7:0]	Digital loopback (ADC to DAC) mixer 2, ADC channel 1 coefficient byte[15:8]	0x00	
0x5B	ADC_LB_MIX2_CH1_BYT 4[7:0]	Digital loopback (ADC to DAC) mixer 2, ADC channel 1 coefficient byte[7:0]	0x00	

Table 2-3. Page 10 Registers for Loopback Mixer (continued)

Register Address	Register	Register Description	Reset Value	Coefficient
0x5C	ADC_LB_MIX2_CH2_BYT 1[7:0]	Digital loopback (ADC to DAC) mixer 2, ADC channel 2 coefficient byte[31:24]	0x7F	b_2
0x5D	ADC_LB_MIX2_CH2_BYT 2[7:0]	Digital loopback (ADC to DAC) mixer 2, ADC channel 2 coefficient byte[23:16]	0xFF	
0x5E	ADC_LB_MIX2_CH2_BYT 3[7:0]	Digital loopback (ADC to DAC) mixer 2, ADC channel 2 coefficient byte[15:8]	0xFF	
0x5F	ADC_LB_MIX2_CH2_BYT 4[7:0]	Digital loopback (ADC to DAC) mixer 2, ADC channel 2 coefficient byte[7:0]	0xFF	
0x60	ADC_LB_MIX2_CH3_BYT 1[7:0]	Digital loopback (ADC to DAC) mixer 2, ADC channel 3 coefficient byte[31:24]	0x00	c_2
0x61	ADC_LB_MIX2_CH3_BYT 2[7:0]	Digital loopback (ADC to DAC) mixer 2, ADC channel 3 coefficient byte[23:16]	0x00	
0x62	ADC_LB_MIX2_CH3_BYT 3[7:0]	Digital loopback (ADC to DAC) mixer 2, ADC channel 3 coefficient byte[15:8]	0x00	
0x63	ADC_LB_MIX2_CH3_BYT 4[7:0]	Digital loopback (ADC to DAC) mixer 2, ADC channel 3 coefficient byte[7:0]	0x00	
0x64	ADC_LB_MIX2_CH4_BYT 1[7:0]	Digital loopback (ADC to DAC) mixer 2, ADC channel 4 coefficient byte[31:24]	0x00	d_2
0x65	ADC_LB_MIX2_CH4_BYT 2[7:0]	Digital loopback (ADC to DAC) mixer 2, ADC channel 4 coefficient byte[23:16]	0x00	
0x66	ADC_LB_MIX2_CH4_BYT 3[7:0]	Digital loopback (ADC to DAC) mixer 2, ADC channel 4 coefficient byte[15:8]	0x00	
0x67	ADC_LB_MIX2_CH4_BYT 4[7:0]	Digital loopback (ADC to DAC) mixer 2, ADC channel 4 coefficient byte[7:0]	0x00	

2.4 TDM Transmission on DOUT

Figure 2-7 shows the different multiplexing for transmitting data through each ASI channel through the DOUT pin.

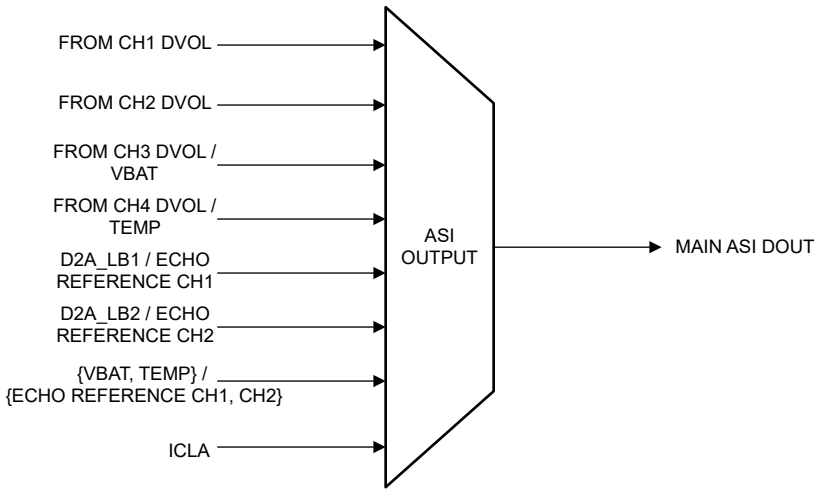

Figure 2-7. TDM Multiplexing to DOUT

The TX slots for the PASI path can be configured in the PASI_TX_CHx registers (B0_P0_R30 to B0_P0_R37). Similarly, the TX slots for the SASI path can be configured in the SASI_TX_CHx registers (B0_P3_R30 to B0_P3_R37).

3 Playback Path Mixers

There are three mixers in the recording path:

1. The *Main ASI Mixer* described in Main ASI Mixer mixes up to eight ASI inputs from the DIN pin, and provide 4 mixed outputs to the DAC signal chain.
2. The *Auxiliary Mixer* described in Auxiliary ASI Mixer mixes CH1 and CH2 inputs from the Auxiliary ASI bus (optionally through a Sample Rate Converter (SRC)). along with the output of the Main ASI mixer.
3. The *Side-Chain Mixer* described in Playback Path Side-Chain Mixer mixes four digital signals from the main ASI mixer with the two ADC-to-DAC loopback signals and the tone and chirp generator. See *Tone Generation and Application Modes of TAx5x1x Devices*.

Note that even if the mixer coefficients are 16-bit values, as mentioned in the data sheet, for a successful coefficient register transaction, the host device must write and read all four bytes starting with the most significant byte for a target coefficient register transaction. For example, to program coefficient a_1 in the main ASI mixer, the user must initiate write operation for registers 0x08, 0x09, 0x0A and 0x0B, and not just 0x0A and 0x0B. This applies for all the playback path mixer coefficients.

3.1 Main ASI Mixer

As shown in Figure 3-1, the main ASI mixer mixes up to 8 digital input signals which are given from the DIN (PASI/SASI RX channels). The RX channels 6, 7 and 8 can only be used when configured for DAC channel, so in any other configuration the corresponding mixer coefficients must be set to 0.

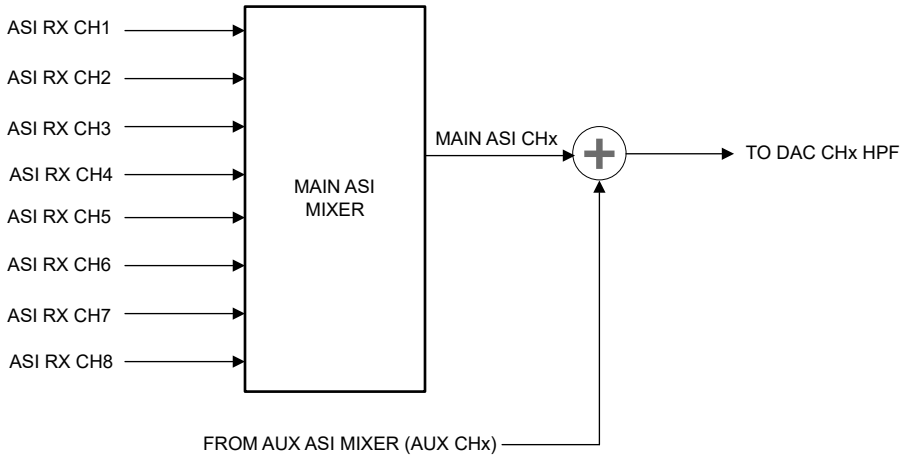

Figure 3-1. Playback Main ASI Mixer

An adder mixes the output of the Main ASI mixer along with the output of the Auxiliary ASI mixer and sends the summed signal to the digital High-Pass Filter (HPF) in the playback signal chain.

The mixing is done per this equation:

$$DAC\ CH_x\ \ HPF\ Input\ \ =\ \ a_x\ \times (MAIN\ ASI\ RX\ CH1)\ \ +\ \ b_x\ \times (MAIN\ ASI\ RX\ CH2)\ \ +\ \ c_x\ \times (MAIN\ ASI\ RX\ CH3)\ \ +\ \ d_x\ \times (MAIN\ ASI\ RX\ CH4)\ \ +\ \ e_x\ \times (MAIN\ ASI\ RX\ CH5)\ \ +f_x\ \times (MAIN\ ASI\ RX\ CH6)\ \ +g_x\ \times (MAIN\ ASI\ RX\ CH7)\ \ +h_x\ \times (MAIN\ ASI\ RX\ CH8)\ \ +\ (AUX\ ASI\ MIXER\ CH_x) \quad (4)$$

If the DACs are configured to operate in 2-channel mode (differential or mono single-ended), the device outputs the signals to the following pins:

1. CH1 (LDAC) signal to OUT1P/OUT1M analog output.
2. CH2 (RDAC) signal to OUT2P/OUT2M analog output.
3. CH3 (LDAC2) signal to DOUT (ASI TX CH5 slot).
4. CH4 (RDAC2) signal to DOUT (ASI TX CH6 slot).

If the DACs are configured to operate in 4-channel mode (stereo single-ended), the device outputs the signals to the following pins:

1. CH1 (LDAC) to OUT1P analog output.
2. CH2 (RDAC) to OUT1M analog output.
3. CH3 (LDAC2) to OUT2P analog output.
4. CH4 (RDAC2) to OUT2M analog output.

The coefficients [a_x, b_x, c_x, d_x, e_x, f_x, g_x, h_x] are programmed as 16-bit signed values in 2.14 format as described in Section 3.1.1. These coefficients can be written into the Page 17 registers which are described in Table 3-1.

Table 3-1. Page 17 Registers for Main ASI Mixer

Register Address	Register	Register Description	Reset Value	Coefficient
0x08	ASI_DIN_MIX_ASI_CH1_RDAC_MIX_BYT1[7:0]	ASI DIN MIXER, ASI CH1 to RDAC coefficient byte[15:8]	0x00	a_2
0x09	ASI_DIN_MIX_ASI_CH1_RDAC_MIX_BYT2[7:0]	ASI DIN MIXER, ASI CH1 to RDAC coefficient byte[7:0]	0x00	
0x0A	ASI_DIN_MIX_ASI_CH1_LDAC_MIX_BYT1[7:0]	ASI DIN MIXER, ASI CH1 to LDAC coefficient byte[15:8]	0x40	a_1
0x0B	ASI_DIN_MIX_ASI_CH1_LDAC_MIX_BYT2[7:0]	ASI DIN MIXER, ASI CH1 to LDAC coefficient byte[7:0]	0x00	
0x0C	ASI_DIN_MIX_ASI_CH1_RDAC2_MIX_BYT1[7:0]	ASI DIN MIXER, ASI CH1 to RDAC2 coefficient byte[15:8]	0x00	a_4
0x0D	ASI_DIN_MIX_ASI_CH1_RDAC2_MIX_BYT2[7:0]	ASI DIN MIXER, ASI CH1 to RDAC2 coefficient byte[7:0]	0x00	
0x0E	ASI_DIN_MIX_ASI_CH1_LDAC2_MIX_BYT1[7:0]	ASI DIN MIXER, ASI CH1 to LDAC2 coefficient byte[15:8]	0x00	a_3
0x0F	ASI_DIN_MIX_ASI_CH1_LDAC2_MIX_BYT2[7:0]	ASI DIN MIXER, ASI CH1 to LDAC2 coefficient byte[7:0]	0x00	
0x10	ASI_DIN_MIX_ASI_CH2_RDAC_MIX_BYT1[7:0]	ASI DIN MIXER, ASI CH2 to RDAC coefficient byte[15:8]	0x40	b_2
0x11	ASI_DIN_MIX_ASI_CH2_RDAC_MIX_BYT2[7:0]	ASI DIN MIXER, ASI CH2 to RDAC coefficient byte[7:0]	0x00	
0x12	ASI_DIN_MIX_ASI_CH2_LDAC_MIX_BYT1[7:0]	ASI DIN MIXER, ASI CH2 to LDAC coefficient byte[15:8]	0x00	b_1
0x13	ASI_DIN_MIX_ASI_CH2_LDAC_MIX_BYT2[7:0]	ASI DIN MIXER, ASI CH2 to LDAC coefficient byte[7:0]	0x00	
0x14	ASI_DIN_MIX_ASI_CH2_RDAC2_MIX_BYT1[7:0]	ASI DIN MIXER, ASI CH2 to RDAC2 coefficient byte[15:8]	0x00	b_4
0x15	ASI_DIN_MIX_ASI_CH2_RDAC2_MIX_BYT2[7:0]	ASI DIN MIXER, ASI CH2 to RDAC2 coefficient byte[7:0]	0x00	
0x16	ASI_DIN_MIX_ASI_CH2_LDAC2_MIX_BYT1[7:0]	ASI DIN MIXER, ASI CH2 to LDAC2 coefficient byte[15:8]	0x00	b_3
0x17	ASI_DIN_MIX_ASI_CH2_LDAC2_MIX_BYT2[7:0]	ASI DIN MIXER, ASI CH2 to LDAC2 coefficient byte[7:0]	0x00	
0x18	ASI_DIN_MIX_ASI_CH3_RDAC_MIX_BYT1[7:0]	ASI DIN MIXER, ASI CH3 to RDAC coefficient byte[15:8]	0x00	c_2
0x19	ASI_DIN_MIX_ASI_CH3_RDAC_MIX_BYT2[7:0]	ASI DIN MIXER, ASI CH3 to RDAC coefficient byte[7:0]	0x00	
0x1A	ASI_DIN_MIX_ASI_CH3_LDAC_MIX_BYT1[7:0]	ASI DIN MIXER, ASI CH3 to LDAC coefficient byte[15:8]	0x00	c_1
0x1B	ASI_DIN_MIX_ASI_CH3_LDAC_MIX_BYT2[7:0]	ASI DIN MIXER, ASI CH3 to LDAC coefficient byte[7:0]	0x00	
0x1C	ASI_DIN_MIX_ASI_CH3_RDAC2_MIX_BYT1[7:0]	ASI DIN MIXER, ASI CH3 to RDAC2 coefficient byte[15:8]	0x00	c_4
0x1D	ASI_DIN_MIX_ASI_CH3_RDAC2_MIX_BYT2[7:0]	ASI DIN MIXER, ASI CH3 to RDAC2 coefficient byte[7:0]	0x00	

Table 3-1. Page 17 Registers for Main ASI Mixer (continued)

Register Address	Register	Register Description	Reset Value	Coefficient
0x1E	ASI_DIN_MIX_ASI_CH3_LDAC2_MIX_BYT1[7:0]	ASI DIN MIXER, ASI CH3 to LDAC2 coefficient byte[15:8]	0x40	c_3
0x1F	ASI_DIN_MIX_ASI_CH3_LDAC2_MIX_BYT2[7:0]	ASI DIN MIXER, ASI CH3 to LDAC2 coefficient byte[7:0]	0x00	
0x20	ASI_DIN_MIX_ASI_CH4_RDAC_MIX_BYT1[7:0]	ASI DIN MIXER, ASI CH4 to RDAC coefficient byte[15:8]	0x00	d_2
0x21	ASI_DIN_MIX_ASI_CH4_RDAC_MIX_BYT2[7:0]	ASI DIN MIXER, ASI CH4 to RDAC coefficient byte[7:0]	0x00	
0x22	ASI_DIN_MIX_ASI_CH4_LDAC_MIX_BYT1[7:0]	ASI DIN MIXER, ASI CH4 to LDAC coefficient byte[15:8]	0x00	d_1
0x23	ASI_DIN_MIX_ASI_CH4_LDAC_MIX_BYT2[7:0]	ASI DIN MIXER, ASI CH4 to LDAC coefficient byte[7:0]	0x00	
0x24	ASI_DIN_MIX_ASI_CH4_RDAC2_MIX_BYT1[7:0]	ASI DIN MIXER, ASI CH4 to RDAC2 coefficient byte[15:8]	0x40	d_4
0x25	ASI_DIN_MIX_ASI_CH4_RDAC2_MIX_BYT2[7:0]	ASI DIN MIXER, ASI CH4 to RDAC2 coefficient byte[7:0]	0x00	
0x26	ASI_DIN_MIX_ASI_CH4_LDAC2_MIX_BYT1[7:0]	ASI DIN MIXER, ASI CH4 to LDAC2 coefficient byte[15:8]	0x00	d_3
0x27	ASI_DIN_MIX_ASI_CH4_LDAC2_MIX_BYT2[7:0]	ASI DIN MIXER, ASI CH4 to LDAC2 coefficient byte[7:0]	0x00	
0x28	ASI_DIN_MIX_ASI_CH5_RDAC_MIX_BYT1[7:0]	ASI DIN MIXER, ASI CH5 to RDAC coefficient byte[15:8]	0x00	e_2
0x29	ASI_DIN_MIX_ASI_CH5_RDAC_MIX_BYT2[7:0]	ASI DIN MIXER, ASI CH5 to RDAC coefficient byte[7:0]	0x00	
0x2A	ASI_DIN_MIX_ASI_CH5_LDAC_MIX_BYT1[7:0]	ASI DIN MIXER, ASI CH5 to LDAC coefficient byte[15:8]	0x00	e_1
0x2B	ASI_DIN_MIX_ASI_CH5_LDAC_MIX_BYT2[7:0]	ASI DIN MIXER, ASI CH5 to LDAC coefficient byte[7:0]	0x00	
0x2C	ASI_DIN_MIX_ASI_CH5_RDAC2_MIX_BYT1[7:0]	ASI DIN MIXER, ASI CH5 to RDAC2 coefficient byte[15:8]	0x00	e_4
0x2D	ASI_DIN_MIX_ASI_CH5_RDAC2_MIX_BYT2[7:0]	ASI DIN MIXER, ASI CH5 to RDAC2 coefficient byte[7:0]	0x00	
0x2E	ASI_DIN_MIX_ASI_CH5_LDAC2_MIX_BYT1[7:0]	ASI DIN MIXER, ASI CH5 to LDAC2 coefficient byte[15:8]	0x00	e_3
0x2F	ASI_DIN_MIX_ASI_CH5_LDAC2_MIX_BYT2[7:0]	ASI DIN MIXER, ASI CH5 to LDAC2 coefficient byte[7:0]	0x00	
0x30	ASI_DIN_MIX_ASI_CH6_RDAC_MIX_BYT1[7:0]	ASI DIN MIXER, ASI CH6 to RDAC coefficient byte[15:8]	0x00	f_2
0x31	ASI_DIN_MIX_ASI_CH6_RDAC_MIX_BYT2[7:0]	ASI DIN MIXER, ASI CH6 to RDAC coefficient byte[7:0]	0x00	
0x32	ASI_DIN_MIX_ASI_CH6_LDAC_MIX_BYT1[7:0]	ASI DIN MIXER, ASI CH6 to LDAC coefficient byte[15:8]	0x00	f_1
0x33	ASI_DIN_MIX_ASI_CH6_LDAC_MIX_BYT2[7:0]	ASI DIN MIXER, ASI CH6 to LDAC coefficient byte[7:0]	0x00	
0x34	ASI_DIN_MIX_ASI_CH6_RDAC2_MIX_BYT1[7:0]	ASI DIN MIXER, ASI CH6 to RDAC2 coefficient byte[15:8]	0x00	f_4
0x35	ASI_DIN_MIX_ASI_CH6_RDAC2_MIX_BYT2[7:0]	ASI DIN MIXER, ASI CH6 to RDAC2 coefficient byte[7:0]	0x00	
0x36	ASI_DIN_MIX_ASI_CH6_LDAC2_MIX_BYT1[7:0]	ASI DIN MIXER, ASI CH6 to LDAC2 coefficient byte[15:8]	0x00	f_3
0x37	ASI_DIN_MIX_ASI_CH6_LDAC2_MIX_BYT2[7:0]	ASI DIN MIXER, ASI CH6 to LDAC2 coefficient byte[7:0]	0x00	

Table 3-1. Page 17 Registers for Main ASI Mixer (continued)

Register Address	Register	Register Description	Reset Value	Coefficient
0x38	ASI_DIN_MIX_ASI_CH7_RDAC_MIX_BYT1[7:0]	ASI DIN MIXER, ASI CH7 to RDAC coefficient byte[15:8]	0x00	g_2
0x39	ASI_DIN_MIX_ASI_CH7_RDAC_MIX_BYT2[7:0]	ASI DIN MIXER, ASI CH7 to RDAC coefficient byte[7:0]	0x00	
0x3A	ASI_DIN_MIX_ASI_CH7_LDAC_MIX_BYT1[7:0]	ASI DIN MIXER, ASI CH7 to LDAC coefficient byte[15:8]	0x00	g_1
0x3B	ASI_DIN_MIX_ASI_CH7_LDAC_MIX_BYT2[7:0]	ASI DIN MIXER, ASI CH7 to LDAC coefficient byte[7:0]	0x00	
0x3C	ASI_DIN_MIX_ASI_CH7_RDAC2_MIX_BYT1[7:0]	ASI DIN MIXER, ASI CH7 to RDAC2 coefficient byte[15:8]	0x00	g_4
0x3D	ASI_DIN_MIX_ASI_CH7_RDAC2_MIX_BYT2[7:0]	ASI DIN MIXER, ASI CH7 to RDAC2 coefficient byte[7:0]	0x00	
0x3E	ASI_DIN_MIX_ASI_CH7_LDAC2_MIX_BYT1[7:0]	ASI DIN MIXER, ASI CH7 to LDAC2 coefficient byte[15:8]	0x00	g_3
0x3F	ASI_DIN_MIX_ASI_CH7_LDAC2_MIX_BYT2[7:0]	ASI DIN MIXER, ASI CH7 to LDAC2 coefficient byte[7:0]	0x00	
0x40	ASI_DIN_MIX_ASI_CH8_RDAC_MIX_BYT1[7:0]	ASI DIN MIXER, ASI CH8 to RDAC coefficient byte[15:8]	0x00	h_2
0x41	ASI_DIN_MIX_ASI_CH8_RDAC_MIX_BYT2[7:0]	ASI DIN MIXER, ASI CH8 to RDAC coefficient byte[7:0]	0x00	
0x42	ASI_DIN_MIX_ASI_CH8_LDAC_MIX_BYT1[7:0]	ASI DIN MIXER, ASI CH8 to LDAC coefficient byte[15:8]	0x00	h_1
0x43	ASI_DIN_MIX_ASI_CH8_LDAC_MIX_BYT2[7:0]	ASI DIN MIXER, ASI CH8 to LDAC coefficient byte[7:0]	0x00	
0x44	ASI_DIN_MIX_ASI_CH8_RDAC2_MIX_BYT1[7:0]	ASI DIN MIXER, ASI CH8 to RDAC2 coefficient byte[15:8]	0x00	h_4
0x45	ASI_DIN_MIX_ASI_CH8_RDAC2_MIX_BYT2[7:0]	ASI DIN MIXER, ASI CH8 to RDAC2 coefficient byte[7:0]	0x00	
0x46	ASI_DIN_MIX_ASI_CH8_LDAC2_MIX_BYT1[7:0]	ASI DIN MIXER, ASI CH8 to LDAC2 coefficient byte[15:8]	0x00	h_3
0x47	ASI_DIN_MIX_ASI_CH8_LDAC2_MIX_BYT2[7:0]	ASI DIN MIXER, ASI CH8 to LDAC2 coefficient byte[7:0]	0x00	

3.1.1 Q-16 Formatting for Mixer Coefficients

The coefficients of the playback path mixers [for example, a_x, b_x, c_x, d_x and so on] are programmed as 16-bit twos-complement values, each occupying four consecutive registers in the register space of the device. These mixer coefficients are in 2.14 format which is shown in Figure 3-2, with a range from –2 (0x8000) to 1.99994 (0x7FFF).

- To convert a floating point number to the corresponding Q16 format, multiply the floating point mixer coefficient by 2^{14} and truncate to the nearest integer.
- For positive integers, convert directly to hexadecimal format.
- For negative integers, take the absolute value of the coefficient, convert the value to binary, negate the value, add one, and convert to hex. For example, to represent -135 in 16-bit two's complement hexadecimal format:
  - Absolute value of -135 is 0000 0000 1000 0111 in binary (or 0x0087 in hex)
  - Negating the binary and adding 1 results in 1111 1111 0111 1001 in binary (or 0xFF79 in hex). This is the twos-complement representation of the negative integer.

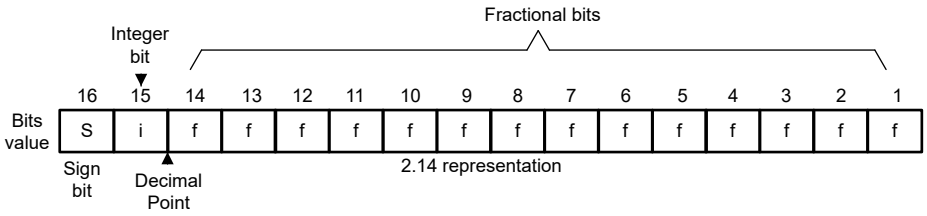

Figure 3-2. Q-16 Representation of Floating-Point Numbers (2.14)

3.1.2 Playback Path Main ASI Mixer - Example

This section describes an example implementation of the main ASI mixer on the playback path. The following sample code was executed on a TAC5112EVM-K evaluation module using PurePath™ Console 3. The test involves giving 8 digital inputs to the mixer:

1. A 150Hz, 0.1FS (Full-Scale) digital sinusoidal input on PASI_RX_CH1.
2. A 300Hz, 0.2FS (Full-Scale) digital sinusoidal input on PASI_RX_CH2.
3. A 600Hz, 0.3FS (Full-Scale) digital sinusoidal input on PASI_RX_CH3.
4. A 850Hz, 0.05FS (Full-Scale) digital sinusoidal input on PASI_RX_CH4.
5. A 1.05kHz, 0.1FS (Full-Scale) digital sinusoidal input on PASI_RX_CH5.
6. A 2.3kHz, 0.1FS (Full-Scale) digital sinusoidal input on PASI_RX_CH6.
7. A 5kHz, 0.2FS (Full-Scale) digital sinusoidal input on PASI_RX_CH7.
8. A 8.5kHz, 0.05FS (Full-Scale) digital sinusoidal input on PASI_RX_CH8.

The device outputs the 4 mixed signals as follows:

1. The CH1 and CH2 of the playback signal chain are routed through the DAC to OUT1P/M and OUT2P/M analog outputs, respectively.
2. The CH3 and CH4 of the playback signal chain are looped back into the DOUT of the main ASI bus (PASI TX Channel 5 and Channel 6).

The results captured are shown in Figure 3-3.

```
w a0 00 00 #Page 0
w a0 01 01 #SW Reset
d 01

w a0 00 00 #Page 0
w a0 02 09 #Exit Sleep Mode with DREG and VREF Enabled
d 10
w a0 1a 30 #PASI in TDM protocol with 32-bit word length
w a0 64 20 #DAC Channel 1 configured for differential output with 0.6*Vref as common mode
w a0 65 20 #DAC OUT1P configured for line out driver and audio bandwidth
w a0 66 20 #DAC OUT1M configured for line out driver and audio bandwidth
w a0 6b 20 #DAC Channel 2 configured for differential output with 0.6*Vref as common mode
w a0 6c 20 #DAC OUT2P configured for line out driver and audio bandwidth
w a0 6d 20 #DAC OUT2M configured for line out driver and audio bandwidth

w a0 22 24 #PASI TX CH5 to DAC Loopback CH1
w a0 23 25 #PASI TX CH6 to DAC Loopback CH2

w a0 26 01 #RX Offset = 1
w a0 28 20 #ASI Input 1 on PASI RX Slot 0
w a0 29 21 #ASI Input 2 on PASI RX Slot 1
w a0 2a 22 #ASI Input 3 on PASI RX Slot 2
w a0 2b 23 #ASI Input 4 on PASI RX Slot 3
w a0 2c 24 #ASI Input 5 on PASI RX Slot 4
w a0 2d 25 #ASI Input 6 on PASI RX Slot 5
w a0 2e 26 #ASI Input 7 on PASI RX Slot 6
w a0 2f 27 #ASI Input 8 on PASI RX Slot 7

w a0 00 01 #Page 1
w a0 2c 80 #Enable DAC ASI Mixer

#IN1 = ASI IN1 = 0.1FS, 150 Hz tone
#IN2 = ASI IN2 = 0.2FS, 300 Hz tone
#IN3 = ASI IN3 = 0.3FS, 600 Hz tone
#IN4 = ASI IN4 = 0.05FS, 850 Hz tone
```

```
#IN5 = ASI IN5 = 0.1FS, 1.05kHz tone
#IN6 = ASI IN6 = 0.1FS, 2.3kHz tone
#IN7 = ASI IN7 = 0.2FS, 5kHz tone
#IN8 = ASI IN8 = 0.05FS, 8.5kHz tone
#No signal on AUX ASI, so 0 signal from AUX mixer output added to main ASI mixer output


#DAC Signal Chain Channel 1 (OUT1P/M) OUT1 = 1.5*IN1 - 1.5IN3
#DAC Signal Chain Channel 2 (OUT2P/M) OUT2 = IN2 + 2*IN4
#DAC Signal Chain Channel 3 (ASI Input Loopback1) OUT3 = IN5 - 2*IN7
#DAC Signal Chain Channel 4 (ASI Input Loopback2) OUT4 = 2IN6 + IN8

w a0 00 11 #Page 17
w a0 08 00 00 60 00 #a1 = 1.5, a2 = 0
w a0 0c 00 00 00 00 #a3 = 0, a4 = 0
w a0 10 40 00 00 00 #b1 = 0, b2 = 1
w a0 14 00 00 00 00 #b3 = 0, b4 = 0
w a0 18 00 00 a0 00 #c1 = -1.5, c2 = 0
w a0 1c 00 00 00 00 #c3 = 0, c4 = 0
w a0 20 7f ff 00 00 #d1 = 0, d2 = 2
w a0 24 00 00 00 00 #d3 = 0, d4 = 0
w a0 28 00 00 00 00 #e1 = 0, e2 = 0
w a0 2c 00 00 40 00 #e3 = 1, e4 = 0
w a0 30 00 00 00 00 #f1 = 0, f2 = 0
w a0 34 7f ff 00 00 #f3 = 0, f4 = 2
w a0 38 00 00 00 00 #g1 = 0, g2 = 0
w a0 3c 00 00 80 00 #g3 = -2, g4 = 0
w a0 40 00 00 00 00 #h1 = 0, h2 = 0
w a0 44 40 00 00 00 #h3 = 0, h4 = 1

w a0 00 00 #Page 0
w a0 76 0f #Output Channels 1-4 enabled
w a0 78 40 #DAC Powered Up
```

Mixer Inputs:

IN1 = 150Hz Sine (0.1FS ASI Input, PASI RX CH1)
IN2 = 300Hz Sine (0.2FS ASI Input, PASI RX CH2)
IN3 = 600Hz Sine (0.3FS ASI Input, PASI RX CH3)
IN4 = 850Hz Sine (0.05FS ASI Input, PASI RX CH4)
IN5 = 1.05kHz Sine (0.1FS ASI input, PASI RX CH5)
IN6 = 2.3kHz Sine (0.1FS ASI Input, PASI RX CH6)
IN7 = 5kHz Sine (0.2FS ASI Input, PASI RX CH7)
IN8 = 8.5kHz Sine (0.05FS ASI input, PASI RX CH8)

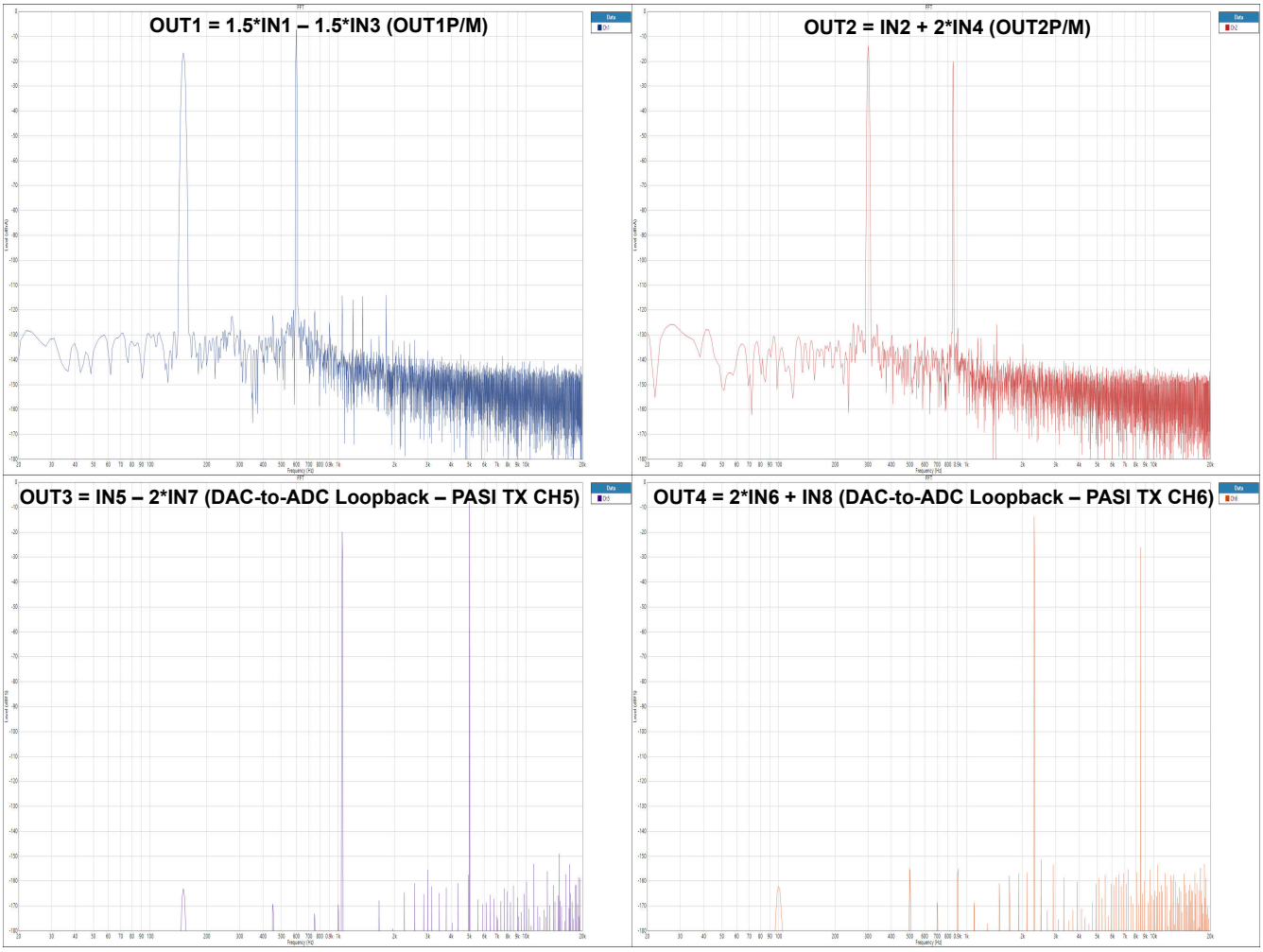

Figure 3-3. Playback Channel Outputs for Main ASI Mixer

3.2 Auxiliary ASI Mixer

The block diagram for the auxiliary ASI mixer is shown in Figure 3-4.

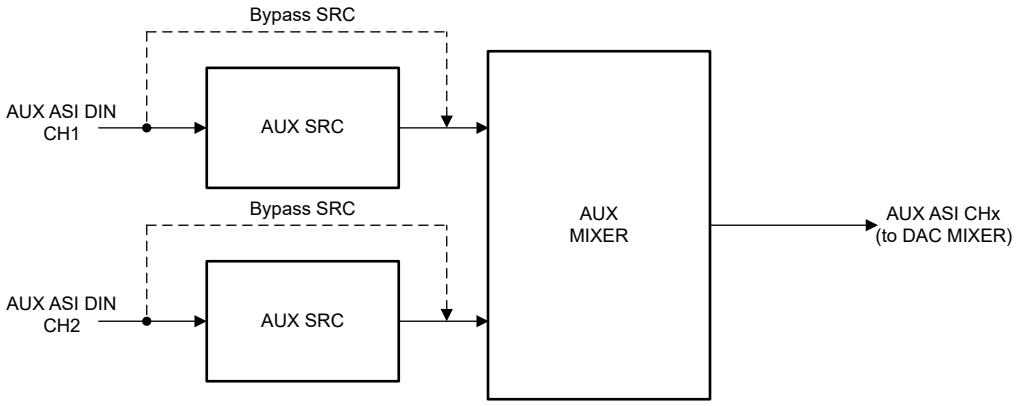

Figure 3-4. Playback Auxiliary ASI Mixer

As indicated in the block diagram, the auxiliary mixer takes 2 digital inputs from the DIN of the auxiliary ASI bus and mixes them per Equation 5.

$$AUX\ CH_x\ \ OUTPUT\ \ = \ \ a_x \times AUX\ ASI\ IN1\ \ + b_x\ \ \times AUX\ ASI\ IN2 \tag{5}$$

This signal is then added to the output of the main ASI mixer and then sent to the digital HPF block of the playback signal chain as shown in Figure 3-1. The Sample Rate Converter (SRC) can either be enabled op bypassed based on the sampling rate of the main and auxiliary ASI buses.

The coefficients [a_x, b_x] can be programmed as 16-bit signed values into the Page 17 registers which are described in Table 3-2. These coefficients are written in the 2.14 format described in Section 3.1.1.

Table 3-2. Page 17 Registers for Auxiliary ASI Mixer

Register Address	Register	Register Description	Reset Value	Coefficient
0x48	ASI_DIN_MIX_ASI_AUX_CH1_RDAC_MIX_BYT1[7:0]	ASI DIN MIXER, ASI AUX_CH1 to RDAC coefficient byte[15:8]	0x00	a_2
0x49	ASI_DIN_MIX_ASI_AUX_CH1_RDAC_MIX_BYT2[7:0]	ASI DIN MIXER, ASI AUX_CH1 to RDAC coefficient byte[7:0]	0x00	
0x4A	ASI_DIN_MIX_ASI_AUX_CH1_LDAC_MIX_BYT1[7:0]	ASI DIN MIXER, ASI AUX_CH1 to LDAC coefficient byte[15:8]	0x40	a_1
0x4B	ASI_DIN_MIX_ASI_AUX_CH1_LDAC_MIX_BYT2[7:0]	ASI DIN MIXER, ASI AUX_CH1 to LDAC coefficient byte[7:0]	0x00	
0x4C	ASI_DIN_MIX_ASI_AUX_CH1_RDAC2_MIX_BYT1[7:0]	ASI DIN MIXER, ASI AUX_CH1 to RDAC2 coefficient byte[15:8]	0x00	a_4
0x4D	ASI_DIN_MIX_ASI_AUX_CH1_RDAC2_MIX_BYT2[7:0]	ASI DIN MIXER, ASI AUX_CH1 to RDAC2 coefficient byte[7:0]	0x00	
0x4E	ASI_DIN_MIX_ASI_AUX_CH1_LDAC2_MIX_BYT1[7:0]	ASI DIN MIXER, ASI AUX_CH1 to LDAC2 coefficient byte[15:8]	0x40	a_3
0x4F	ASI_DIN_MIX_ASI_AUX_CH1_LDAC2_MIX_BYT2[7:0]	ASI DIN MIXER, ASI AUX_CH1 to LDAC2 coefficient byte[7:0]	0x00	

Table 3-2. Page 17 Registers for Auxiliary ASI Mixer (continued)

Register Address	Register	Register Description	Reset Value	Coefficient
0x50	ASI_DIN_MIX_ASI_AUX_CH2_RDAC_MIX_BYT1[7:0]	ASI DIN MIXER, ASI AUX_CH2 to RDAC coefficient byte[15:8]	0x40	b_2
0x51	ASI_DIN_MIX_ASI_AUX_CH2_RDAC_MIX_BYT2[7:0]	ASI DIN MIXER, ASI AUX_CH2 to RDAC coefficient byte[7:0]	0x00	
0x52	ASI_DIN_MIX_ASI_AUX_CH2_LDAC_MIX_BYT1[7:0]	ASI DIN MIXER, ASI AUX_CH2 to LDAC coefficient byte[15:8]	0x00	b_1
0x53	ASI_DIN_MIX_ASI_AUX_CH2_LDAC_MIX_BYT2[7:0]	ASI DIN MIXER, ASI AUX_CH2 to LDAC coefficient byte[7:0]	0x00	
0x54	ASI_DIN_MIX_ASI_AUX_CH2_RDAC2_MIX_BYT1[7:0]	ASI DIN MIXER, ASI AUX_CH2 to RDAC2 coefficient byte[15:8]	0x40	b_4
0x55	ASI_DIN_MIX_ASI_AUX_CH2_RDAC2_MIX_BYT2[7:0]	ASI DIN MIXER, ASI AUX_CH2 to RDAC2 coefficient byte[7:0]	0x00	
0x56	ASI_DIN_MIX_ASI_AUX_CH2_LDAC2_MIX_BYT1[7:0]	ASI DIN MIXER, ASI AUX_CH2 to LDAC2 coefficient byte[15:8]	0x00	b_3
0x57	ASI_DIN_MIX_ASI_AUX_CH2_LDAC2_MIX_BYT2[7:0]	ASI DIN MIXER, ASI AUX_CH2 to LDAC2 coefficient byte[7:0]	0x00	

3.2.1 Playback Path Auxiliary ASI Mixer - Example

This section describes an example implementation of the auxiliary ASI mixer on the recording path. The following sample code was executed on a TAC5112EVM-K evaluation module using PurePath™ Console 3. The test involves giving 4 digital inputs to the mixer:

1. A 1.5kHz, 0.4FS (Full-Scale) digital sinusoidal input on PASI_RX_CH1 at 48kHz sampling rate.
2. A 3.3kHz, 0.4FS (Full-Scale) digital sinusoidal input on PASI_RX_CH2 at 48kHz sampling rate.
3. A 100Hz, 0.5FS (Full-Scale) digital sinusoidal input on SASI_RX_CH1 at 16kHz sampling rate.
4. A 900Hz, 0.6FS (Full-Scale) digital sinusoidal input on SASI_RX_CH2 at 16kHz sampling rate.

The device outputs the 4 mixed signals as follows:

1. The CH1 and CH2 of the playback signal chain are routed through the DAC to OUT1P/M and OUT2P/M analog outputs, respectively.
2. The CH3 and CH4 of the playback signal chain are looped back into the DOUT of the main ASI bus (PASI TX Channel 5 and Channel 6).

Since PASI bus was running at 48kHz and SASI bus at 16kHz, the SRC is enabled, and the PASI is considered the main ASI bus, while the SASI is considered the auxiliary ASI bus.

The results are shown in Figure 3-5.

```
w a0 00 00 #Page 0
w a0 01 01 #SW Reset
d 01

w a0 00 00 #Page 0
w a0 02 09 #Exit Sleep Mode with DREG and VREF Enabled
d 10
w a0 1a 30 #PASI in TDM protocol with 32-bit word length
w a0 64 20 #DAC Channel 1 configured for differential output with 0.6*Vref as common mode
w a0 65 20 #DAC OUT1P configured for line out driver and audio bandwidth
w a0 66 20 #DAC OUT1M configured for line out driver and audio bandwidth
w a0 6b 20 #DAC Channel 2 configured for differential output with 0.6*Vref as common mode
w a0 6c 20 #DAC OUT2P configured for line out driver and audio bandwidth
w a0 6d 20 #DAC OUT2M configured for line out driver and audio bandwidth
```

```
w a0 0a 10 #Configure GPIO1 as GPI
w a0 0b 10 #Configure GPIO2 as GPI
w a0 0c 71 #Configure GPIO3 as SASI DOUT
w a0 0d 02 #Configure GPI1 as GPI
w a0 11 94 #Configure GPIO1 as SASI FSYNC, GPIO2 as SASI BCLK
w a0 12 60 #Select GPI1 as SASI DIN
w a0 18 00 #Enable SASI


w a0 22 24 #PASI TX CH5 to DAC Loopback CH1
w a0 23 25 #PASI TX CH6 to DAC Loopback CH2

w a0 26 01 #RX Offset = 1
w a0 28 20 #PASI RX CH1 to DAC CH1
w a0 29 21 #PASI RX CH2 to DAC CH2

w a0 00 03 #Page 3
w a0 28 20 #SASI RX CH1 to DAC CH1
w a0 29 21 #SASI RX CH2 to DAC CH2


w a0 00 01 #Page 1
w a0 17 80 #Enable SRC
w a0 2c 80 #Enable DAC ASI Mixer

#DAC AUX Mixer Inputs
#IN1 = Main ASI IN1 - 1.5kHz, 0.4FS signal tone (0.4FS)
#IN2 = Main ASI IN2 - 3.3kHz, 0.4FS signal tone (0.4FS)
#IN3 = Aux ASI IN1 - 100Hz, 0.5FS signal tone (0.4FS)
#IN4 = Aux ASI IN2 - 900Hz, 0.6FS signal tone (0.4FS)

#DAC Signal Chain OUT1 =  0.5*IN1 + 0.25*IN2 + 0.2*IN3 + 0.33*IN4
#DAC Signal Chain OUT2 =  0.2*IN1 + 0.5*IN2 + 0.4*IN3 + 0.5*IN4
#DAC Signal Chain OUT3 =  0.8*IN2 + 1.1*IN3
#DAC Signal Chain OUT4 =  1.25*IN1 + 0.5*IN4

w a0 00 11 #Page 17
#Main ASI Mixer Coefficients
w a0 08 0c cd 20 00 #a1 = 0.5, a2 = 0.2
w a0 0c 50 00 00 00 #a3 = 0, a4 = 1.25
w a0 10 20 00 10 00 #b1 = 0.25, b2 = 0.5
w a0 14 00 00 33 33 #b3 = 0.8, b4 = 0
w a0 18 00 00 00 00 #c1 = 0, c2 = 0
w a0 1c 00 00 00 00 #c3 = 0, c4 = 0
w a0 20 00 00 00 00 #d1 = 0, d2 = 0
w a0 24 00 00 00 00 #d3 = 0, d4 = 0


#Aux ASI Mixer Coefficients
w a0 48 19 9a 0c cd #a1 = 0.2, a2 = 0.4
w a0 4c 00 00 46 66 #a3 = 1.1, a4 = 0
w a0 50 20 00 15 1f #b1 = 0.33, b2 = 0.5
w a0 54 20 00 00 00 #b3 = 0, b4 = 0.5



w a0 00 00 #Page 0
w a0 76 0f #DAC Channels 1-4 enabled
w a0 78 40 #DAC Powered Up
```

Mixer Inputs:
IN1 = 1.5kHz Sine (0.4FS ASI Input, PASI RX CH1)
IN2 = 3.3kHz Sine (0.4FS ASI Input, PASI RX CH2)
IN3 = 100Hz Sine (0.5FS ASI input, SASI RX CH1)
IN4 = 900Hz Sine (0.6FS ASI Input, SASI RX CH2)

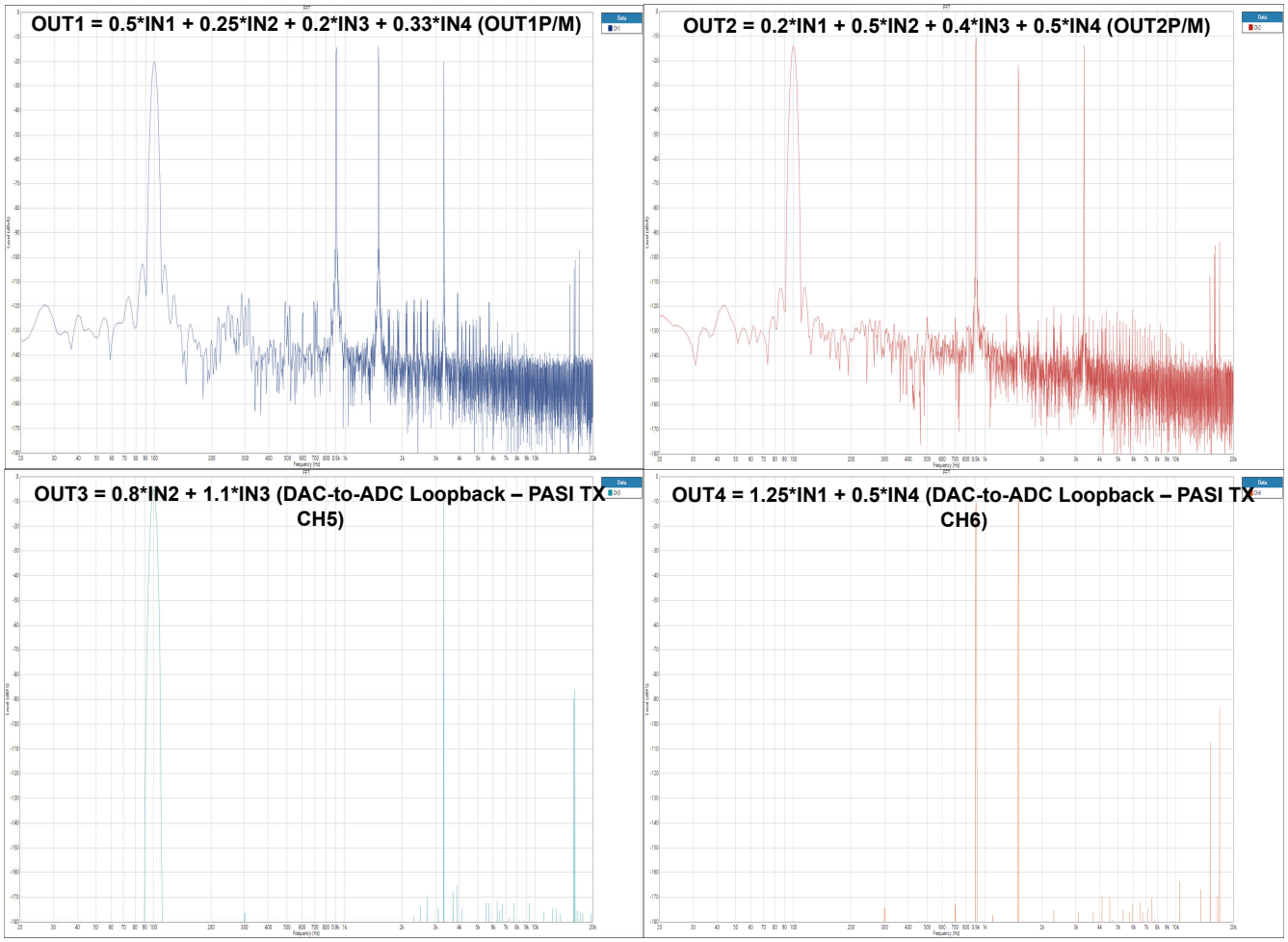

Figure 3-5. Playback Channel Outputs for Auxiliary ASI Mixer

3.3 Playback Path Side-Chain Mixer

A shown in Figure 3-6, the Side-Chain (SC) mixer mixes the following signals:

1. The output of the digital biquad filters from 4 playback channel signal chain.
2. The output of the two ADC-to-DAC loopback mixers (A2D_LBx)
3. The in-built signal generators SG1 and SG2.

As shown in *Tone Generation and Application Modes of TAx5x1x Devices*, the output amplitude of the signal generators is decided by the respective side-chain mixer coefficients. Programming these specific coefficients above 1 results in data overflow and saturation.

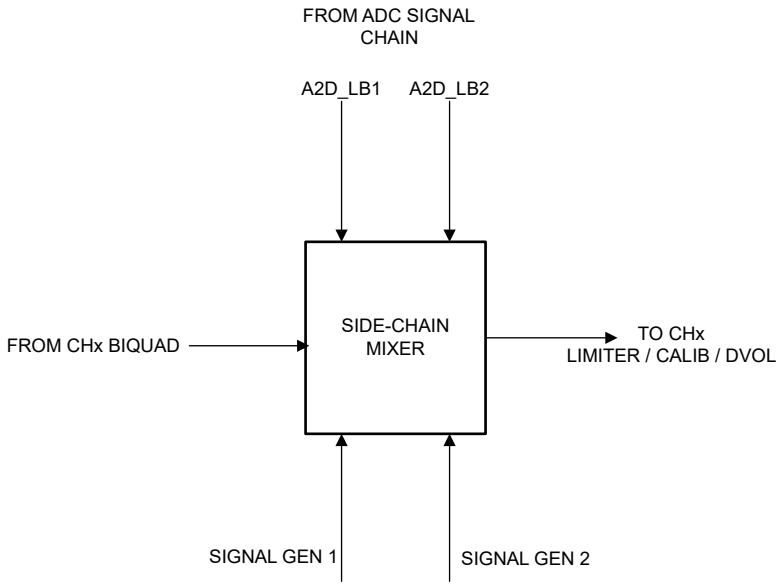

Figure 3-6. Side-Chain Mixer

The output of the SC mixer is sent to the channel limiter/claibration/digital volume control block in the signal chain.

The coefficients [a_x, b_x, c_x, d_x] are programmed as 16-bit integers into the Page 17 registers which are described in Table 3-3. These coefficients are written in the 2.14 format described in Section 3.1.1.

Table 3-3. Page 17 Registers for SC Mixer

Register Address	Register	Register Description	Reset Value
0x58	SC_DAC_MIX_ADCLB_CH1_RDAC_MIX_BYT1[7:0]	SC DAC MIXER, ADC Loopback CH1 to RDAC coefficient byte[15:8]	0x00
0x59	SC_DAC_MIX_ADCLB_CH1_RDAC_MIX_BYT2[7:0]	SC DAC MIXER, ADC Loopback CH1 to RDAC coefficient byte[7:0]	0x00
0x5A	SC_DAC_MIX_ADCLB_CH1_LDAC_MIX_BYT1[7:0]	SC DAC MIXER, ADC Loopback CH1 to LDAC coefficient byte[15:8]	0x00
0x5B	SC_DAC_MIX_ADCLB_CH1_LDAC_MIX_BYT2[7:0]	SC DAC MIXER, ADC Loopback CH1 to LDAC coefficient byte[7:0]	0x00
0x5C	SC_DAC_MIX_ADCLB_CH1_RDAC2_MIX_BYT1[7:0]	SC DAC MIXER, ADC Loopback CH1 to RDAC2 coefficient byte[15:8]	0x00
0x5D	SC_DAC_MIX_ADCLB_CH1_RDAC2_MIX_BYT2[7:0]	SC DAC MIXER, ADC Loopback CH1 to RDAC2 coefficient byte[7:0]	0x00
0x5E	SC_DAC_MIX_ADCLB_CH1_LDAC2_MIX_BYT1[7:0]	SC DAC MIXER, ADC Loopback CH1 to LDAC2 coefficient byte[15:8]	0x00
0x5F	SC_DAC_MIX_ADCLB_CH1_LDAC2_MIX_BYT2[7:0]	SC DAC MIXER, ADC Loopback CH1 to LDAC2 coefficient byte[7:0]	0x00
0x60	SC_DAC_MIX_ADCLB_CH2_RDAC_MIX_BYT1[7:0]	SC DAC MIXER, ADC Loopback CH2 to RDAC coefficient byte[15:8]	0x00
0x61	SC_DAC_MIX_ADCLB_CH2_RDAC_MIX_BYT2[7:0]	SC DAC MIXER, ADC Loopback CH2 to RDAC coefficient byte[7:0]	0x00

Table 3-3. Page 17 Registers for SC Mixer (continued)

Register Address	Register	Register Description	Reset Value
0x62	SC_DAC_MIX_ADCLB_CH2_LDAC_MIX_BYT1[7:0]	SC DAC MIXER, ADC Loopback CH2 to LDAC coefficient byte[15:8]	0x00
0x63	SC_DAC_MIX_ADCLB_CH2_LDAC_MIX_BYT2[7:0]	SC DAC MIXER, ADC Loopback CH2 to LDAC coefficient byte[7:0]	0x00
0x64	SC_DAC_MIX_ADCLB_CH2_RDAC2_MIX_BYT1[7:0]	SC DAC MIXER, ADC Loopback CH2 to RDAC2 coefficient byte[15:8]	0x00
0x65	SC_DAC_MIX_ADCLB_CH2_RDAC2_MIX_BYT2[7:0]	SC DAC MIXER, ADC Loopback CH2 to RDAC2 coefficient byte[7:0]	0x00
0x66	SC_DAC_MIX_ADCLB_CH2_LDAC2_MIX_BYT1[7:0]	SC DAC MIXER, ADC Loopback CH2 to LDAC2 coefficient byte[15:8]	0x00
0x67	SC_DAC_MIX_ADCLB_CH2_LDAC2_MIX_BYT2[7:0]	SC DAC MIXER, ADC Loopback CH2 to LDAC2 coefficient byte[7:0]	0x00
0x68	SC_DAC_MIX_SIGGEN_CH1_RDAC_MIX_BYT1[7:0]	SC DAC MIXER, Signal Generator CH1 to RDAC coefficient byte[15:8]	0x00
0x69	SC_DAC_MIX_SIGGEN_CH1_RDAC_MIX_BYT2[7:0]	SC DAC MIXER, Signal Generator CH1 to RDAC coefficient byte[7:0]	0x00
0x6A	SC_DAC_MIX_SIGGEN_CH1_LDAC_MIX_BYT1[7:0]	SC DAC MIXER, Signal Generator CH1 to LDAC coefficient byte[15:8]	0x00
0x6B	SC_DAC_MIX_SIGGEN_CH1_LDAC_MIX_BYT2[7:0]	SC DAC MIXER, Signal Generator CH1 to LDAC coefficient byte[7:0]	0x00
0x6C	SC_DAC_MIX_SIGGEN_CH1_RDAC2_MIX_BYT1[7:0]	SC DAC MIXER, Signal Generator CH1 to RDAC2 coefficient byte[15:8]	0x00
0x6D	SC_DAC_MIX_SIGGEN_CH1_RDAC2_MIX_BYT2[7:0]	SC DAC MIXER, Signal Generator CH1 to RDAC2 coefficient byte[7:0]	0x00
0x6E	SC_DAC_MIX_SIGGEN_CH1_LDAC2_MIX_BYT1[7:0]	SC DAC MIXER, Signal Generator CH1 to LDAC2 coefficient byte[15:8]	0x00
0x6F	SC_DAC_MIX_SIGGEN_CH1_LDAC2_MIX_BYT2[7:0]	SC DAC MIXER, Signal Generator CH1 to LDAC2 coefficient byte[7:0]	0x00
0x70	SC_DAC_MIX_SIGGEN_CH2_RDAC_MIX_BYT1[7:0]	SC DAC MIXER, Signal Generator CH2 to RDAC coefficient byte[15:8]	0x00
0x71	SC_DAC_MIX_SIGGEN_CH2_RDAC_MIX_BYT2[7:0]	SC DAC MIXER, Signal Generator CH2 to RDAC coefficient byte[7:0]	0x00
0x72	SC_DAC_MIX_SIGGEN_CH2_LDAC_MIX_BYT1[7:0]	SC DAC MIXER, Signal Generator CH2 to LDAC coefficient byte[15:8]	0x00
0x73	SC_DAC_MIX_SIGGEN_CH2_LDAC_MIX_BYT2[7:0]	SC DAC MIXER, Signal Generator CH2 to LDAC coefficient byte[7:0]	0x00
0x74	SC_DAC_MIX_SIGGEN_CH2_RDAC2_MIX_BYT1[7:0]	SC DAC MIXER, Signal Generator CH2 to RDAC2 coefficient byte[15:8]	0x00
0x75	SC_DAC_MIX_SIGGEN_CH2_RDAC2_MIX_BYT2[7:0]	SC DAC MIXER, Signal Generator CH2 to RDAC2 coefficient byte[7:0]	0x00

Table 3-3. Page 17 Registers for SC Mixer (continued)

Register Address	Register	Register Description	Reset Value
0x76	SC_DAC_MIX_SIGGEN_CH2_LDAC2_MIX_BYT1[7:0]	SC DAC MIXER, Signal Generator CH2 to LDAC2 coefficient byte[15:8]	0x00
0x77	SC_DAC_MIX_SIGGEN_CH2_LDAC2_MIX_BYT2[7:0]	SC DAC MIXER, Signal Generator CH2 to LDAC2 coefficient byte[7:0]	0x00

3.3.1 Playback Path Side-Chain - Example

This section describes an example implementation of the side-chain (SC) mixer on the playback path. The following sample code was executed on a TAC5112EVM-K evaluation module using PurePath™ Console 3. The SC mixer mixes the following inputs:

1. A 1kHz, 1Vrms differential analog sinusoidal signal on IN1P/IN1M that is mixed through the ADC-to-DAC loopback mixer.
2. A 2.2kHz, 0.5Vrms differential analog sinusoidal signal on IN2P/IN2M that is mixed through the ADC-to-DAC loopback mixer.
3. A 100Hz, 0.4FS (Full-Scale) digital sinusoidal tone on PASI RX Channel 1.
4. A 750Hz, 0.6FS (Full-Scale) digital sinusoidal tone on PASI RX Channel 2.
5. A 3.33kHz sinusoidal signal generated through the SG1signal generator.

The device plays the 2 mixed signals through the DAC on the OUT1P/M and OUT2P/M analog outputs, respectively.

```
w a0 00 00 #Page 0
w a0 01 01 #SW Reset
d 01

w a0 00 00 #Page 0
w a0 02 09 #Exit Sleep Mode with DREG and VREF Enabled
w a0 1a 30 #TDM protocol with 32-bit word length
w a0 4d 00 #VREF set to 2.75V for 2Vrms differential fullscale input
w a0 50 00 #ADC Channel 1 configured for AC-coupled differential input with 5kOhm input impedance
and audio bandwidth
w a0 55 00 #ADC Channel 2 configured for AC-coupled differential input with 5kOhm input impedance
and audio bandwidth
w a0 64 20 #DAC Channel 1 configured for differential output with 0.6*Vref as common mode
w a0 65 20 #DAC OUT1P configured for line out driver and audio bandwidth
w a0 66 20 #DAC OUT1M configured for line out driver and audio bandwidth
w a0 6b 20 #DAC Channel 2 configured for differential output with 0.6*Vref as common mode
w a0 6c 20 #DAC OUT2P configured for line out driver and audio bandwidth
w a0 6d 20 #DAC OUT2M configured for line out driver and audio bandwidth

w a0 26 01 #RX Offset = 1
w a0 28 20 #RX CH1 to DAC CH1
w a0 29 21 #RX CH2 to DAC CH2

w a0 00 01 #Page 1
w a0 2c d0 #Enable DAC ASI Mixer, Loopback Mixer, DAC Side-Chain Mixer

#ADC INPUTS
#CH1 = 1kHz, 1Vrms (0.5FS)
#CH2 = 2.2kHz, 0.5Vrms (0.25FS)
#ADC Loopback mixers
#LB1 = 0.2*CH1 + 0.8*CH2
w a0 00 0a #Page 10
w a0 48 19 99 99 9a #a1 = 0.2
w a0 4c 66 66 66 66 #b1 = 0.8
w a0 50 00 00 00 00 #c1 = 0
w a0 54 00 00 00 00 #d1 = 0

#LB2 = 0.6*CH1 + 0.4*CH2
w a0 58 4c cc cc cd #a2 = 0.6
w a0 5c 33 33 33 33 #b2 = 0.4
w a0 60 00 00 00 00 #c2 = 0
w a0 64 00 00 00 00 #d2 = 0
```

```
#Tone generator
#TG1 = 3.33kHz sine tone
#TG2 = No Signal
w a0 00 12
w a0 24 74 3e 09 17
w a0 20 6A 84 FE 00
w a0 2c 35 96 a4 6c
w a0 28 38 03 3C 00


#DAC ASI Inputs
#IN1 = 100Hz, 0.4FS (0.4FS)
#IN2 = 750Hz, 0.6FS (0.6FS)

w a0 00 11 #Page 17
#DAC output OUT1 = IN1 + 0.5*LB1
#DAC output OUT2 = IN2 + 0.4*LB2 + 0.2*TG1
w a0 58 00 00 20 00 #a1 = 0.5, a2 = 0
w a0 5c 00 00 00 00 #a3 = 0, a4 = 0
w a0 60 19 9a 00 00 #b1 = 0, b2 = 0.4
w a0 64 00 00 00 00 #b3 = 0, b4 = 0
w a0 68 0c cd 00 00 #c1 = 0, c2 = 0.2
w a0 6c 00 00 00 00 #c3 = 0, c4 = 0
w a0 70 00 00 00 00 #d1 = 0, d2 = 0
w a0 74 00 00 00 00 #d3 = 0, d4 = 0


w a0 00 00 #Page 0
w a0 76 cc #ADC CH1-2, DAC CH1-2 Enabled
w a0 78 c0 #ADC, DAC Paths enabled
```

Mixer Inputs:
IN1 = 1kHz, 1Vrms Sine (0.5FS analog, IN1P/M)
IN2 = 2.2kkHz, 0.5Vrms Sine (0.25FS analog, IN1P/M)
LB1 = ADC-to-DAC Loopback 1 = 0.2*IN1 + 0.8*IN2
LB2 = ADC-to-DAC Loopback 2 = 0.6*IN1 + 0.4*IN2
SG1 = Signal Generator 1 = 3.3kHz Sine tone (1FS
SG2 = Signal Generator2 = No Signal
IN3 = 100Hz Sine (0.4FS ASI Input, PASI RX CH1)
IN4 = 750Hz Sine (0.6FS ASI Input, PASI RX CH2)

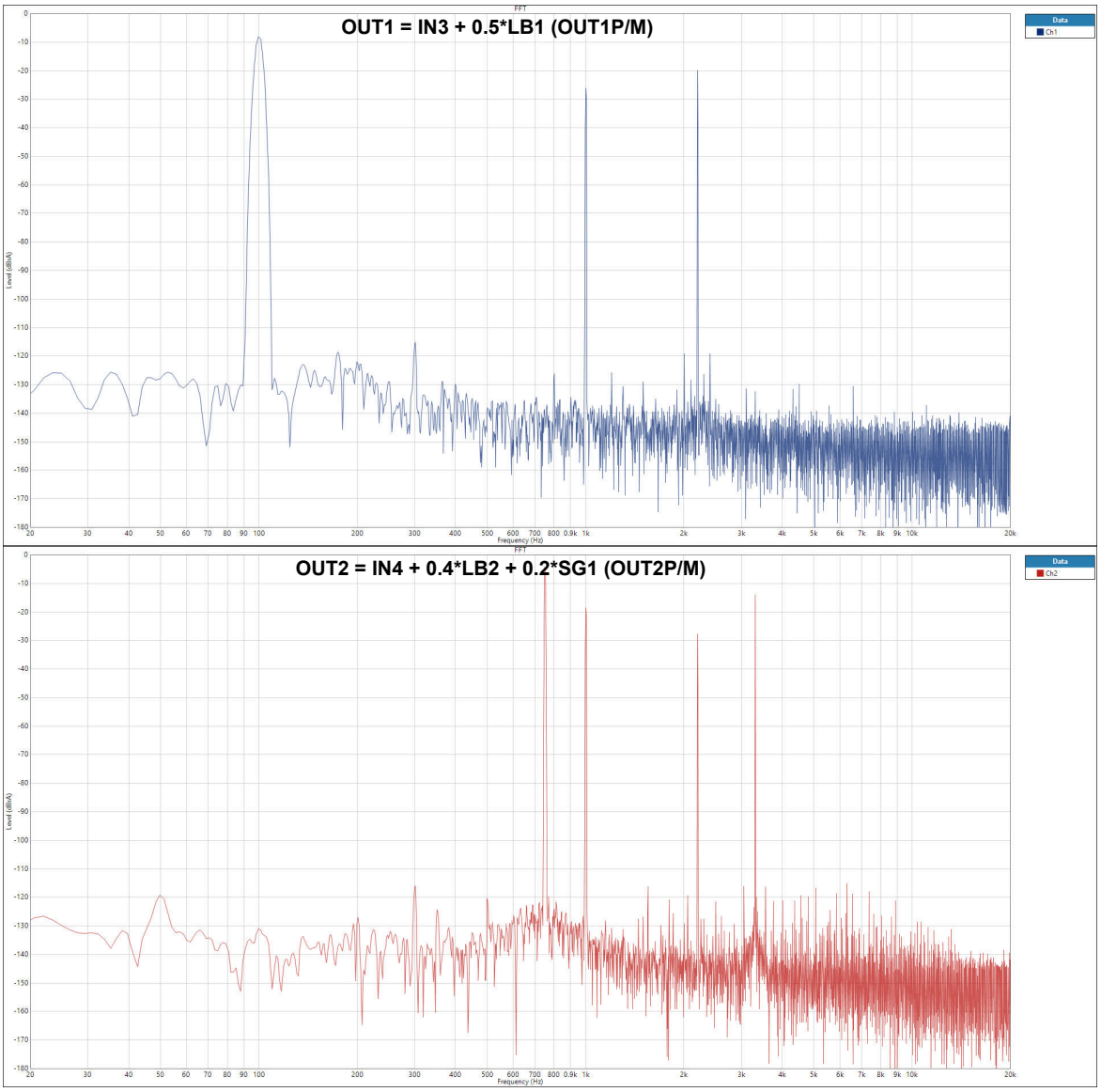

Figure 3-7. Playback Channel Outputs for Side-Chain Mixer

4 Application: ADC Channel Summation to Improve TAC5212 Dynamic Range

Consider two inputs, which have a *signal* component, and a *noise* component.

$$\begin{aligned} V_{in1} &= V_{sig1} + V_{noise1} \\ V_{in2} &= V_{sig2} + V_{noise2} \end{aligned} \quad (6)$$

When these two inputs are mixed together, the *signal* component is correlated, and hence adds directly, whereas the *noise* component is uncorrelated, and adds as root-sum-square.

Therefore, when the two inputs are mixed together in equal weight, the resultant output is:

$$V_{out} = \left(\frac{V_{sig1} + V_{sig2}}{2} \right) + \frac{\sqrt{{V_{noise1}}^2 + {V_{noise2}}^2}}{2} \quad (7)$$

If the same source is used for both inputs (as shown in Figure 4-1), then:

$$\begin{aligned} V_{sig1} &= V_{sig2} = V_{sig} \\ V_{noise1} &= V_{noise2} = V_{noise} \end{aligned} \quad (8)$$

The resulting output is

$$V_{out} = V_{sig} + \frac{V_{noise}}{\sqrt{2}} \quad (9)$$

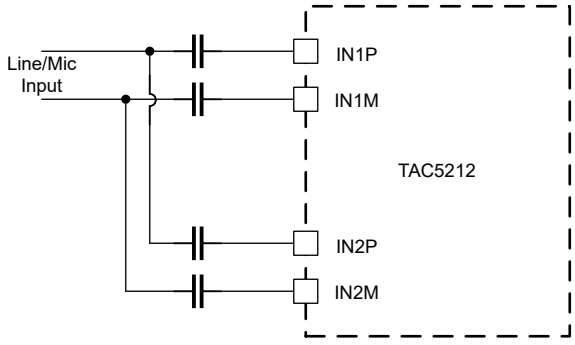

Figure 4-1. Same Input Connected to Both ADC Channels for Channel Summation

While the signal amplitude remains the same, the noise has reduced by a factor of 1.414. This can result in an improvement in the signal-to-noise ratio of the effective output by 3dB

This concept was tested out in TAC5212EVM-K, with the following configuration script and the same analog signal connected across both IN1P/M and IN2P/M.

```
w a0 00 00 # Page 0
w a0 01 01 #SW Reset
d 01

# Page 0 Register Writes
w a0 00 00
w a0 02 09 #Exit Sleep Mode with DREG and VREF Enabled
d 10
w a0 1a 30 #PASI in TDM protocol with 32-bit word length
w a0 4d 00 #VREF set to 2.75V for 2Vrms differential fullscale input
w a0 50 00 #ADC Channel 1 configured for AC-coupled differential input with 5kOhm input impedance
and audio bandwidth
w a0 55 00 #ADC Channel 2 configured for AC-coupled differential input with 5kOhm input impedance
and audio bandwidth


w a0 1e 20 #Recording Channel 1 on TDM Slot 0
w a0 1f 21 #Recording Channel 2 on TDM Slot 0
```

```
#Same signal on ADC CH1, ADC CH2
w a0 00 0a #Page 10
#Confugre Mixer1 for OUT1 = 0.5*IN1 + 0.5*IN2
w a0 08 40 00 00 00
w a0 0c 40 00 00 00
w a0 10 00 00 00 00
w a0 14 00 00 00 00
#Confugre Mixer1 for OUT2 = 0.5*IN1 + 0.5*IN2
w a0 18 40 00 00 00
w a0 1c 40 00 00 00
w a0 20 00 00 00 00
w a0 24 00 00 00 00


w a0 00 00 #Page 0
w a0 76 c0 #ADC Channels 1-2 Enabled
w a0 78 80 #ADC Powered Up
```

Table 4-1 shows the dynamic range with CH1 and CH2 individually, along with the 3dB improvement seen through channel summation. The measurements are A-weighted.

Table 4-1. Dynamic Range With and Without Channel Summation on TAC5212

Channel Summation via Mixer	CH1 Dynamic Range (dB)	CH2 Dynamic Range (dB)
Not Enabled	118.9dB	118.8dB
Enabled	121.9dB	121.9dB

5 Application: Analog Input to Analog Output Signal Flow in TAC5412-Q1

In the TAC5412-Q1 devices, the analog input can be mixed along with the DAC signal chain and played onto the analog outputs through the digital mixers. This is done using the ADC-to-DAC loopback path, and the side-chain mixer to translate the analog input voltage to a corresponding analog output voltage. Figure 5-2shows the analog input and analog output connections:

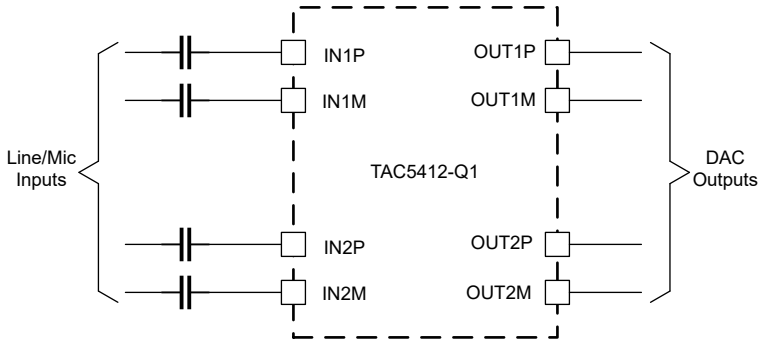

Figure 5-1. Input and Output Connections for TAC5412-Q1

This was tested on a TAC5412Q15B5EVM-K evaluation module using the following script where the ADC path is configured for a 10Vrms full-scale differential input, and the DAC path is configured for a 2Vrms full-scale differential output. The expectation here can be that when a 8.91Vrms (-1dBFS for ADC) is provided at the INxP/M pins, a 1.78Vrms (-1dBFS for DAC) can be seen on the corresponding OUTxP/M pins. The measurements are shown in Figure 5-2.

```
w a0 00 00 # Page 0
w a0 01 01 #SW Reset
d 01
# Page 0 Register Writes
w a0 00 00
w a0 02 09 #Exit Sleep Mode with DREG and VREF Enabled
d 10
w a0 1a 30 #PASI in TDM protocol with 32-bit word length
w a0 4d 00 #VREF set to 2.75V for 2Vrms differential fullscale input
w a0 50 00 #ADC Channel 1 configured for differential input with 10Vrms swing
w a0 55 00 #ADC Channel 2 configured for differential input with 10Vrms swing
w a0 64 20 #DAC Channel 1 configured for differential output with 0.6*Vref as common mode
w a0 65 20 #DAC OUT1P configured for line out driver and audio bandwidth
w a0 66 20 #DAC OUT1M configured for line out driver and audio bandwidth
w a0 6b 20 #DAC Channel 2 configured for differential output with 0.6*Vref as common mode
w a0 6c 20 #DAC OUT2P configured for line out driver and audio bandwidth
w a0 6d 20 #DAC OUT2M configured for line out driver and audio bandwidth

w a0 26 01 #RX Offset = 1

w a0 28 20 #RX CH1 to DAC CH1
w a0 29 21 #RX CH2 to DAC CH2

#ADC INPUTS
#CH1 = 1kHz, 8.91Vrms Sine (-1dBFS)
#CH2 = 2.2kHz, 5Vrms Sine (-6dBFS)
#ADC Loopback mixers
#LB1 = 1*CH1 + 0*CH2
w a0 00 0a #Page 10
w a0 48 7f ff ff ff #a1 = 1
w a0 4c 00 00 00 00 #b1 = 0
w a0 50 00 00 00 00 #c1 = 0
w a0 54 00 00 00 00 #d1 = 0

#LB2 = 0*CH1 + 1*CH2
w a0 58 00 00 00 00 #a2 = 0
w a0 5c 7f ff ff ff #b2 = 1
w a0 60 00 00 00 00 #c2 = 0
w a0 64 00 00 00 00 #d2 = 0

#DAC Inputs
#CH1 = CH2 = 0
```

```
w a0 00 11 #Page 17
#DAC output OUT1 = 1*LB1
#DAC output OUT2 = 1*LB2
w a0 58 00 00 3f ff #a1 = 0, a2 = 0
w a0 5c 00 00 00 00 #a3 = 0, a4 = 0
w a0 60 3f ff 00 00 #b1 = 0, b2 = 0
w a0 64 00 00 00 00 #b3 = 0, b4 = 0
w a0 68 00 00 00 00 #c1 = 0, c2 = 0
w a0 6c 00 00 00 00 #c3 = 0, c4 = 0
w a0 70 00 00 00 00 #d1 = 0, d2 = 0
w a0 74 00 00 00 00 #d3 = 0, d4 = 0


w a0 00 00 #Page 0
w a0 76 cc #ADC CH1-2, DAC CH1-2 Enabled
w a0 78 e0 #ADC, DAC Path and MICBIAS enabled
```

Analog Inputs (ADC Full-Scale = 10Vrms):
CH1 = 8.91Vrms, 1kHz Sine (-1dBFS, IN1P/M)
CH2 = 5Vrms, 1kHz Sine (-6dBFS, IN1P/M)
DAC Full-Scale = 2Vrms

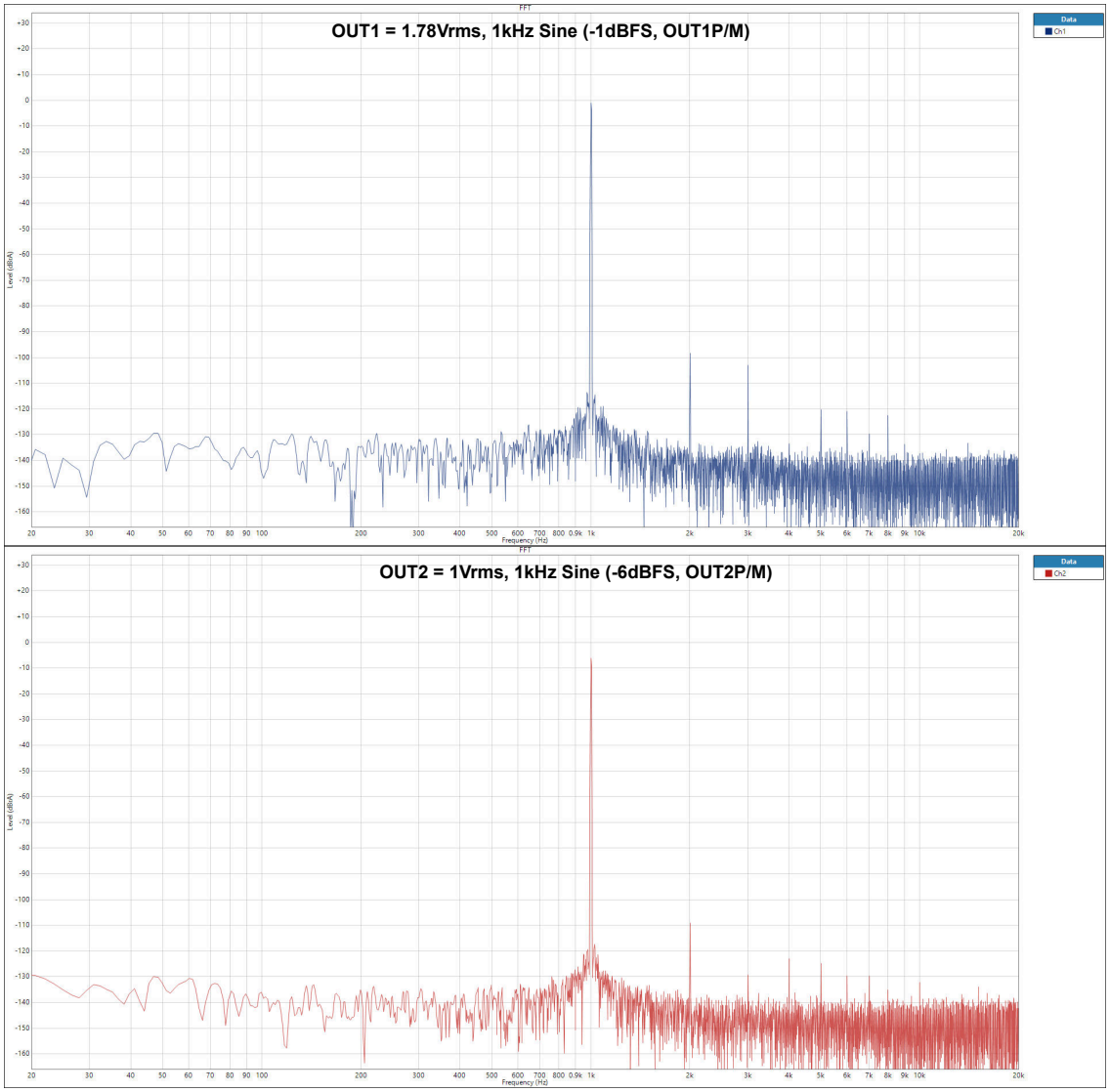

Figure 5-2. Analog Input-to-Analog Output Measured on TAC5412-Q1

6 Summary

The operation of the different digital mixers present in the recording and playback signal chains have been described in this application note, along with examples to demonstrate how these mixers can be configured using PurePath™™ Console 3. The document also describes two use cases where these mixers can be configured and used in an audio system.

7 References

- Texas Instruments, *TAC5212 High-Performance Stereo Audio Codec With 119dB Dynamic Range ADC and 120dB Dynamic Range DAC*, data sheet.
- Texas Instruments, *TAC5412-Q1 Automotive Low Power Stereo Audio Codec With Integrated Programmable Boost, Micbias and Diagnostics*, data sheet.
- Texas Instruments, *Increasing the Dynamic Range and SNR of Audio ADC With Channel Summation*, application note.
- Texas Instruments, *TAx5x1x Synchronous Sample Rate Conversion*, application note.
- Texas Instruments, *Tone Generation and Application Modes of TAx5x1x Devices*, application note.

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