DAC8550/51/52 Evaluation Module

This user's guide describes the characteristics, operation, and the use of the DAC8550/51/52 Evaluation Module. It covers all pertinent areas involved to properly use this EVM board along with the devices that it supports. The physical PCB layout, schematic diagram, and circuit descriptions are included.

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1 EVM Overview

This section gives a general overview of the DAC8550/51/52 evaluation module (EVM) and describes some factors that must be considered in using this module.

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1.1 Features

This EVM features the DAC8550/51/52 digital-to-analog converter (DAC). The DAC8550/51/52EVM is a simple evaluation module designed for quickly and easily evaluating the functionality and performance of the high-resolution, single- or dual-channel, and serial input DAC. This EVM features a serial interface to communicate with any host microprocessor or TI DSP-based system.

Although this EVM was specifically designed for the DAC8550/51 (single-channel) and DAC8552 (dual-channel) devices, it can also accommodate the DAC7512, DAC7513, DAC8501, DAC8531, and DAC8532 as they are all pin-compatible devices for the MSOP-8 (DGK) package. The DAC devices that can be installed onto the EVM board are shown in Table 1. The DAC8550/51EVM or DAC8552EVM are the only EVMs that are shipped from the factory. The remaining DAC devices listed in Table 1 have to be installed by the user as an option, if evaluating these devices is desired.

Table 1. List of DAC Devices Supported by This EVM

EVM Version	Device Option	Channel	Installation
12 Bit	DAC7512E	1	Optional
	DAC7513E	1	Optional
16 Bit	DAC8501E	1	Optional
	DAC8531E	1	Optional
	DAC8532IDGK	2	Optional
	DAC8550IDGK	**1**	**Default**
	DAC8551IDGK	**1**	**Default**
	DAC8552IDGK	**2**	**Default**

Although the DAC was designed for single-supply operation, a bipolar output range is also possible by properly configuring the output operational amplifier circuit. This is discussed in detail in Section 3.2.3. In addition, the external operational amplifier is also installed as an option to provide output signal conditioning or boost capacitive load drive and for other output mode requirement desired.

A +5-V precision voltage reference is provided as a default circuit reference for the DAC, but as an option, a connection terminal is also available for external voltage reference, if desired.

Also an option, a 4.096-V precision reference can be added if a REF3240 is installed via U4. Because the REF3240 does not come installed from the factory, the user must install it, if desired.

1.2 Power Requirements

The following sections describe the power requirements of this EVM.

1.2.1 Supply Voltage

The DC power supply (V_{DD}) requirement for this DAC8550/51/52EVM is selectable between +3.3 V and +5 V via W1 jumper header. The +3.3 V comes from J6-8 or J5-1 (if installed), and the +5 V comes from J6-3 or J5-3 (if installed) terminals, when plugged in via 5-6K Interface Board or the HPA449. These power supply voltages are referenced to ground through the J6-6 terminal. The V_{CC} and V_{SS} are only used by the U2 operational amplifier, which ranges from +15 V to –15 V maximum and connects through J1-3 and J1-1, respectively (if installed), or through J6-1 and J6-2 terminals. All the analog power supplies are referenced to analog ground through J1-2 and J6-6 terminals.

CAUTION

To avoid potential damage to the EVM board, ensure that the correct cables are connected to their respective terminals as labeled on the EVM board.

Stresses above the maximum listed voltage ratings may cause permanent damage to the device.

The negative rail of the output operational amplifier, U2, can be selected between VSS and AGND via W5 jumper. The external operational amplifier is installed as an option to provide output signal conditioning or for other output mode requirements desired.

1.2.2 Reference Voltage

The +5-V precision voltage reference is provided as the main source to supply the external voltage reference for the DAC through REF02, U3, via jumper W4 by shorting pins 1 and 2. The reference voltage goes through an adjustable 100-kΩ potentiometer, R11, in series with 20-kΩ R10, to allow the user to adjust the reference voltage to its desired settings. The voltage reference then is buffered through U8A as seen by the device under test. The test points TP1, TP2, and TP5 are also provided, as well as J4-18 and J4-20, to allow the user to connect another external reference source if the onboard reference circuit is not desired. The external voltage reference should not exceed +5 Vdc.

The REF02 precision reference is powered by V_{CC} (+15 V) through J1-3 or J6-1 terminal.

An optional +4.096-V precision voltage reference also is provided to supply the external voltage reference and set the voltage output range of the DAC under test through REF3240, U4, via jumper resistor, R15. When using U4 as a reference source, ensure that pin J4-20 is not energized; otherwise, damage to the EVM and the host board may occur.

The test point TP1 and J4-20 are provided to allow the user to connect to another external reference source if the onboard reference circuit is not desired. The external voltage reference should not exceed the applied power supply, V_{DD}, of the DAC under test.

The REF3240 precision reference is powered by +5 VA through J6-3 or J5-3 terminal (if installed).

CAUTION

When applying an external voltage reference through TP1 or J4-20, ensure that it does not exceed +5 V maximum. Otherwise, this can permanently damage the DAC8550/51/52, U1, device under test.

1.3 EVM Basic Functions

This EVM is designed primarily as a functional evaluation platform to test certain functional characteristics of the DAC8550/51/52 DAC. Functional evaluation of the installed DAC device can be accomplished with the use of any microprocessor, TI DSP, or some sort of a signal/waveform generator.

The headers J2 (top side) and P2 (bottom side) are pass-through connectors provided to allow the control signals and data required to interface a host processor or waveform generator to the DAC8550/51/52EVM using a custom-built cable.

A TI adapter interface board, the 5-6K Interface Board, is also available to fit and mate with TI's C5000 and C6000 DSP Starter Kits (DSK). This eliminates problems involved in building a custom cable. In addition, this EVM can connect to and interface with an MSP430-based platform (HPA449) that uses the MSP430F449 microprocessor. For more details or information regarding the 5-6K Interface Board or the HPA449 platform, call Texas Instruments or send an e-mail to *dataconvapps@list.ti.com*.

The DAC outputs can be monitored through the selected pins of the J4 header connector. The output(s) can be switched through their respective jumpers W2 and W7 for the purpose of stacking. Stacking allows a total of two (for DAC8550/51) or four (for DAC8552) DAC channels to be used, providing that the frame synchronization signal, $\overline{\text{SYNC}}$, is unique for each EVM board stacked.

In addition, the option of selecting one DAC output that can be fed to the non-inverting side of the output operational amplifier, U2, is also possible by using a jumper across the selected pins of J4. The output operational amplifier, U2, must first be configured correctly for the desired waveform characteristic (see Section 3 of this user's guide).

Figure 1 shows a block diagram of the DAC8550/51/52EVM.

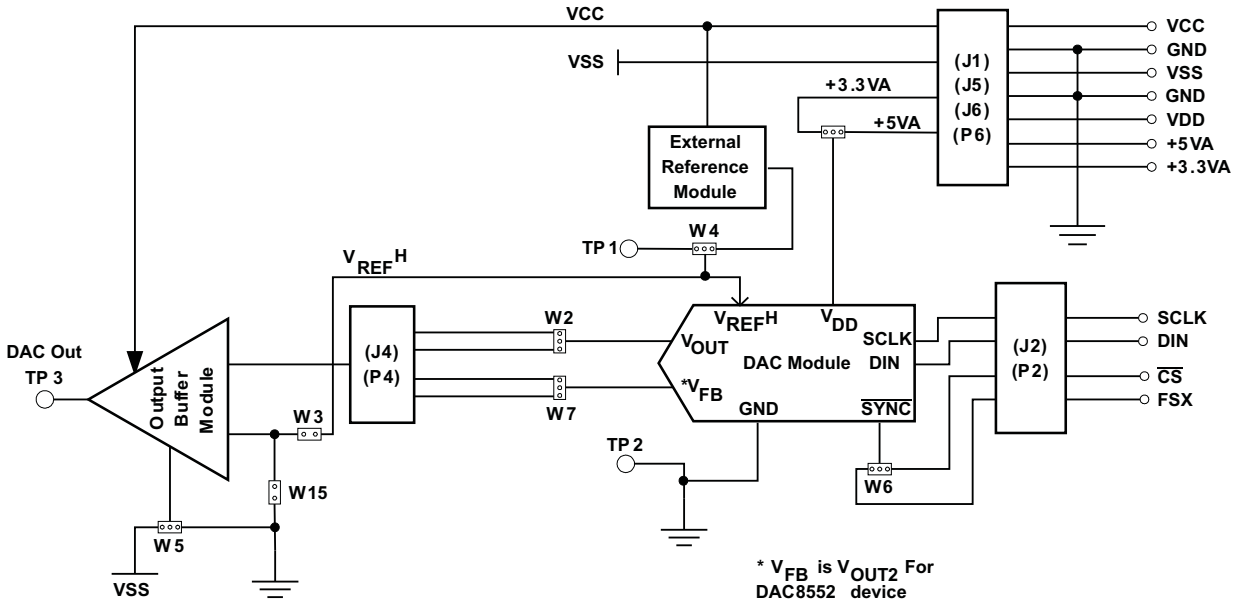


Figure 1. EVM Block Diagram

2 PCB Design and Performance

This section discusses the layout design of the PCB, describing the physical and mechanical characteristics of the EVM, as well as a brief description of the EVM test performance procedure performed. The list of components used on this evaluation module is included in this section.

2.1 PCB Layout

The DAC8550/51/52EVM is designed to preserve the performance quality of the DAC, the device under test (DUT), as specified in the data sheet. To take full advantage of the EVM's capabilities, use care during the schematic design phase to properly select the right components and to build the circuit correctly. The circuit should include adequate bypassing, identifying and managing the analog and digital signals, and understanding the components' electrical and mechanical attributes.

The main design concern during the layout process is the optimal placement of components and the proper routing of signals. Place the bypass capacitors as close as possible to the pins; properly separate the analog and digital signals from each other. In the layout process, carefully consider the power and ground plane because of their importance. A solid plane is ideally preferred, but because of its greater cost, sometimes a split plane can be used satisfactorily. When considering a split plane design, analyze the component placement and carefully split the board into its analog and digital sections starting from the DUT. The ground plane plays an important role in controlling the noise and other effects that otherwise contributes to the error of the DAC output. To ensure that the return currents are handled properly, route the appropriate signals only in their respective sections, meaning that the analog traces should only lay directly above or below the analog section and the digital traces in the digital section. Minimize the length of the traces but use the biggest possible trace width allowable in the design. These design practices are illustrated in Figure 2 through Figure 8.

The DAC8550/51/52EVM board is constructed on a four-layer printed-circuit board (PCB) using a copper-clad FR-4 laminate material. The PCB has a dimension of 43,1800 mm (1.7000 inch) × 82,5500 mm (3.2500 inch), and the board thickness is 1,5748 mm (0.062 inch). Figure 2 through Figure 6 show the individual artwork layers.

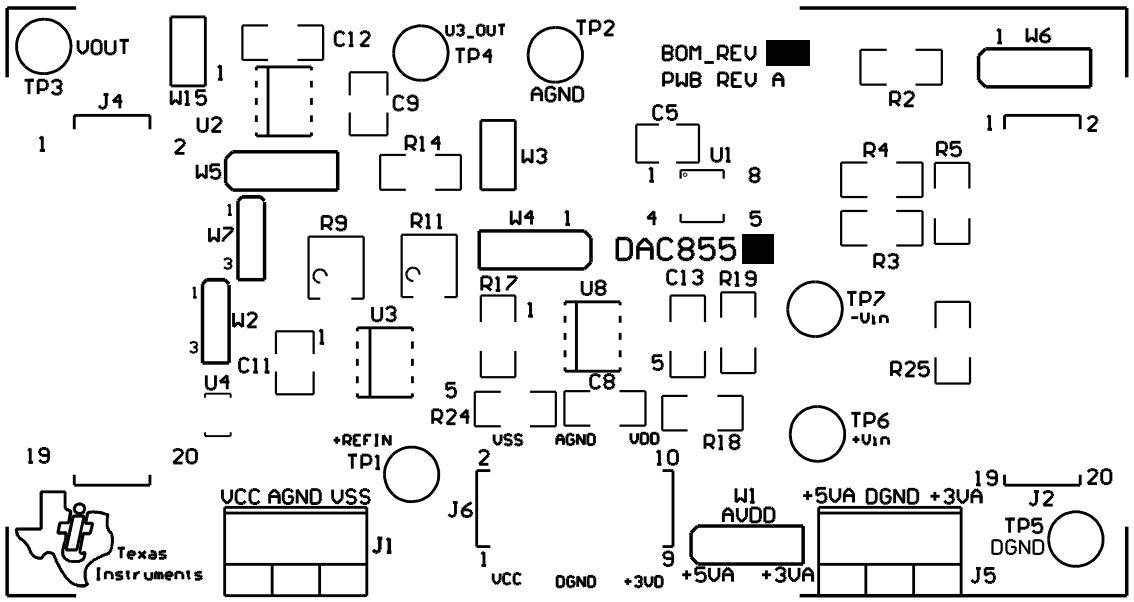


Figure 2. Top Silkscreen

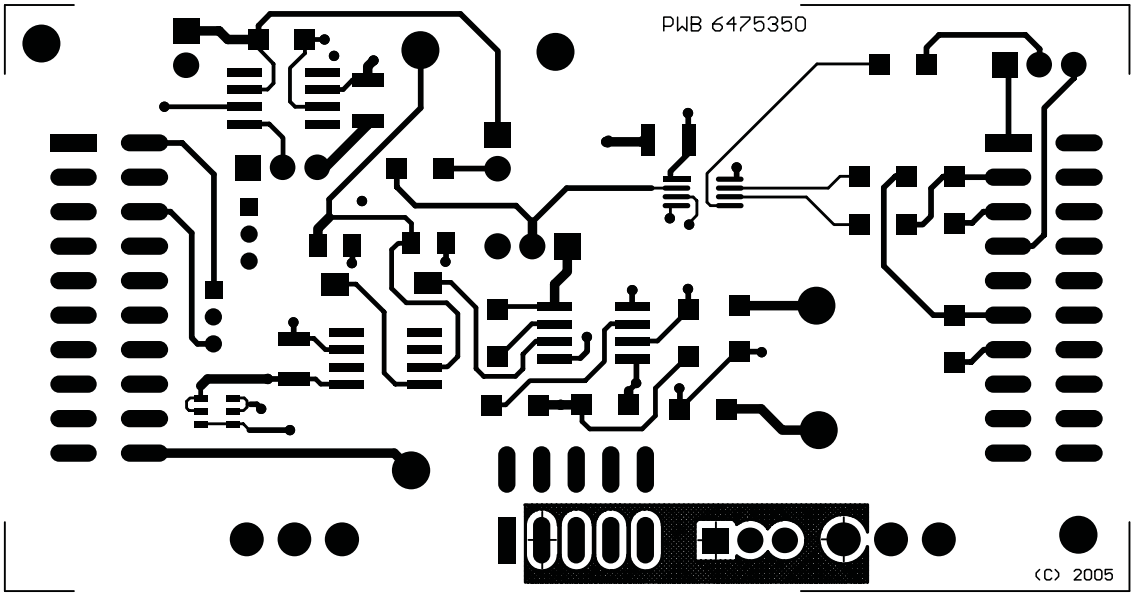


Figure 3. Layer 1 (Top Signal Plane)

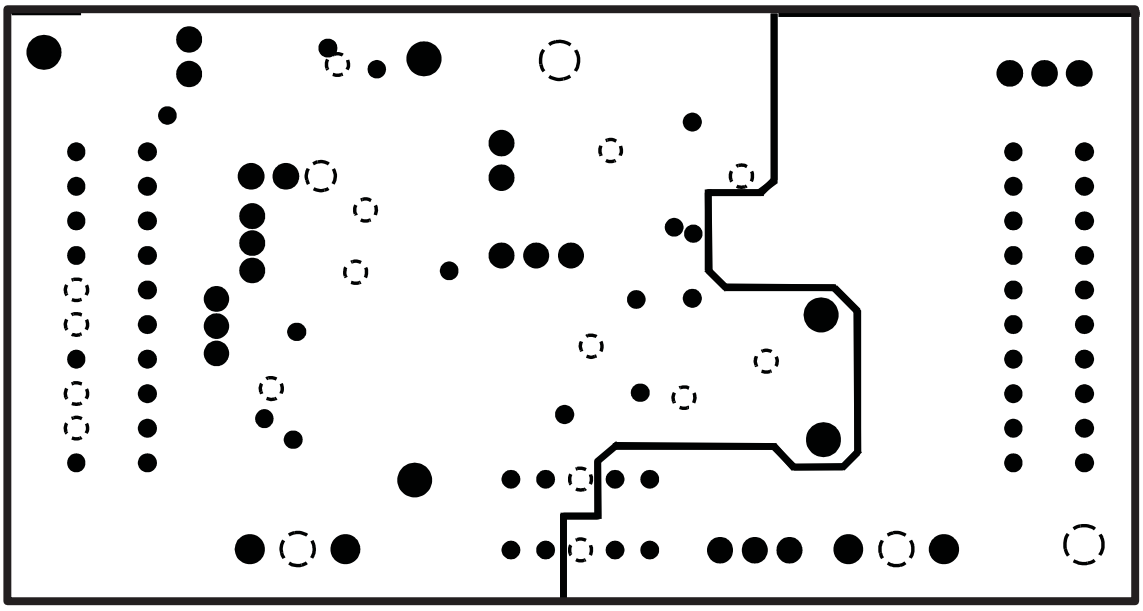


Figure 4. Layer 2 (Ground Plane)

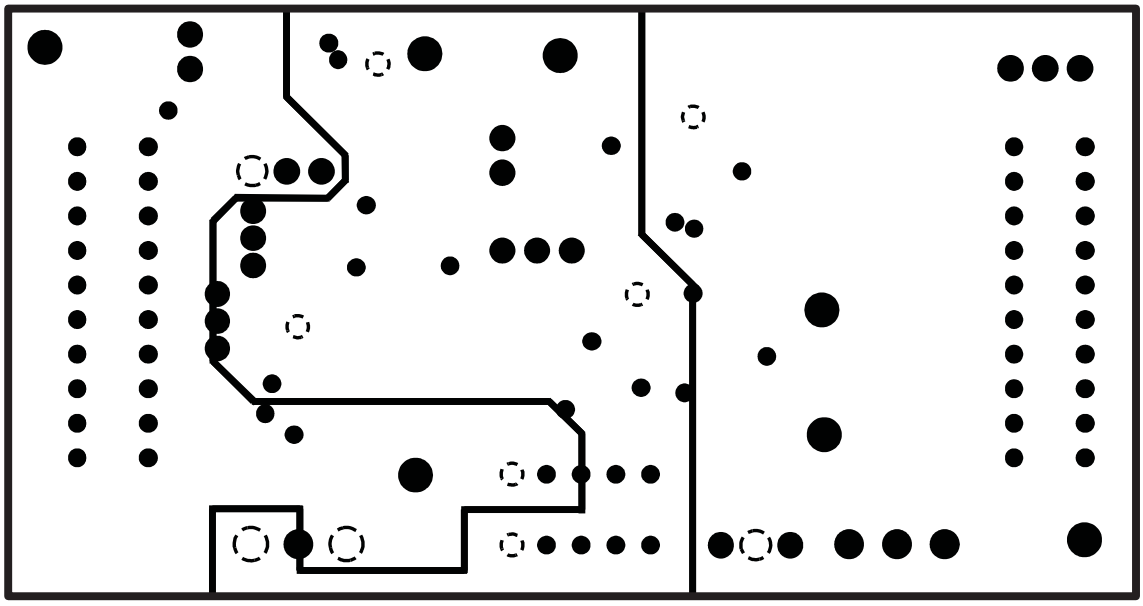


Figure 5. Layer 3 (Power Plane)

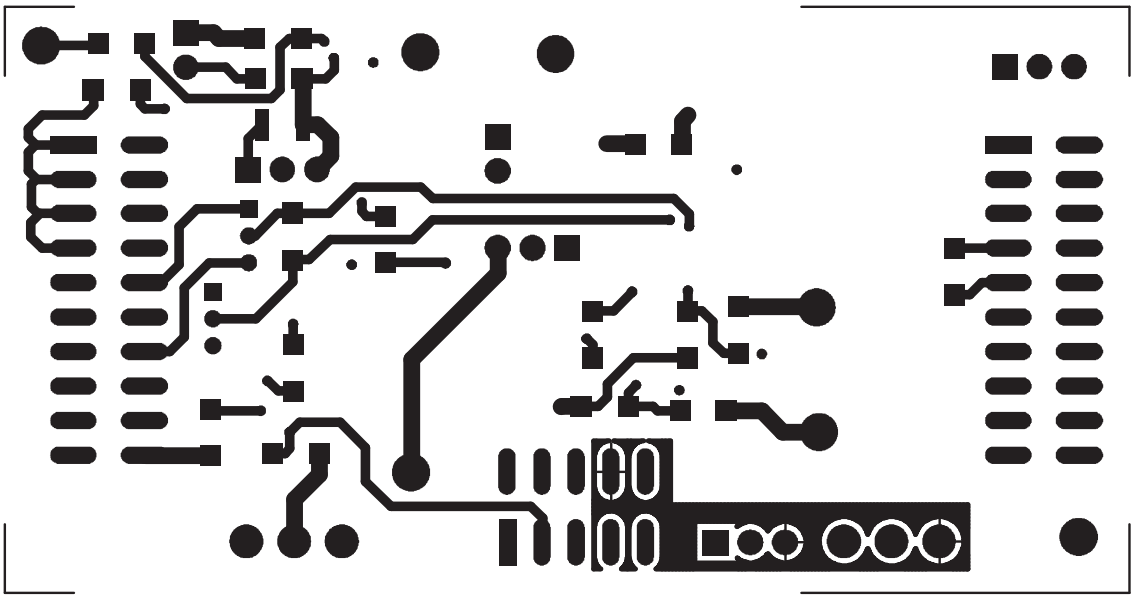


Figure 6. Layer 4 (Bottom Signal Plane)

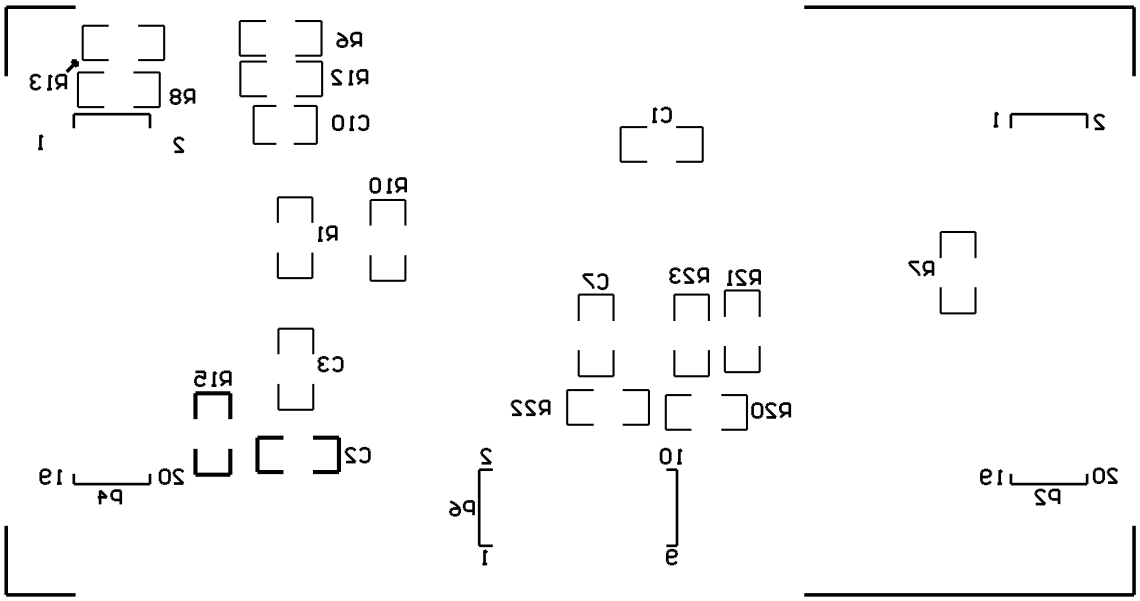


Figure 7. Bottom Silkscreen

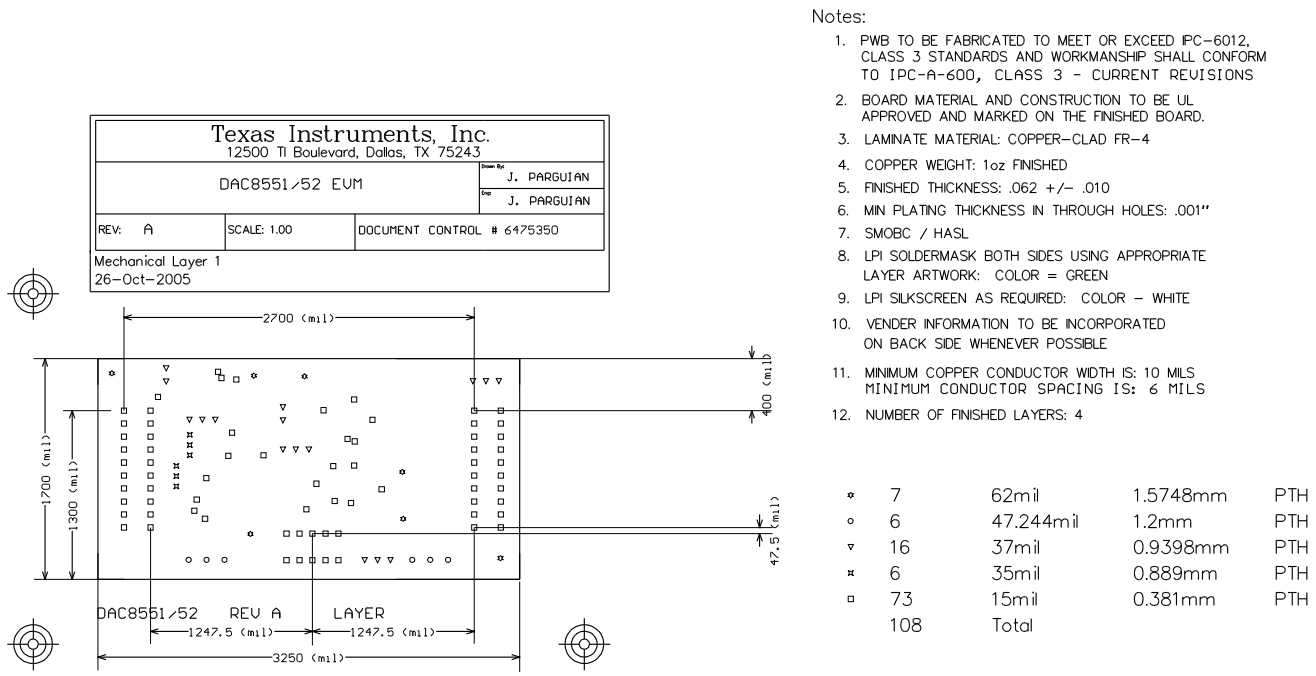


Figure 8. Drill Drawing

2.2 EVM Performance

The EVM performance test is performed using a high-density DAC bench test board, an Agilent 3458A digital multimeter, and a PC running the LabVIEW™ software. The EVM board is tested for all codes of 65535, and the DUT is allowed to settle for 1 ms before the meter is read. This process is repeated for all codes to generate the measurements for INL and DNL.

Figure 9 shows the INL and DNL characteristic plots.

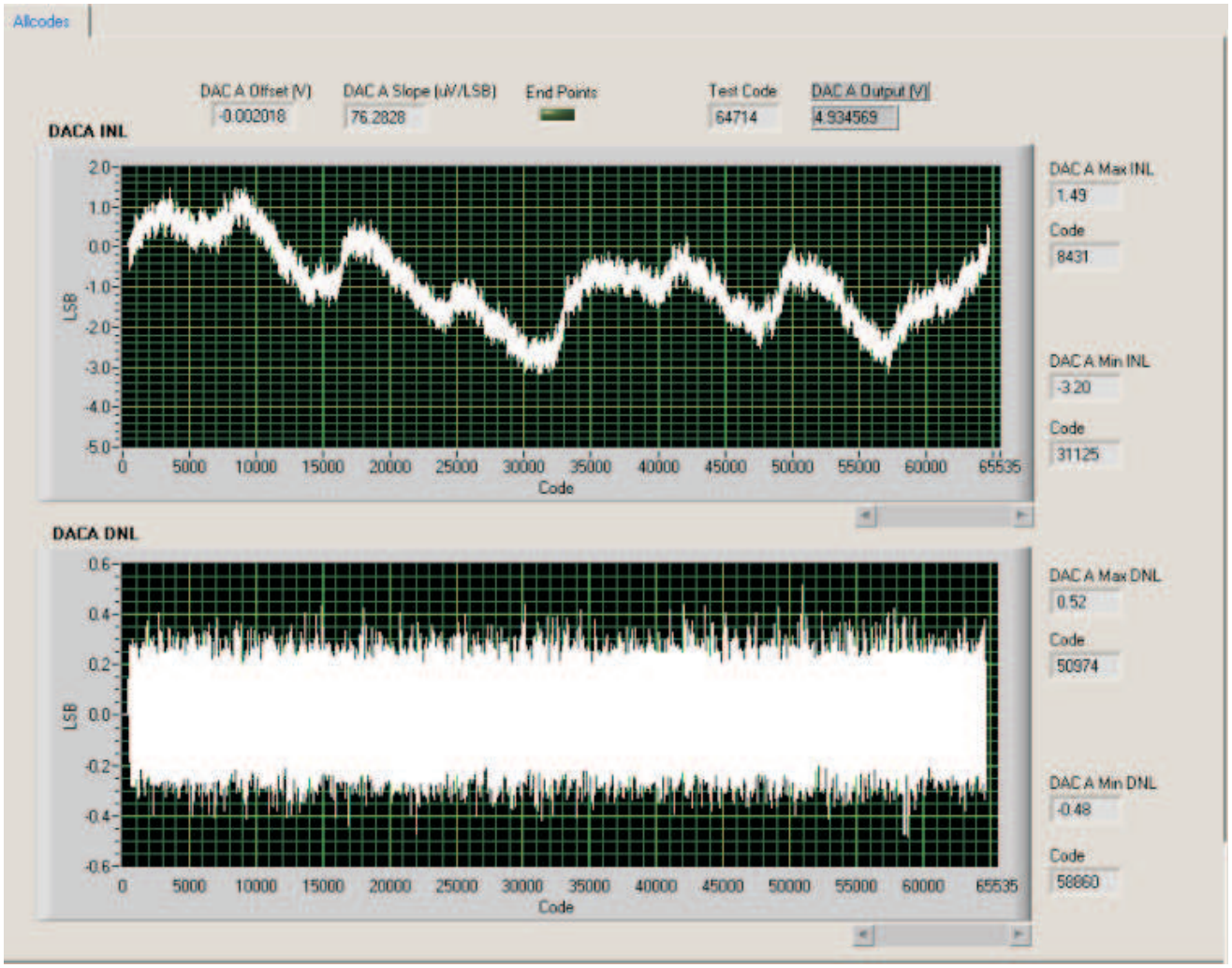


Figure 9. INL and DNL Characteristic Plot

2.3 Bill of Materials

Table 2. Parts List

Item	Qty	Value	Designators	Description	Vendor	Vendor Part Number
1	3	0.1 µF	C1 C3 C7	Multilayer Ceramic Chip Capacitor, 1206 SMD, 25V, ±15% TC, ±10% Tol	TDK	C3216X7R1E104KT
2	2	1 µF	C9 C10	Multilayer Ceramic Chip Capacitor, 1210 SMD, 25V, ±15% TC, ±10% Tol	TDK	C3225X7R1E105KT
3	1	1 nF	C12	Multilayer Ceramic Chip Capacitor, 1206 SMD, 25V, ±15% TC, ±10% Tol	TDK	C3216X7R1H102KT
4	1	0.47 µF	C2	Multilayer Ceramic Chip Capacitor, 1206 SMD, 50V, ±15% TC, ±10% Tol(1)	TDK	C3216X7R1H474KT
5	2	10 µF	C5 C11	Multilayer Ceramic Chip Capacitor, 1210 SMD, 25V, ±15% TC, ±10% Tol	TDK	C3225X7R1E106KT
6	3	10 kΩ	R6 R12 R14	1/8W 1206 Thick Film Chip Resistor, ±1% Tol	Panasonic	ERJ-8ENF1002V

(1) P2, P4, and P6 parts are not shown in the schematic diagram. All the P-designated parts are installed in the bottom side of the PCB opposite the J-designated counterpart. For example, J2 is installed on the top side whereas P2 is installed on the bottom side opposite of J2. **The following components are not installed: J1, J5, C2, C8, C13, R5, R7, R15, R18, R19, R20, R21, R22, R23, R24, R25, and U4. The installed U1 device determines the type of EVM.**

Table 2. Parts List (continued)

Item	Qty	Value	Designators	Description	Vendor	Vendor Part Number
7	1	20 kΩ Trim Pot	R9	5T Potentiometer, 4mm SMD, Cermet	Bourns	3214W-1-203E
8	10	0 Ω	R1 R2 R3 R4 R5 R7 R8 R15 R17 R25	1/4W 1206 Thick Film Chip Resistor, ±5% Tol(1)	Panasonic	ERJ-8GEY0R00V
9	1	100 Ω	R13	1/4W 1206 Thick Film Chip Resistor, ±5% Tol	Panasonic	ERJ-8GEYJ101V
10	1	20 kΩ	R10	1/4W 1206 Thick Film Chip Resistor, ±5% Tol	Panasonic	ERJ-8GEYJ203V
11	1	100 kΩ Trim Pot	R11	Potentiometer, 4mm SMD, Cermet	Bourns	3214W-1-104E
12	2	10 × 2 × 0.1 SMT	J2 J4	20-PIN Terminal Strip	Samtec	TSM-110-01-S-DV-M
13	1	5 × 2 × 0.1 SMT	J6	10-PIN Terminal Strip	Samtec	TSM-105-01-T-DV
14	2	3 × 1 × 0.138 TH	J1 J5	3-Pin Terminal Block(1)	On-Shore Tech	ED555/3DS
15	2	10 × 2 × 0.1 SMT	P2 P4	20-PIN Socket Strip(1)	Samtec	SSW-110-22-S-D-VS-P
16	1	5 × 2 × 0.1 SMT	P6	10-PIN Socket Strip(1)	Samtec	SSW-105-22-F-D-VS-K
17	7	1 × 1 × 0.061D TH	TP1 TP2 TP3 TP4 TP5 TP6 TP7	Turret Terminal Pin	Mill-Max	2348-2-00-01-00-00-07-0
18	1	Bipolar Op-Amp	U8	8-SOP(D) High Precision Low Noise Op-Amp	Texas Instruments	OPA2227UA
19	1	16-Bit String DAC	U1	MSOP-8(DGK), 1-CH, SPI, Low Glitch, Voltage Output DAC(1)	Texas Instruments	DAC8550IDGK
				MSOP-8(DGK), 1-CH, SPI, Low Glitch, Voltage Output DAC (1)		DAC8551IDGK
				MSOP-8(DGK), 2-CH, SPI, Low Glitch, Voltage Output DAC(1)		DAC8552IDGK
20	1	4.096 V Reference	U4	4ppm/°C, 100 µA, SOT23-6 VOLTAGE REFERENCE(1)	Texas Instruments	REF3240AIDBV
21	1	5 V Reference	U3	15ppm/°C, ±0.2% Tol Output, SOIC-8, Voltage Reference	Texas Instruments	REF02AU
22	1	Bipolar Op-Amp	U2	8-SOP(D) High Precision, Low Offset and Drift, Op-Amp	Texas Instruments	OPA277UA
23	2	3 × 1 × 0.7874 TH	W2 W7	3-PIN Terminal Strip	Samtec	TMMH-103-01-T-T
24	2	2 × 1 × 0.1 TH	W3 W15	Modified 0.025" Square Post Header	Samtec	MTSW-102-08-T-S-295
25	4	3 × 1 × 0.1 TH	W1 W4 W5 W6	Modified 0.025" Square Post Header	Samtec	MTSW-103-08-T-S-295
26	9	Not Installed	C8 C13 R18 R19 R20 R21 R22 R23 R24	Do not install these components	To Be Determined	To Be Determine

3 EVM Operation

This section covers in detail the EVM operation to guide the user in evaluating the onboard DAC and how to interface the EVM to a specific host processor.

See the DAC8550 data sheet (SLAS476), DAC8551 data sheet (SLAS429), and DAC8552 data sheet (SLAS430) for information about the serial interface and other related topics.

The EVM board is factory-tested and configured to operate in the unipolar output mode.

3.1 Factory Default Setting

The EVM board is set to its default configuration from the factory as described on Table 3 to operate in unipolar +5-V mode. Figure 10 and Figure 11 show the default jumper configuration as described in the table for the DAC8550/51 and DAC8552, respectively.

Table 3. Factory Default Jumper Setting

Reference	Jumper Position	Function
W1	1-2	Analog supply for the DAC8550/51/52 is +5 VA.
W2	1-2	DAC output A ($V_{OUT}A$) is routed to J4-2.
W3	OPEN	$V_{REF}H$ is not routed to the inverting input of the operational amplifier for voltage offset with gain of 2 output (for bipolar mode of operation).
W4	1-2	Onboard external buffered reference U3 is routed to $V_{REF}H$.
W5	1-2	Negative supply rail of U2 operational amplifier is supplied with V_{SS}.
W6	1-2	$\overline{CS}$ signal from J2 is used for frame synchronization, $\overline{SYNC}$, signal.
W7	OPEN	For DAC8550/51 EVM, the V_{FB} is not routed out unless there is a need to minimize the output error. If using W7, remove R1 and short W7; then connect V_{FB} and $V_{OUT}A$ as close as possible to the load.
	1-2	For DAC8552 EVM, R1 is not installed and W7 is shorted so that $V_{OUT}B$ is routed to J4-10 header terminal.
	2-3	For DAC8552 EVM, R1 is not installed, and W7 is shorted so that $V_{OUT}B$ is routed to J4-14 header terminal.
W15	CLOSE	Output operational amplifier, U2, is configured for a gain of 2.
J4	2-1	DAC output A ($V_{OUT}A$) is connected to the non-inverting input of the output operational amplifier, U2.

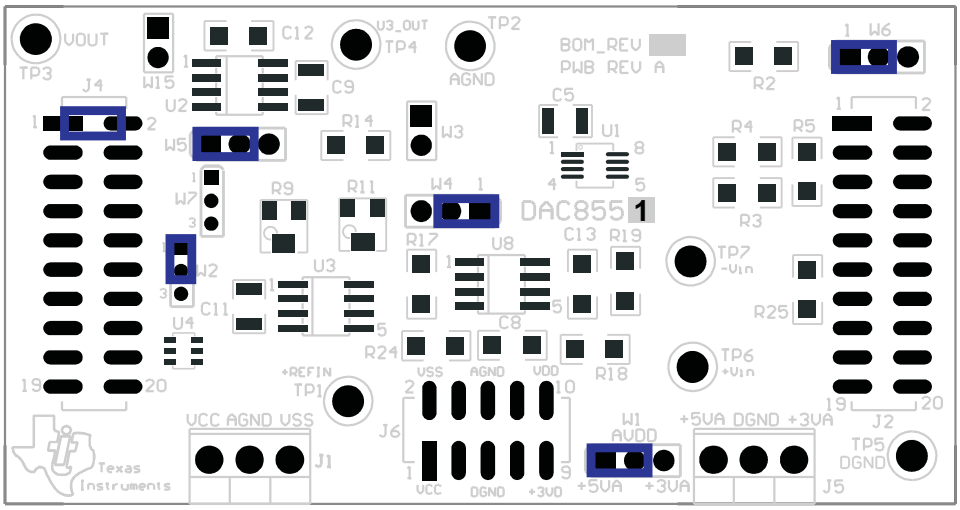


Figure 10. DAC8550/51 EVM Default Jumper Configuration

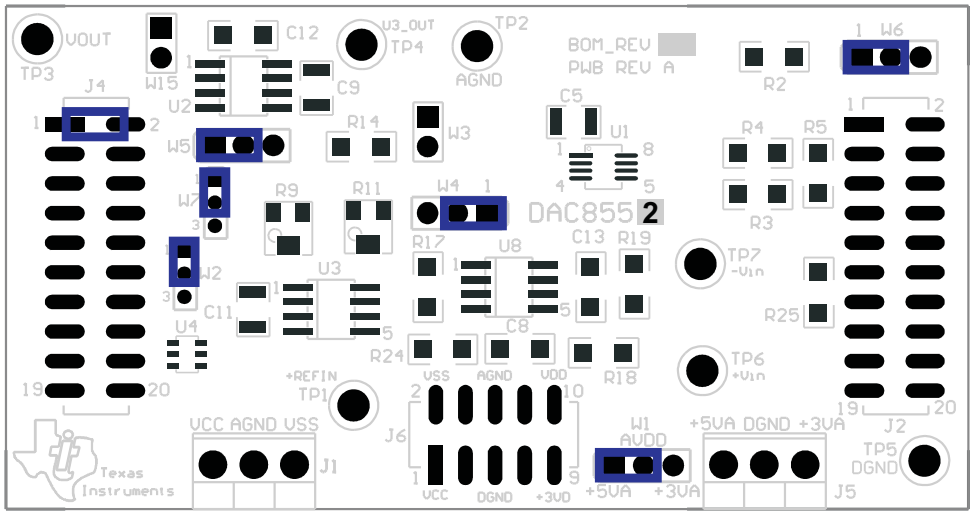


Figure 11. DAC8552 EVM Default Jumper Configuration

3.2 Host Processor Interface

The host processor basically drives the DAC; therefore, the proper operation of the DAC depends on the successful configuration between the host processor and the EVM board. Additionally, a properly written code is required to operate the DAC.

A custom cable can be made specific to the host interface platform. The EVM allows an interface to the host processor through the J2 header connector for the serial control signals and the serial data input. The output can be monitored through the J4 header connector.

An interface adapter board also is available for a specific TI DSP starter kit as well as an MSP430-based microprocessor as mentioned in Section 1. Using the TI Interface Board alleviates the task of building customized cables and allows easy configuration of a simple evaluation system.

The DAC8550/51/52 interfaces with any host processor capable of handling SPI™ protocols or the TI DSP. For more information regarding the DAC8550/51/52 data interface, see the data sheet.

3.3 EVM Stacking

The stacking of EVMs is possible if users need to evaluate two DAC8550/51/52 devices to yield a total of up to two-channel (for DAC8550/51) or four-channel (for DAC8552) outputs. A maximum of two EVMs are allowed because the output terminal, J4, dictates the number of DAC channels that can be connected without output bus contention. Table 4 shows how the DAC output channels are mapped into the output terminal, J4, with respect to the jumper position of W2 and W7.

Table 4. DAC Output Channel Mapping

Reference	Jumper Position	Function
W2	1-2	DAC output A (V_{OUT}A) is routed to J4-2.
	2-3	DAC output A (V_{OUT}A) is routed to J4-6.
W7	1-2	DAC output B (V_{OUT}B) is routed to J4-10.
	2-3	DAC output B (V_{OUT}B) is routed to J4-14.

In order to allow exclusive control of each EVM that is stacked together, each DAC8550/51/52 must have a separate $\overline{\text{SYNC}}$ signal. This is accomplished in hardware by routing the $\overline{\text{SYNC}}$ signal of the first EVM through $\overline{\text{CS}}$ (P2/J2 pin 1) by shorting pins 1-2 of jumper W6. The second EVM should use the FSX signal (P2/J2 pin 7) to drive the $\overline{\text{SYNC}}$ signal by shorting pins 2-3 of the jumper W6. The output can be mapped as described in Table 4 for each of the EVMs stacked.

3.4 The Output Operational Amplifier

The EVM includes an optional signal-conditioning circuit for the DAC output through an external operational amplifier, U2. Only one DAC output channel can be monitored at any given time for evaluation because the odd-numbered pins (J4-1 to J4-7) are tied together. The output operational amplifier is set to unity gain configuration by default but can be modified by simple jumper settings. Nevertheless, the raw output of the DAC can be probed through the specified pins of the J4 output terminal, which also provides mechanical stability when stacking or plugging into any interface board. In addition, it provides easy access for monitoring up to two (DAC8550/51) or four (DAC8552) DAC channels when stacking two EVMs together (see Section 3.3).

The following sections describe the different configurations of the output amplifier, U2.

3.4.1 Unity Gain Output

The buffered output configuration can be used to prevent loading the DAC8550/51/52, although it may present some slight distortion because of the feedback resistor and capacitor. The user can tailor the feedback circuit to closely match the desired wave shape by simply desoldering R6 and C12 and replacing them with the desired values. It is also possible to simply eliminate R6 and C12 altogether and to solder a 0-Ω resistor in place of R6, if desired.

Table 5 shows the jumper setting for the unity gain configuration of the DAC external output buffer in unipolar or bipolar mode.

Table 5. Unity Gain Output Jumper Settings

Reference	Jumper Position		Function
	Unipolar	Bipolar	
W3	OPEN	OPEN	Disconnect $V_{REF}H$ from the inverting input of the operational amplifier.
W5	2-3	1-2	Supplies V_{SS} to the negative rail of operational amplifier or ties it to AGND.
W15	OPEN	OPEN	Disconnect negative input of the operational amplifier from the gain resistor, R12.

3.4.2 Output Gain of Two

Two types of configurations yield an output gain of 2, depending on the setup of the jumpers W3 and W15. These configurations allow the user to choose whether the DAC output has $V_{REF}H$ as an offset or not.

Table 6 shows the proper jumper settings of the EVM for the 2× gain output of the DAC.

Table 6. Gain of Two Output Jumper Settings

Reference	Jumper Position		Function
	Unipolar	Bipolar	
W3	Close	Close	Inverting input of the output operational amplifier, U2, is connected to $V_{REF}H$ for use as its offset voltage with a gain of 2. W15 jumper must be open.
	Open	Open	$V_{REF}H$ is disconnected from the inverting input of the output operational amplifier, U2. W15 jumper must be closed.
W5	2-3	1-2	Supplies power, V_{SS}, to the negative rail of operational amplifier, U2, for bipolar mode, or ties it to AGND for unipolar mode.
W15	Close	Close	Configures operational amplifier, U2, for a gain of 2 output without a voltage offset. W3 jumper must be open.
	Open	Open	Inverting input of the operational amplifier, U2, is disconnected from the gain resistor, R12. W3 jumper must be closed.

3.4.3 Capacitive Load Drive

Another output configuration option is to drive a wide range of capacitive load requirements. However, all operational amplifiers under certain conditions may become unstable, depending on the operational amplifier configuration, gain, and load value. These are just a few of the factors that can affect operational amplifier stability performance and should be considered when implementing.

In unity gain, the OPA627 operational amplifier, U2, performs well with large capacitive loads. Increasing the gain enhances the amplifier's ability to drive even more capacitance, and adding a load resistor further improves the capacitive load drive capability.

Table 7 shows the jumper setting configuration for a capacitive load drive.

Table 7. Capacitive Load Drive Output Jumper Settings

Reference	Jumper Position		Function
	Unipolar	Bipolar	
W3	Open	Open	$V_{REF}H$ is disconnected from the inverting input of the output operational amplifier, U2.
W5	2-3	1-2	Supplies power, V_{SS}, to the negative rail of operational amplifier, U2, for bipolar mode, or ties it to AGND for unipolar mode.
W15	Open	Open	Capacitive load drive output of DAC is routed to pin 1 of W15 jumper and may be used as the output terminal.

3.5 Optional Signal-Conditioning Operational Amplifier (U8B)

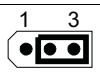
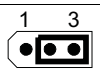
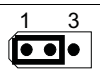
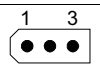
One part of the dual-package operational amplifier, OPA2227 (U8), is used for reference buffering (U8A) whereas the other is unused. This unused operational amplifier (U8B) is left for whatever operational amplifier circuit application the user desires to implement. The 1206 footprint for the resistors and capacitors surrounding the U8B operational amplifier are not populated and thus are available for easy configuration. Test points TP6 and TP7 are not installed either; so, the user has the option of how to connect the ± input signals to this operational amplifier. No test point has been made available for the output due to space restriction, but a wire can simply be soldered to the output of the operational amplifier via the unused component pads that connect to it.

Once the operational amplifier circuit is realized, the configuration becomes easy by simply populating the corresponding components that match the circuit designed and leaving all other unused component footprints unpopulated.

3.6 Jumper Setting

Table 8 shows the function of each specific jumper setting of the EVM.

Table 8. Jumper Setting Function

Reference	Jumper Setting	Function
W1		+5-V analog supply is selected for AV_{DD}.
		+3.3-V analog supply is selected for AV_{DD}.
W2		Routes $V_{OUT}A$ to J4-2.
		Routes $V_{OUT}A$ to J4-6.
W3		Disconnects $V_{REF}H$ to the inverting input of the output operational amplifier, U2
		Connects $V_{REF}H$ to the inverting input of the output operational amplifier, U2
W4		Routes the adjustable, buffered, onboard +5-V reference to the $V_{REF}H$ input of the DAC8550/51/52.
		Routes the user-supplied reference from U4 (if installed), TP1 or J4-20 to the $V_{REF}H$ input of the DAC8550/51/52.
W5		Negative supply rail of the output operational amplifier, U2, is powered by V_{SS} for bipolar operation.
		Negative supply rail of the output operational amplifier, U2, is tied to AGND for unipolar operation.
W6		$\overline{CS}$ signal from J2-1 is routed to drive the $\overline{SYNC}$ signal of the DAC8550/51/52.
		FSX signal from J2-7 is routed to drive the $\overline{SYNC}$ signal of the DAC8550/51/52.
W7		For DAC8550/51EVM, the V_{FB} is routed out to minimize the output error. Remove R1 and short W7 as shown; then connect V_{FB} and $V_{OUT}A$ as close as possible to the load. The V_{FB} signal is then routed to J4-10.
		For DAC8552EVM, R1 is not installed and W7 is shorted as shown so that $V_{OUT}B$ is routed to J4-10 header terminal.
		This is the default jumper position for DAC8550/51EVM when R1 is installed.
		For DAC8550/51EVM, the V_{FB} is routed out to minimize the output error. Remove R1 and short W7 as shown; then connect V_{FB} and $V_{OUT}A$ as close as possible to the load. The V_{FB} signal is then routed to J4-14.
		For DAC8552EVM, R1 is not installed, and W7 is shorted as shown so that $V_{OUT}B$ is routed to J4-14 header terminal.
W15		Disconnects the inverting input of the output operational amplifier, U2, from the gain resistor, R12.
		Connects the inverting input of the output operational amplifier, U2, to the gain resistor, R12, for gain of 2 configuration.
Legend:  Indicates the corresponding pins that are shorted or closed.		

3.7 Related Texas Instruments Documentation

To obtain a copy of any of the following TI documents, call the Texas Instruments Literature Response Center at (800) 477–8924 or the Product Information Center (PIC) at (972) 644–5580. When ordering, identify the manual by its title and literature number. Updated documents also can be obtained through the TI Web site at www.ti.com.

Data Sheets	Literature Number
DAC8550	SLAS476
DAC8551	SLAS429
DAC8552	SLAS430
DAC8531	SBAS192
DAC8532	SBAS246
DAC8501	SBAS212
DAC7512	SBAS156
DAC7513	SBAS157
REF02	SBVS003
REF3240	SBVS058
OPA627	SBOS165
OPA2227	SBOS110

3.8 Questions About This or Other Data Converter EVMs?

If you have questions about this or other Texas Instruments Data Converter evaluation modules, send an e-mail to the Data Converter Application Team at *dataconvapps@list.ti.com*. Include in the subject heading the product with which you have questions or concerns.

3.9 Schematic

The schematic appears on the following page.

DUT can accomodate the following devices:

1) DAC8552 (MSOP-8 and SON-8)
2) DAC8551 (MSOP-8 and SON-8)
3) DAC8550 (MSOP-8 and SON-8)
4) DAC8532 (MSOP-8)
5) DAC8531 (MSOP-8)
6) DAC8501 (MSOP-8)
7) DAC7513 (MSOP-8)
8) DAC7512 (MSOP-8)

See User's Guide for more information.

Revision History		
REV	ECN Number	Approved

J2 Serial Header: CS, SCLK, CLKR, FSX, FSR, SDI, DR, GPIO5 / GPIO0, GPIO1, GPIO2, GPIO3, GPIO4, SCL, SDA

U1 DAC8551: VDD, SYNC, VFB, SCLK, VOUT, DIN, VREF, GND

U2 Op Amp: U2_+IN, U2_-IN, U2_OUT

J4 OUTPUT HEADER: OUT_A1, OUT_A2, VFB_A, VFB_B, -REFin, +REFin

U4 is OPTIONAL - Do not populate U4, C2, and R15

U4 REF3240: GND_F, OUT_F, GND_S, OUT_S, ENABLE, IN

U3 REF02AU(8): TRIM, OUT, V+, TEMP, NC, NC, GND, NC

U8A OPA2227UA

U8B OPA2227UA

J6: +3.3VD, +1.8VD, +5VA, VCC, VSS, -5VA, +3.3VA, VDD

J1: VSS, VCC

J5: +3.3VA, +5VA

VCC = +15V Analog
VDD = +2.7V to +5.0V Digital
VSS = 0V to -15V Analog

EDGE Numbers:

DAC8550EVM BOM = 6483265
DAC8551EVM BOM = 6475348
DAC8552EVM BOM = 6475349
DAC8551-2EVM PWB = 6475350
DAC8551-2EVM DDB = 6475351 (BLOCK)
DAC8551-2EVM PCA = 6475352
DAC8550EVM KIT = 6430334 (BLOCK)
DAC8551EVM KIT = 6475353 (BLOCK)
DAC8552EVM KIT = 6475354 (BLOCK)

TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243

Title: DAC8550/51/52 EVM			
Engineer: J. PARGUIAN	DOCUMENTCONTROL # 6475351		REV: A
Drawn By:	DATE: 22-Jun-2006	SIZE:	SHEET: OF: 1
FILE: DAC8551 Rev A.Sch			

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of +2.7 V to +5 V and the output voltage range of -5 V to +5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 30°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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