ADS5400EVM-CVAL

User's Guide

Literature Number: SLAU471A
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1 Overview

This ADS5400EVM-CVAL user's guide gives an overview of the EVM and provides a general description of the features and functions to be considered while using this module.

1.1 Purpose

The ADS5400EVM-CVAL provides a platform for evaluating the ADS5400HFS/EM device under various signal, reference, and supply conditions. Use this document along with the EVM schematic diagram supplied.

1.2 EVM Quick-Start Procedure

Power Supply

Power connections to the EVM are supplied by banana jack sockets.

Clock

The EVM provides an external SMA connector for input of the ADC clock. The single-ended input is converted into a differential signal at the input of the device.

Analog Inputs

The analog input to the ADC is provided by a external SMA connector. The user supplies a single-ended input or differential input (SMA connector which is not populated in the EVM). If the single-ended configuration is used, the signal is converted into the differential signal before the ADC.

1.3 Power Requirements

The EVM can be powered directly from 5 V for the ADC analog supply, or EVM jumper settings can be modified to use the onboard power solution from Texas Instruments (TI). The input power supply voltage range for the EVM can be 6 V to 36 V only if the onboard TI power solution is used.

CAUTION

Voltage Limits: Exceeding the maximum input voltages can damage EVM components. Undervoltage may cause improper operation of some or all of the EVM components.

1.4 ADS5400EVM-CVAL Operational Procedure

The ADS5400EVM-CVAL provides a flexible means of evaluating the ADS5400HFS/EM in various modes of operation. A quick-setup procedure follows.

1. Verify all jumper settings according to the schematic jumper list in Table 1.

Table 1. Jumper List

Jumper	Function	Default Jumper Setting
ADC Circuit		
JP4	EN	2-3
JP5	PWD	2-3
JP6	REFSEL	2-3
Power Supply		
JP12	3.3VA_IN	1-2
JP13	3.3VD_IN	1-2
JP14	5V_IN	1-2
JP15	TPS79501 INPUT SELECT	1-2
JP16	5V_AUX	2-3
JP17	TPS5420 INPUT SELECT	NO SHUNT

2. Connect the 5-V supply between J5 and J6 (GND), If you are using the TSW1200 for capture, it can also be used to source 5 V for the EVM. On the TSW1200, configure JP8 to short 1-2 and J22 to short 1-2 and jumper over 5 V from the banana jacks on the TSW1200 to J5 on the ADC EVM. Do not connect a voltage source greater than 5.5 V.
3. Switch on power supplies.
4. Using a function generator with 50-Ω output impedance, generate a 0-V offset, 1.5-Vpp sine-wave clock into J12. The frequency of the clock must be within the specification for the device speed grade.
5. Use a frequency generator with a 50-Ω output impedance to provide a 0-V offset, –1-dBFS-amplitude sine-wave signal into J1. This provides a transformer-coupled differential input signal to the ADC.
6. Connect the TSW1200 or suitable logic analyzer to J4 to capture the resulting digital data. If you connect a TSW1200 to capture data, follow the additional alphabetically labeled steps. For more information, see Section 3.
   (a) After installing the TSW1200 software and connecting the TSW1200 to the USB port, open the TSW1200 software.
   (b) Depending on the ADC under evaluation, select ADS5400 from the “TI ADC Selection” pulldown menu.
   (c) Change the “ADC Sample Rate” and “ADC Input Frequency” to match those of the signal generator.
   (d) After selecting a Single Tone FFT test, press the “Capture Data” button.

2 Circuit Description

2.1 Schematic Diagram

The schematic diagram for this EVM is attached at the end of this document. See the schematic before changing any jumpers.

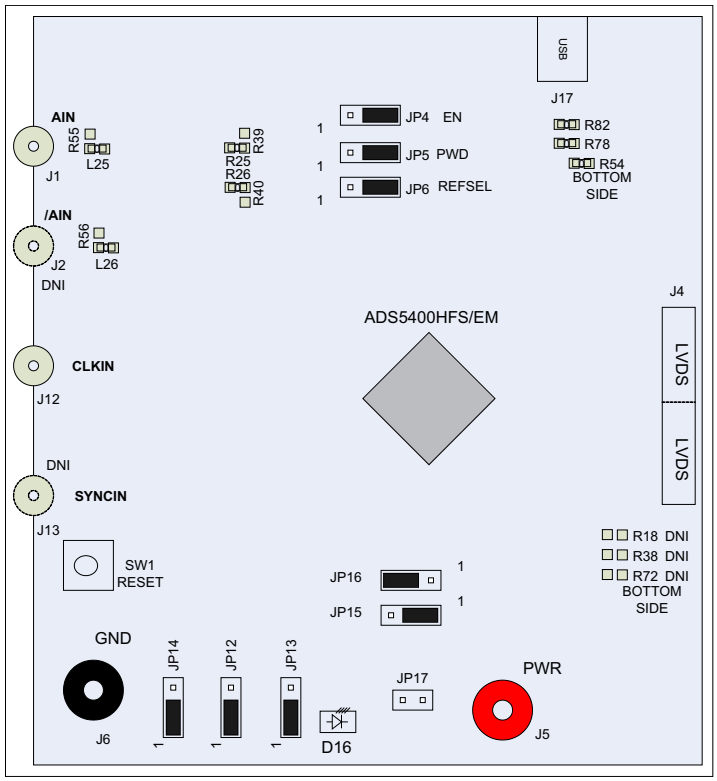

Figure 1. ADS5400EVM-CVAL Jumpers

2.2 Circuit Function

The following sections describe the function of individual circuits. See the relevant data sheet for device operating characteristics.

2.2.1 Power

Power is supplied to the EVM through a TI power solution. Although various power options are available on this EVM, care must be taken while applying power on J5 as different options have different voltage ranges specified. Table 2 displays the general jumper setting information; Table 3 displays the various power option settings. Prior to making any jumper settings, see the Figure 14 schematic.

Table 2. EVM Power Supply Jumper Description

EVM Banana Jack	Description	Jumper setting
J5	Input	5-V to 36-V power supply; default - apply just 5 V
JP12	3.3VA_IN	1-2 → Connect 3.3-V AVdd to TPS79633 output; 2-3 → Ground
JP13	3.3VD_IN	1-2 → Connect 3.3-V DVdd to TPS79633 output; 2-3 → Ground
JP14	5V_IN	1-2 → Connect 5-V AVdd to 5V_Aux; 2-3 → Ground
JP15	TPS79501 INPUT SELECT	1-2 → Connects 5.3 V to input of TPS79501; 2-3 → TPS79501 input connected to J5
JP16	5V_AUX	1-2 → TPS79501 op as 5v_Aux rails; 2-3 → 5V_aux rail connected to J5

Table 2. EVM Power Supply Jumper Description (continued)

EVM Banana Jack	Description	Jumper setting
JP17	TS5420 INPUT SELECT	Shunt → J5 connected to TPS5420D

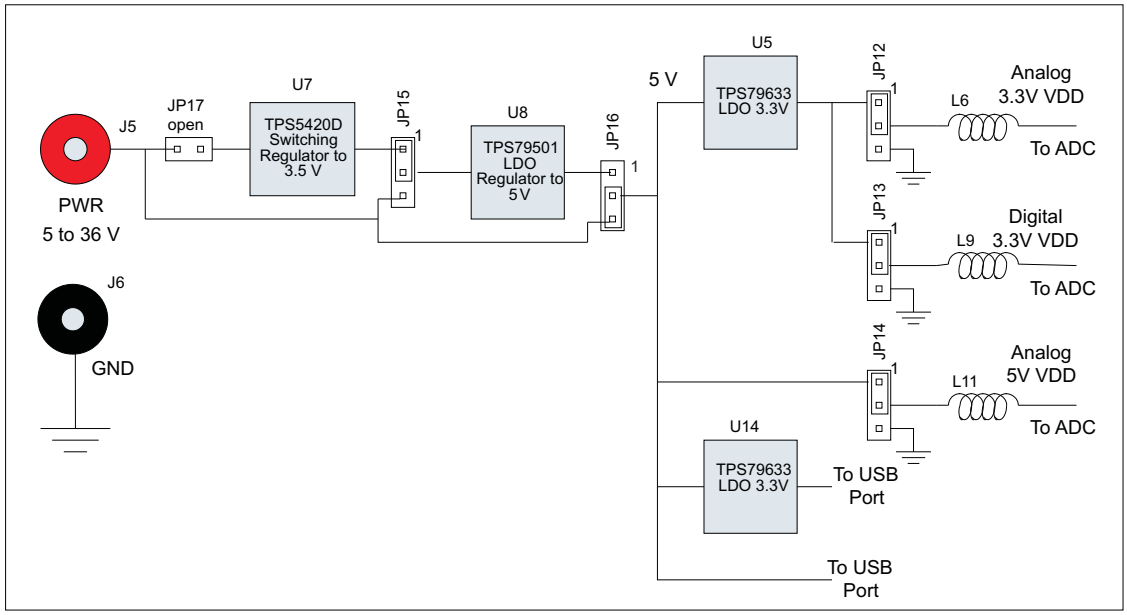

Figure 2. ADS5400EVM-CVAL Distribution

Table 3. EVM Power Supply Options

EVM Option	Evaluation Goal	Jumper Changes Required	Voltage on J5	Comments
1	Evaluate ADC performance using a cascaded switching power supply (TPS5420D) and LDO solution (TPS79501DCQ)	JP12 → 1-2; JP13 → 1-2; JP14 → 1-2; JP15 → 1-2; JP16 → 1-2; JP17 → 1-2;	6 V to 36 V	Isolates input voltage from the requirement for a clean analog supply input
2 (Default)	Evaluate ADC performance using a LDO-based solution.	JP12 → 1-2; JP13 → 1-2; JP14 → 1-2; JP15 → 1-2; JP16 → 2-3, JP17 → No shunt;	5 V to 5.5 V	Requires clean input supply as this connects to ADS5400 5-V analog supply input
3	Evaluate ADC performance using an isolated ADC AVDD and DVDD for current consumption measurements	JP12 → connect 3.3V to pin 2 of Jumper; JP13 →connect 3.3V to pin 2 of Jumper; JP14 → connect 5 V to pin 2 of Jumper and ground to J6; JP15 →No shunt ; JP16 →No shunt ; JP17 → No shunt;	Do not apply power on J5.	Separates power inputs for analog and digital for individual current consumption measurements

2.2.1.1 Power Supply Option 1

Option 1 supplies the power to the ADC using cascaded topology of the TPS5420D and the TPS79501DCQ. The TPS5420 is a step-down converter which works with the input voltage in the range of 6 V to 36 V. The switching supply increases efficiency for higher input voltages but does create noise on the voltage supplies. To reduce the noise, an ultralow-noise, high-PSSR LDO TPS79501DCQ is used to clean the power supply. The TPS5420D is designed for output of 5.3 V, which acts as input for TPS79501. The TPS79501 is designed to output a 5-V output, which is the AVDD for the ADC. This voltage rail is

input to the LDO TPS79633, which outputs 3.3 V, used for DVDD for the ADC. This solution adds two features to the EVM: one is to increase the range of the power supply on jumper J5 from 6 V to 36 V, allowing the user to choose any power supply source in the specified range without causing significant power dissipation. The other feature is that the output voltage rail has a much lower ripple, ensuring the better performance of the part even when the power source is fluctuating.

2.2.1.2 Power Supply Option 2, Default

Option 2 supplies power to the ADC using the LDO TPS79633DCQ. The LDO limits the power supply on J5 to be in the range 5 V to 5.5 V only. This option again has the output voltage much cleaner as the LDOs chosen have high PSSR and low noise. Care must be taken while powering up the EVM using this option, as higher voltage or reverse polarity may damage the EVM.

2.2.1.3 Power Supply Option 3

Option 3 is used to evaluate ADC performance using an isolated AVDD and DVDD power supply for current consumption measurements. This option must be used with caution as reversing the power supply or connecting to the wrong connector can result in damage to the EVM.

2.2.2 Clock Input

The clock can be supplied to the ADC from J12 directly from an external source. For the direct supply of the clock to the ADC, a single-ended square or sinusoidal clock input must be applied to J12. The clock frequency must be within the maximum frequency specified for the ADC. The clock input is converted to a differential signal by a Mini-Circuits™ JTX-4-10T (1), which has an impedance ratio of 4, implying that voltage applied on J12 is stepped up by a factor of 2. ADC performance in this case depends on the clock source quality. The single-ended option is also the default configuration on the EVM, when it is shipped from the factory. The test result using this option is shown in Figure 4.

2.2.3 Analog Inputs

The EVM is configured to use a transformer-coupled input from a single-ended source. The SMA connector J1 provides the inputs. The SMA connector J2 provides an option for a differential input, which is not populated. To set up for one of these options, the EVM must be configured as per the options listed in Table 5. See the Figure 11 schematic prior to making any jumper changes .

(1) Earlier versions of the ADS5400EVM-CVAL might have the ADT4-1WT populated as the clock transformer. The ADT4-1WT is rated up to 775 MHz while the JTX-4-10T is rated up to 1 GHz. The footprint on the EVM for this component (T3, please see the bill of materials in section 5.3) works for both transformers. The JTX-4-10T is the recommended transformer to populate although both will make the device to clock.

Table 4. Analog Input Jumper description

EVM Banana Jack	Description	Jumper setting
J1	Analog input Single ended.	
J2	Analog input, can be used with J1 for differential input	Not populated

Table 5. EVM Analog Input Options

EVM Option	Evaluation Goal	Jumper Changes Required	Voltage on J7 and J9	Analog signal to ADC	Comments
1	Evaluate ADC performance using direct single-ended input to ADC.	L25, L26, R25, and R26 installed with 0 Ω	Do not connect	From J1	Default
2	Differential input	L26, R39, R40, and R55 installed with 0 Ω	Do not connect	From J1, J2	

2.2.3.1 Analog Input Option 1

Option 1 supplies the transformer coupled input from J1 to ADC. This configuration is the default on the EVM. The test result using this option is shown in Figure 4.

The transformer footprint used on the ADS5400EVM-CVAL is flexible to accommodate either transformers or baluns from several suppliers. If baluns are installed, then the signal must be AC coupled to the ADS5400HFS/EM so that the common-mode biasing circuits in the input may bias the signal to the desired common-mode level. AC coupling capacitors C128 and C129 on the EVM serve this purpose. By default, a dual balun (Minicircuits ETC1-1-13) is installed on the ADS5400EVM-CVAL. Depending on the input frequency to be evaluated, it may be desirable to select a different transformer or balun component more suited to a particular frequency range.

2.2.3.2 Analog Input Option 2

Option 2 allows the use of a differential input applied to two SMA connectors, and the differential input signal then bypasses the transformer coupling. By default, the SMA connector for the negative side of the differential input is not assembled on the EVM and must be added before this option is used. By default, component L25 is assembled with a 0-ohm jumper resistor to steer the positive side of the differential input to the transformer input. This 0-Ω resistor must be moved from component location L25 to component location R55 to steer the signal around the transformer coupling. Then the 0-Ω resistors R25 and R26 must be removed and installed instead in locations R39 and R40. This completes the differential path from J1 and J2 to the analog inputs of the ADS5400HFS/EM.

2.2.4 Digital Outputs

The LVDS digital outputs can be accessed through the J4 output connector. A parallel 100-Ω termination resistor must be placed at the receiver to properly terminate each LVDS data pair. These resistors are required if the user wants to analyze the signals on an oscilloscope or a logic analyzer. The ADC performance also can be quickly evaluated using the TSW1200 boards as explained in next section.

2.2.5 Sync Input

The ADS5400HFS/EM analog-to-digital converter device features a Reset input pin that may also be referred to as a Sync input pin, depending on the mode of operation of the device. When the LVDS output clock for the ADS5400HFS/EM is operating in DDR mode, it may be desirable to reset the output clocking circuitry to put the phase of the DDR clock in a known position, particularly if multiple ADS5400HFS/EM devices are to be synchronized. Also, a pulse on the Reset/Sync input pin results in a SYNCOUT output pulse if SYNC mode is enabled.

Because the ADS5400EVM-CVAL has a single ADS5400HFS/EM device installed on it, it is unnecessary to use the Reset/Sync input for normal evaluation, and the TSW1200 does not require the Reset/Sync pin to be used. Nevertheless, the ADS5400EVM provides mechanisms for using the Reset/Sync input.

The default configuration of the ADS5400EVM-CVAL provides for switch SW1 to assert a reset pulse to the Reset/Sync input pin. An LVDS buffer device converts the pulse from the switch to a differential input to the ADS5400HFS/EM. Because the switch SW1 is not synchronized to the sample clock at all, setup and hold timings between the resulting reset input and the sample clock cannot be ensured. Switch SW1 is simply a way to assert the signal to see what effect the Reset/Sync input may have on the device. Pressing switch SW1 may have about a 50% probability of inverting the phase of the LVDS DDR output clock

The Reset/Sync input may be used as a periodic SYNC input that causes a SYNCOUT output signal useful for synchronizing the sample data across multiple data converters or to some external event. The SYNC input in this case must meet setup and hold timing relationships relative to the input sample clock. To facilitate this mode, the ADS5400EVM-CVAL has an SMA input J13 (normally not installed) that is converted to differential by transformer coupling to the Reset/Sync input pins in a path that is matched both in schematic and layout with the sample clock input path. Thus, if clock and sync signals are generated and synchronized externally, then the ADS5400EVM preserves their timing relationship up to the input pins of the ADS5400HFS/EM. To enable the transformer-coupled SYNC input from J13, resistors R30 and R33 are to be removed and AC coupling capacitors C66 and C71 are to be installed.

3 Evaluation

3.1 TSW1200 Capture Board

The TSW1200 board can be used to analyze the performance of the EVM. The TSW1200EVM assists designers in prototyping and evaluating the performance of high-speed ADCs that feature parallel or serialized LVDS outputs. The TSW1200 has the LVDS 100-Ω termination resistor on the input interface for ADC outputs.

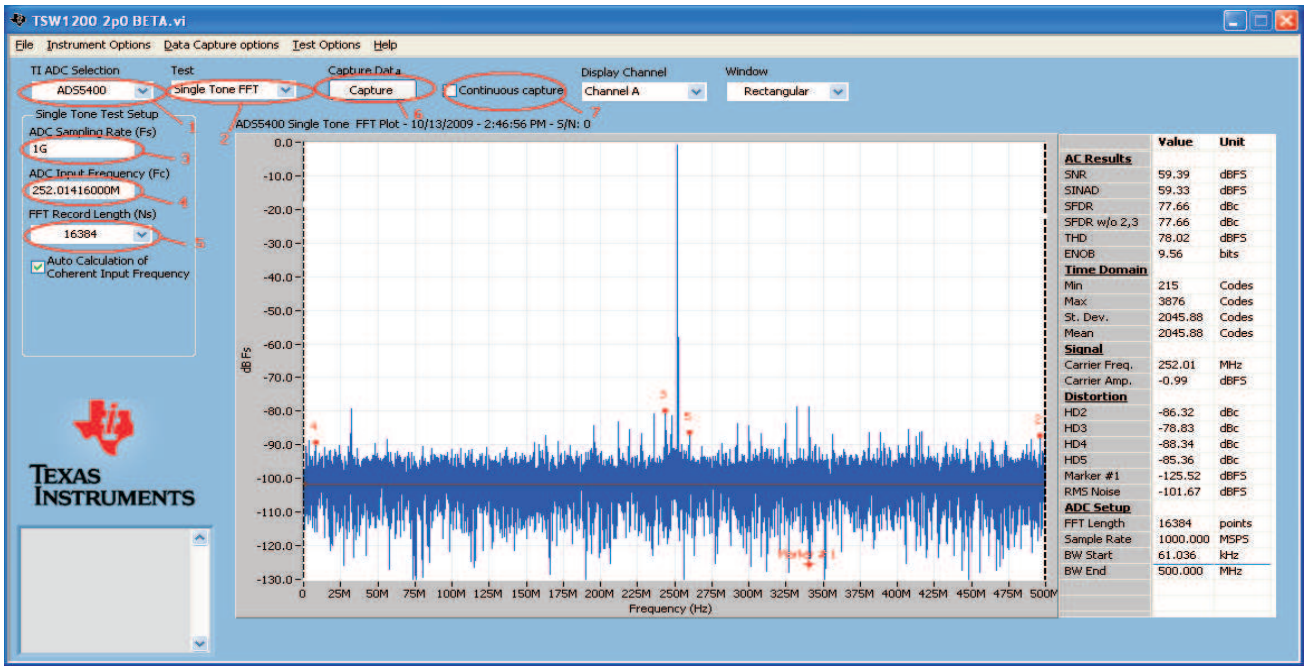

Figure 3. TSW1200 GUI Introduction

Start the TSW1200 software as follows.

1. Select the ADC type to be used before capturing.
2. For test, select Single Tone FFT plot.
3. For the ADC Sampling Rate, type in the value.
4. Type in the ADC Input Frequency. Auto calculation of the input frequency depends on the FFT record length. As soon as the number is entered, the software calculates the coherent input frequency corresponding to that FFT length. This frequency signal must be supplied through the signal generator.
5. Select the FFT Record Length.
6. Select Capture to obtain the plot
7. The Continuous Capture option is used if the user wants to continuously capture the FFT.

Be sure to adjust the input level signal to attain the dBFs of approximately -1.

3.2 Quick-Test Results

The user can make the jumper setting as mentioned in Table 1. In this configuration, the EVM uses an external clock source from J12 and a direct input signal J1 to the ADC. This setup uses Power Option 2 (Table 3) and Analog Input Option 1 (Table 5), which is the default on the EVM. Figure 4 shows the ADC performance capture using TSW1200 with the input signal of a 252-MHz frequency and clock frequency of 1000 MHz with the ADS5400HFS/EM.

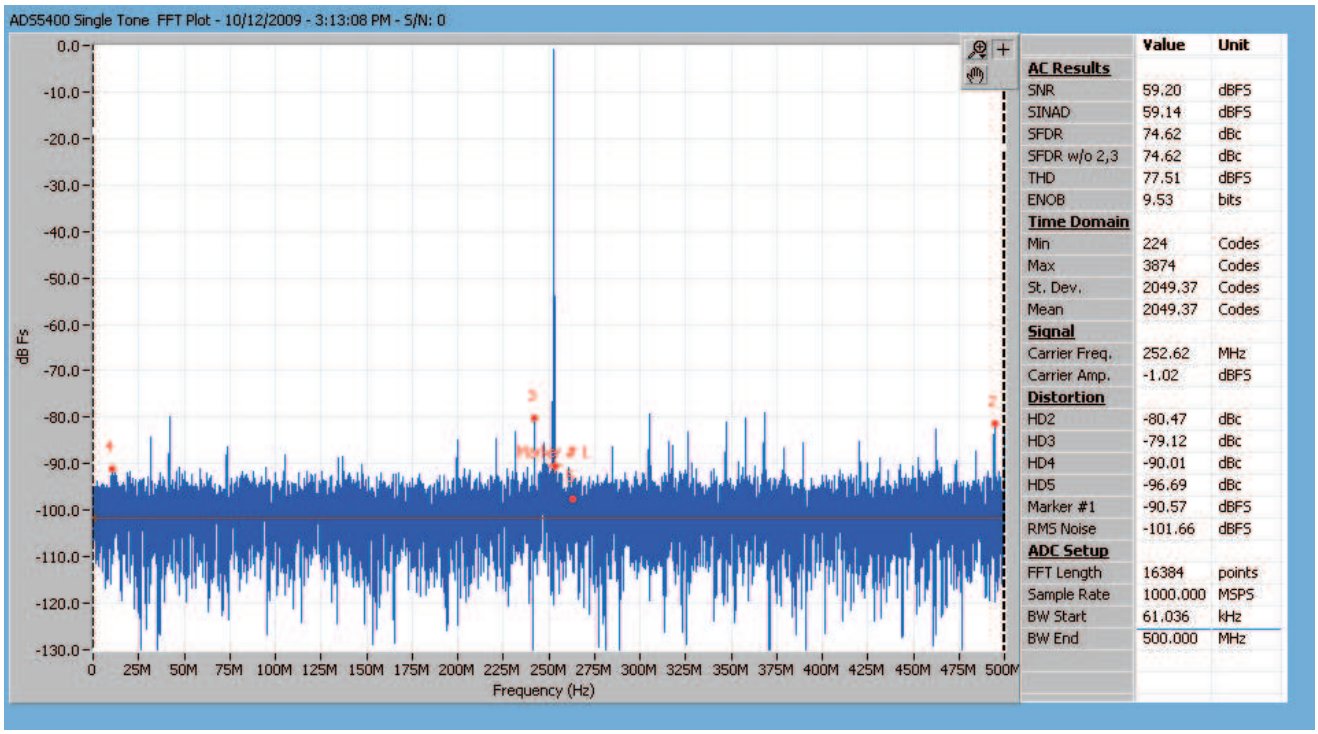

Figure 4. Quick-Setup Test Result.

4 SPI Interface

This section describes the SPI control interface, installation of the GUI for SPI, and its usage. This EVM can use SPI in two ways. One is through the TI ADC SPI Control Interface and another is using TI TSW1200EVM Software 2.0. This section describes both methods in detail.

4.1 TI ADC SPI Interface

This section describes the software features of the EVM kit. The TI ADC SPI control software provides full control of the SPI interface, allowing users to write to any of the ADC registers found in the data sheet. For most ADS5400HFS/EM performance evaluations, users do not need to use the TI SPI control software. They only need to use the ADC SPI control software when the desired feature is inaccessible through the ADC parallel interface mode.

4.1.1 Installing the TI ADC SPI Interface

ADC SPI control software can be installed on a personal computer by running the setup.exe file located on the CD. This file installs the graphical user interface (GUI) along with the USB drivers needed to communicate with the USB port that resides on the EVM. The software installation provides for installation in a default directory, which the user may change to some other directory path if desired, as shown in Figure 5. After the software is installed, insert the USB cable in the EVM to complete the installation. The Found New Hardware wizard starts and when prompted, users must allow the Windows™ operating system to search for device drivers by checking "Yes, this time only" as seen in Figure 6. The Found New Hardware wizard automatically finds TI ADC SPI Interface drivers. When prompted that the TI ADC SPI Interface has not passed Windows Logo Testing, select "continue anyway" as shown in Figure 5 and Figure 6. After completion, the TI ADC SPI Interface shows up in the Hardware Device Manager. Figure 7 shows the SPI interface in the Hardware Device Manager which indicates that it is ready for use.

NOTE: Before plugging in the USB cable for the first time, install the TI ADC SPI software. The software installs the drivers necessary for USB communication.

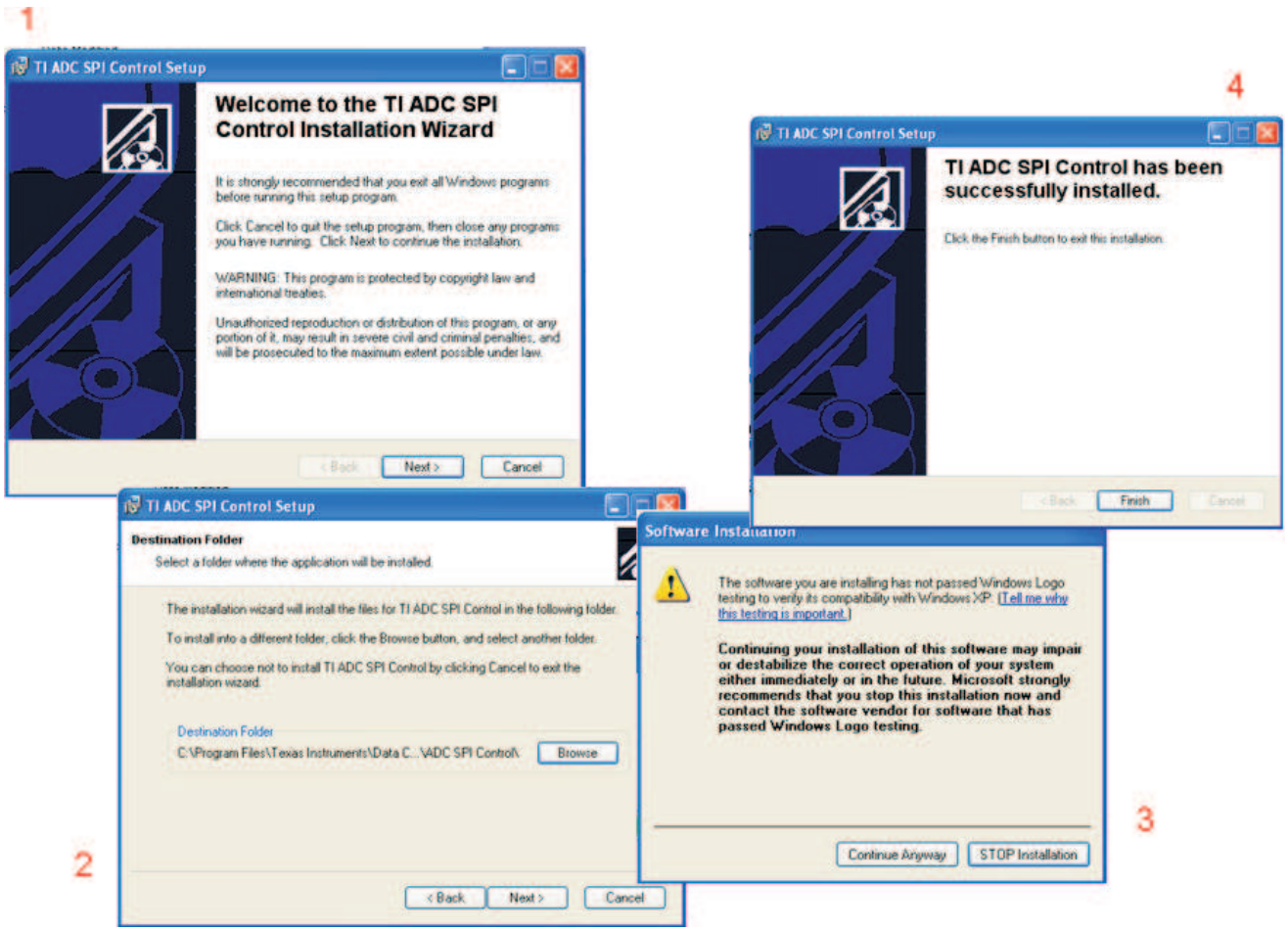

Figure 5. SPI Install Screens

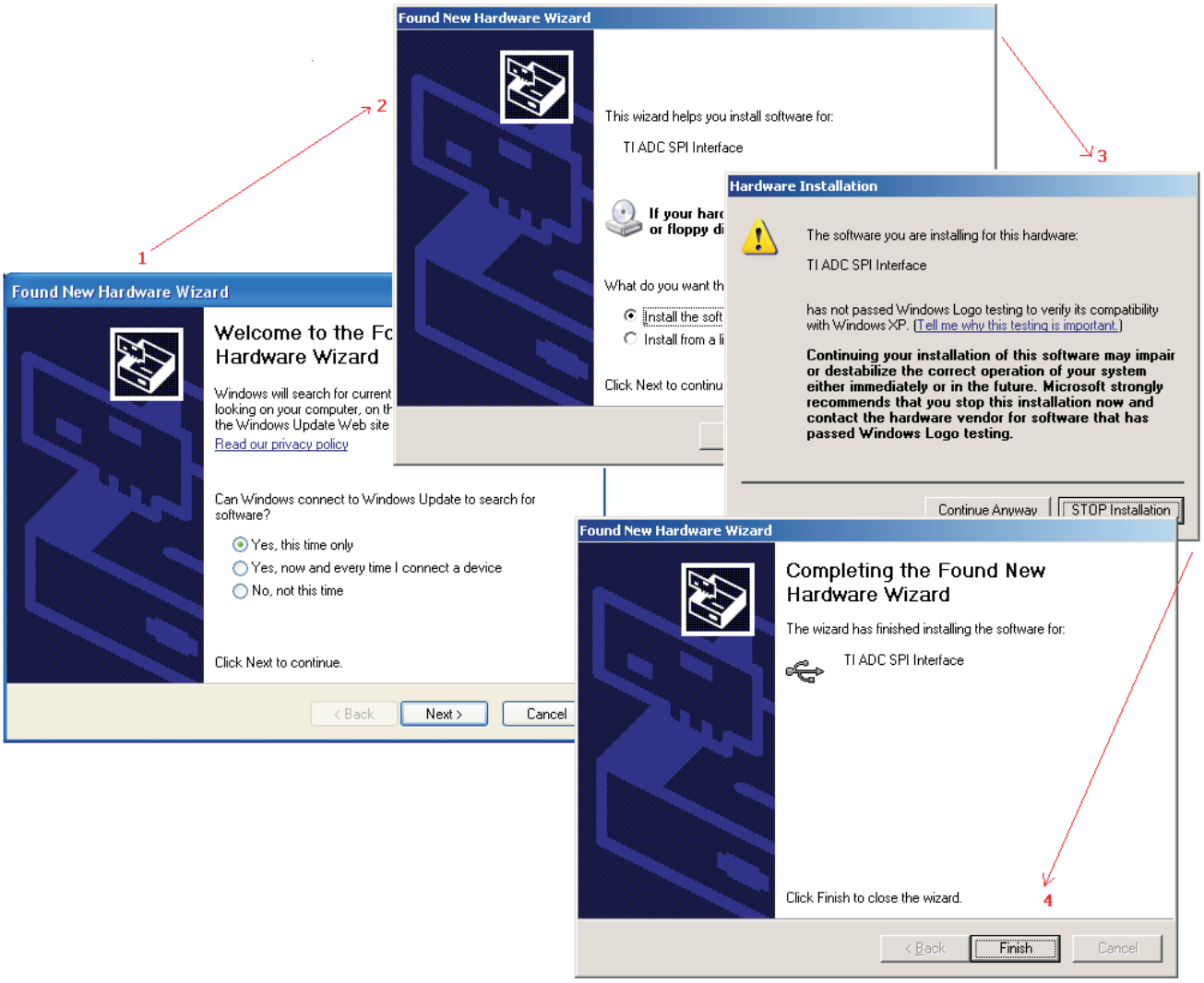

Figure 6. Found New Hardware

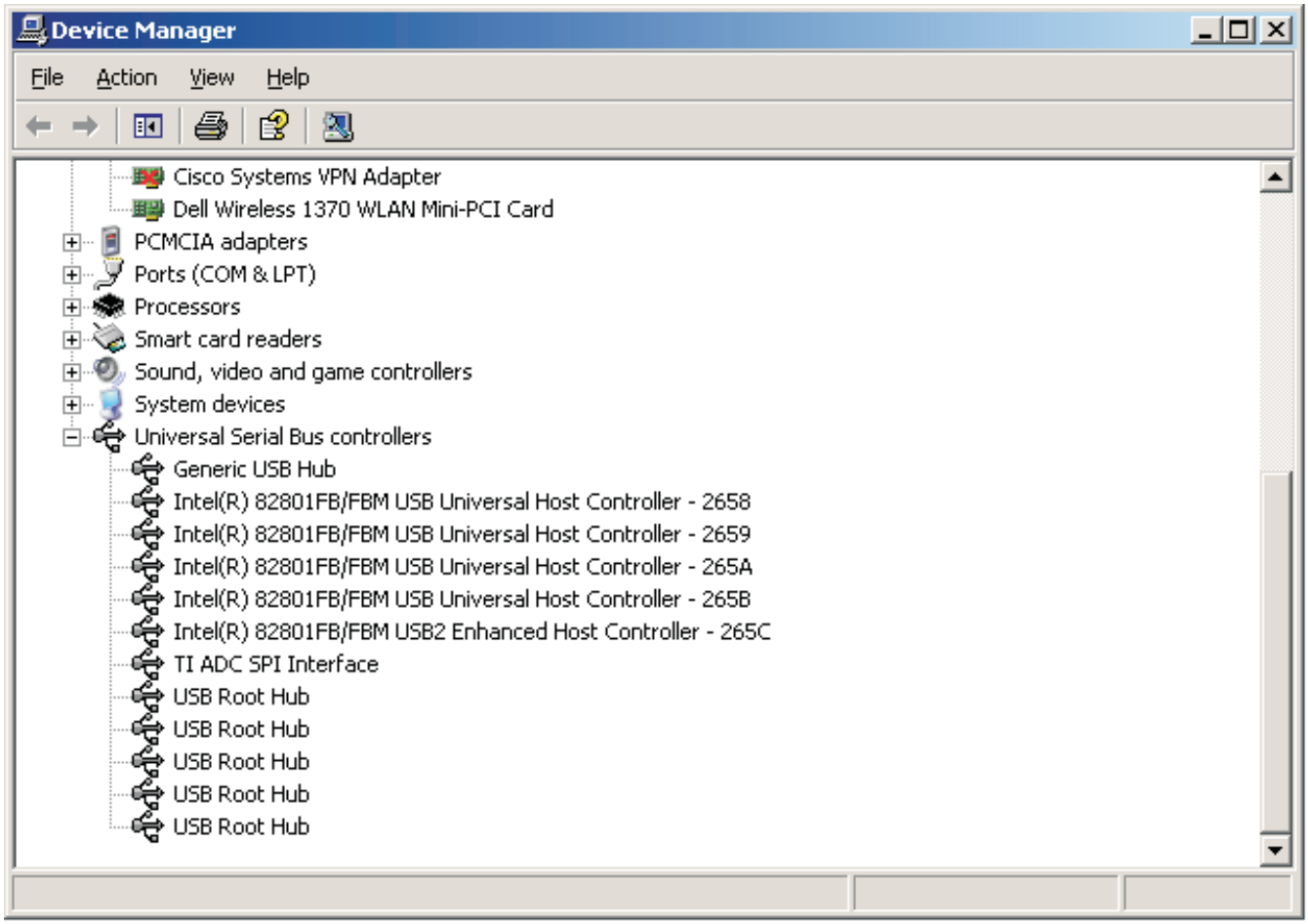

Figure 7. Hardware Device Manager

4.1.2 Using the TI ADC SPI Interface

By default, the ADS5400EVM-CVAL is configured to allow the register space in the ADS5400HFS/EM to be accessed by way of the TI ADC SPI User Interface. The TI ADC SPI User Interface has tabs across the top of the User Interface window to choose the family of ADC EVM. At this time, the ADS5400HFS/EM SPI format does not yet have a tab and is chosen instead by selecting the Register Interface tab and then leaving the format selection on Select ADC. Later revisions of the TI ADC SPI User Interface may add a device tab labeled as ADS5400HFS/EM.

The TI ADC SPI User Interface allows write access to the register space of the ADS5400HFS/EM. First, the address of the register to be written is entered in the Address Byte field. Then the data value to be written is entered in the Data Byte field. The write operation can then be completed by either pressing the Send Data button or by hitting Enter on the keyboard. Both the address and data are by default entered in hexadecimal notation, but the User Interface allows for the use of decimal, octal, or binary data formats as well by using the mouse to change the data format from x to d, o, or b.

The address field of the register space in the ADS5400HFS/EM is 5 bits long. Three additional bits in the SPI definition for the ADS5400HFS/EM are not currently supported by the SPI User Interface, and these three additional bits (for read/write direction and for number of bytes to be written) must be set to 0 for use with the SPI software. For example, a write to address 0b00101 binary is written to 0b00000101 in binary or 0x05 in hexadecimal using the SPI User Interface. Later revisions to the SPI software may enable the use of read-back from the SPI register space, but that is unsupported at this time.

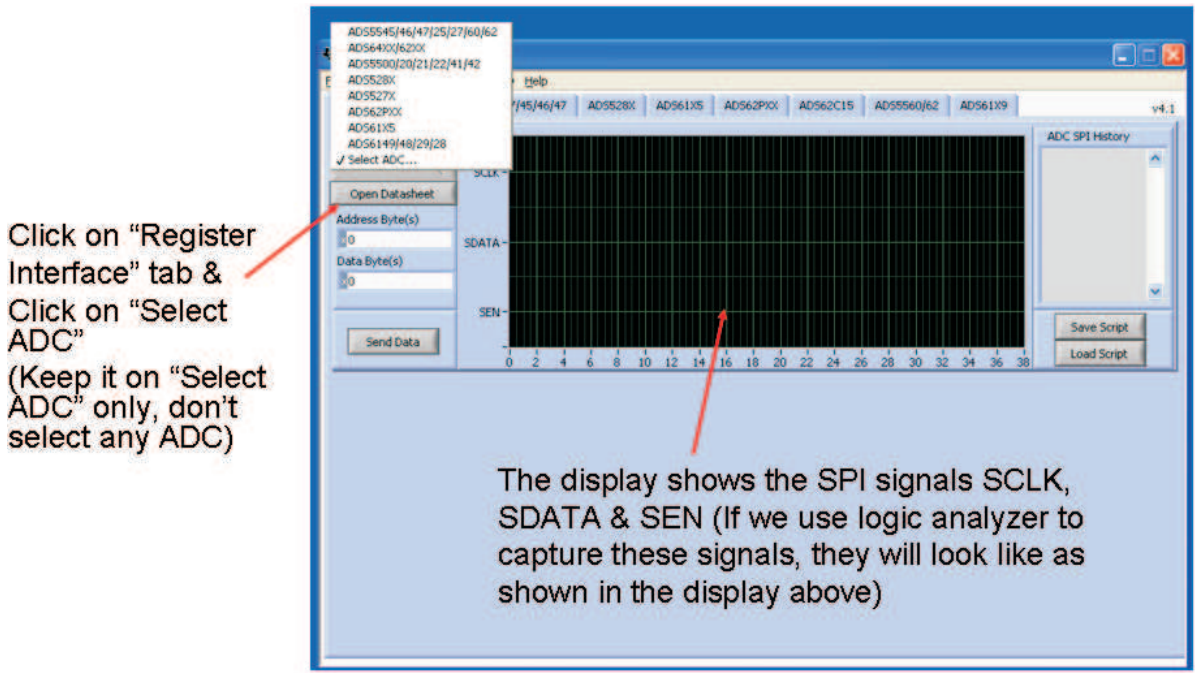

Figure 8. SPI Program Format

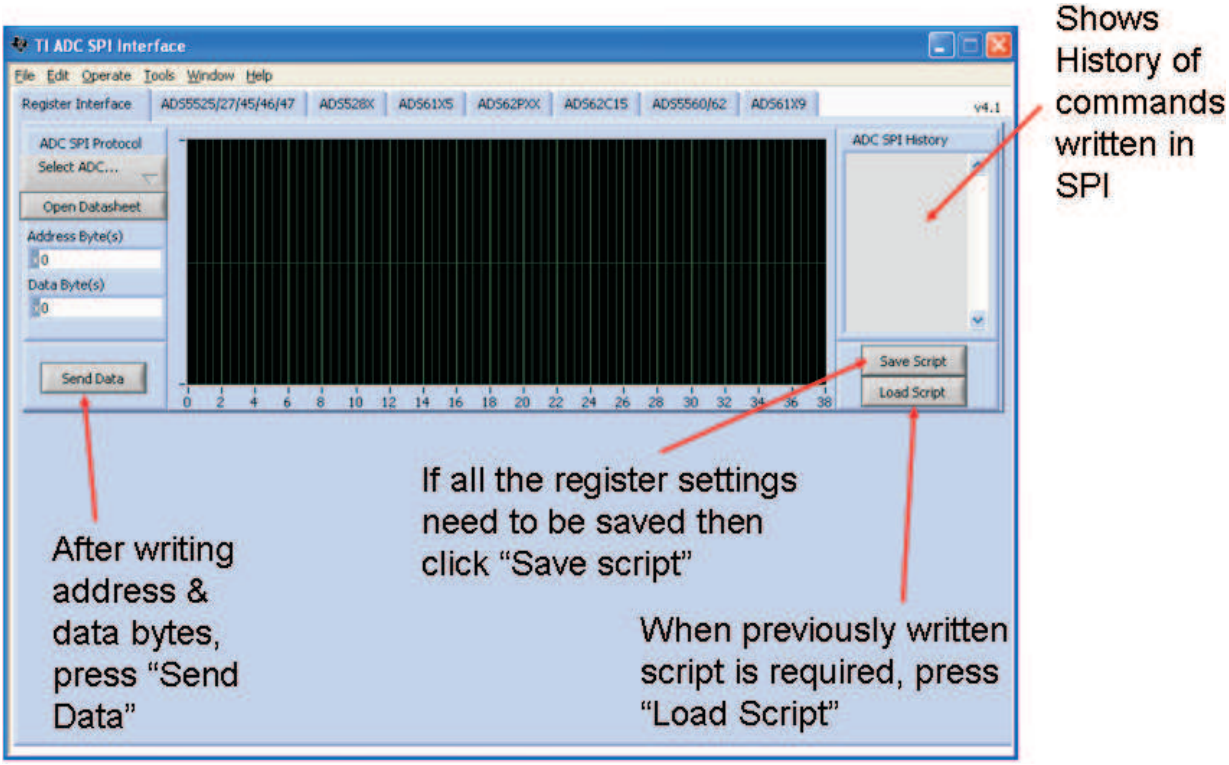

Figure 9. SPI Program Usage

4.2 Controlling the SPI Interface Using TI TSW1200 Software 2.0

The ADS5400EVM-CVAL provides an option for the TSW1200 to drive the SPI interface to perform register writes to the ADS5400HFS/EM register space. To enable this option, the 0-Ω resistors installed in locations R54, R78, and R82 must be removed and installed in locations R18, R38, and R72 instead. This connects the SPI signals SCLK, SEN, and SDATA to the TSW1200 connector J4 instead of to the USB port on the EVM.

The TSW1200 User Interface revision 2.0 or newer includes a SPI control pane as shown in Figure 10. Much like the TI ADC SPI User Interface, the SPI pane of the TSW1200 User Interface allows register accesses to be specified in terms of address byte and data byte. The Send Data button causes the registers accesses listed in the SPI Command Queue to be written to the ADS5400HFS/EM. Unlike the TI ADC SPI Interface, the TSW1200 User Interface allows several register accesses to be entered into the Command Queue, and then pressing the Send Data button causes the whole queue to be written at once.

The benefit of using the Command Queue to queue up register accesses is that once a commonly used string of register accesses are listed in the command queue, the queue may be saved under a command name, and loading this command name later fills the queue with the string of register accesses and then the send data button writes the queue to the ADC. This simple mechanism of creating a script of register writes may be more convenient for frequently used sequences of register writes. Also, if a register access is typed incorrectly, then by writing to the queue before sending the data to the device allows for the chance to clear the queue and start over on typing in the register accesses.

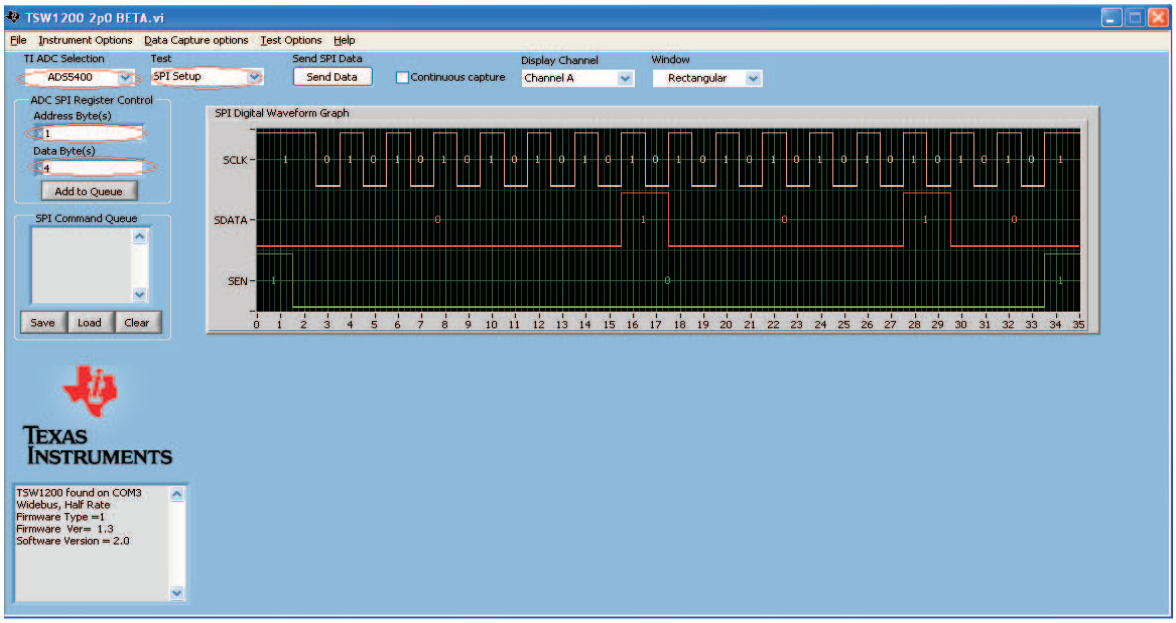

Figure 10. TI TSW1200 SPI Interface

5 Physical Description

This section describes the physical characteristics and printed-circuit board (PCB) layout of the EVM.

5.1 PCB Schematics

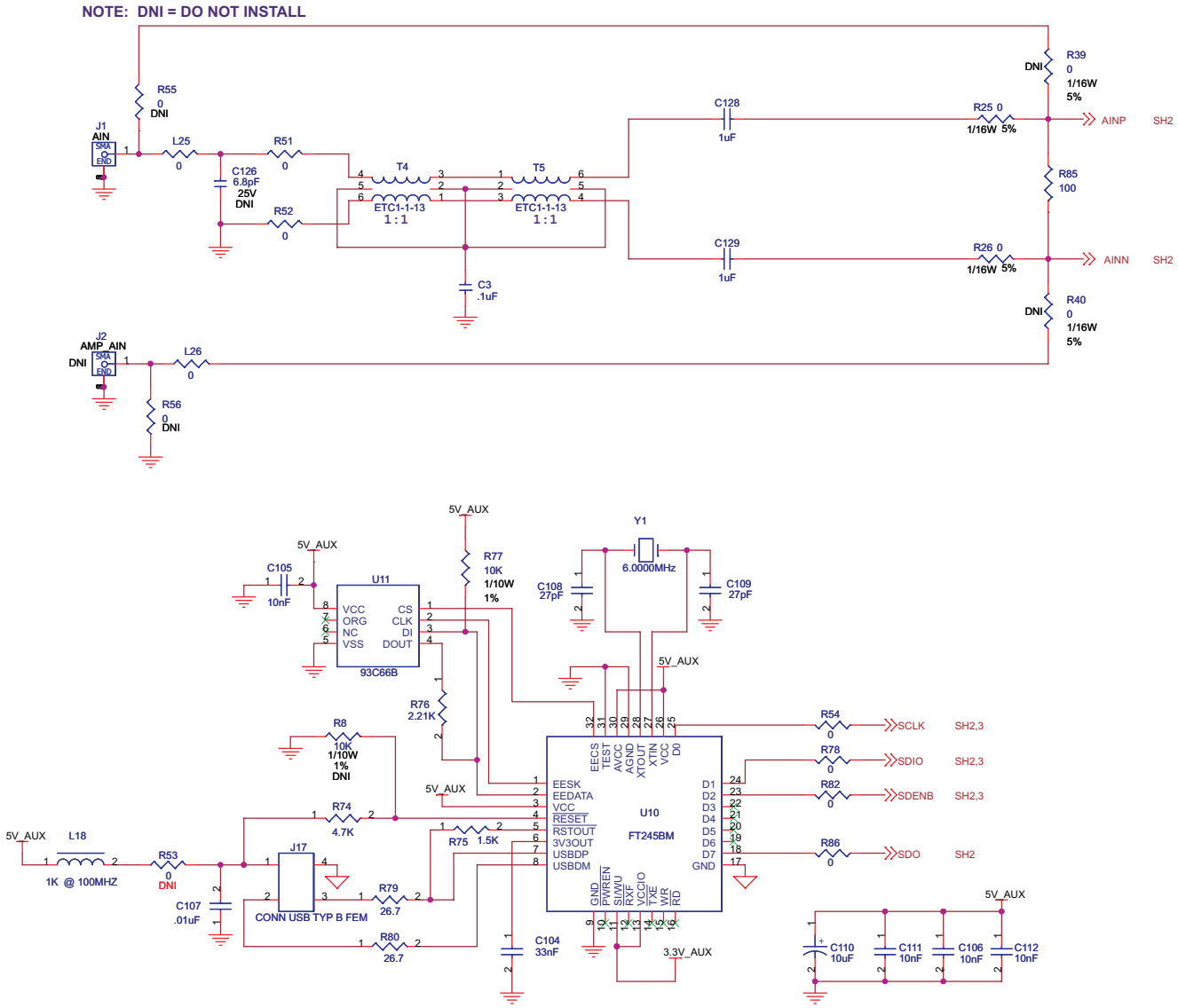

Figure 11. EVM Schematics, Sheet 1

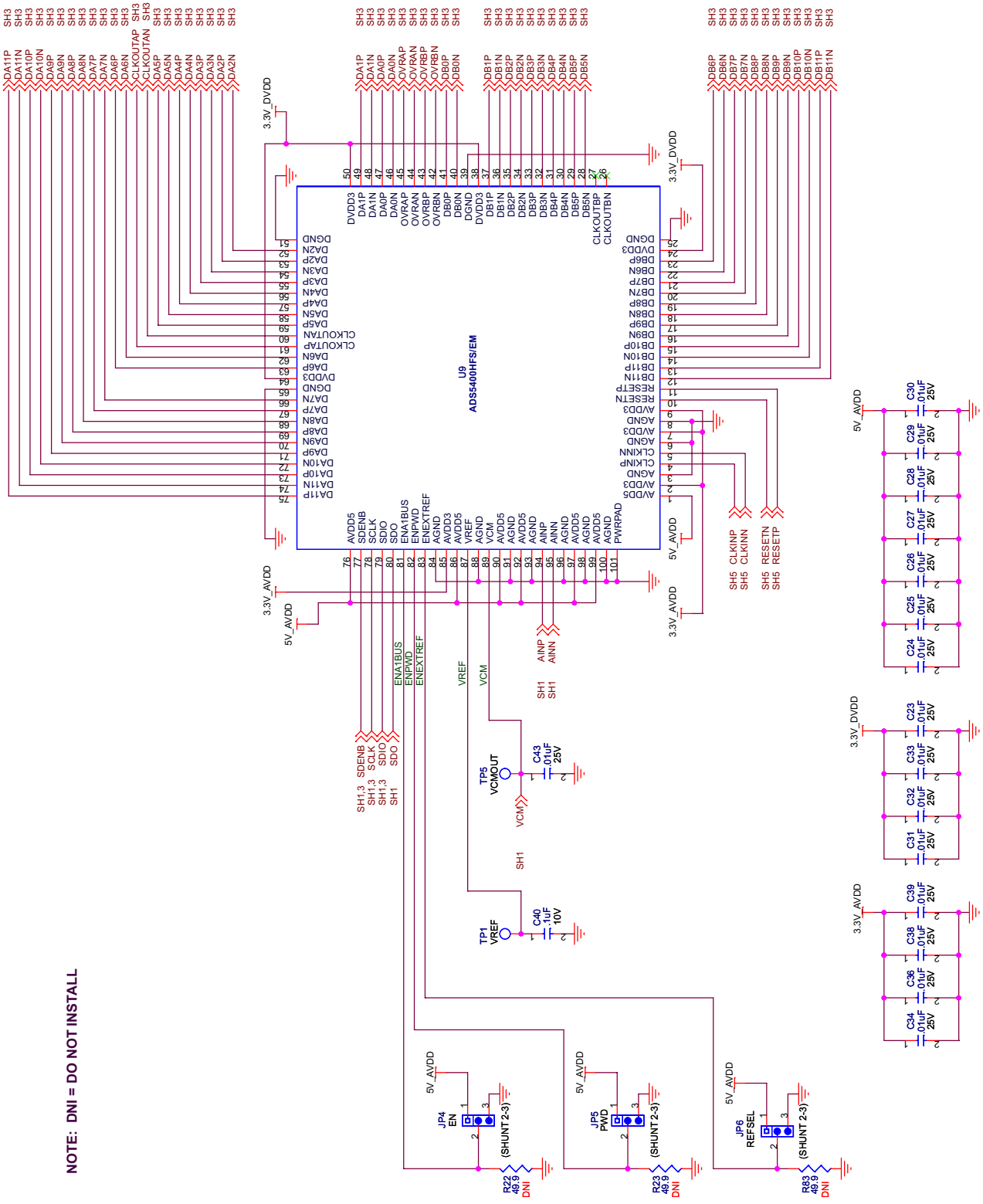

Figure 12. EVM Schematics, Sheet 2

NOTE: DNI = DO NOT INSTALL

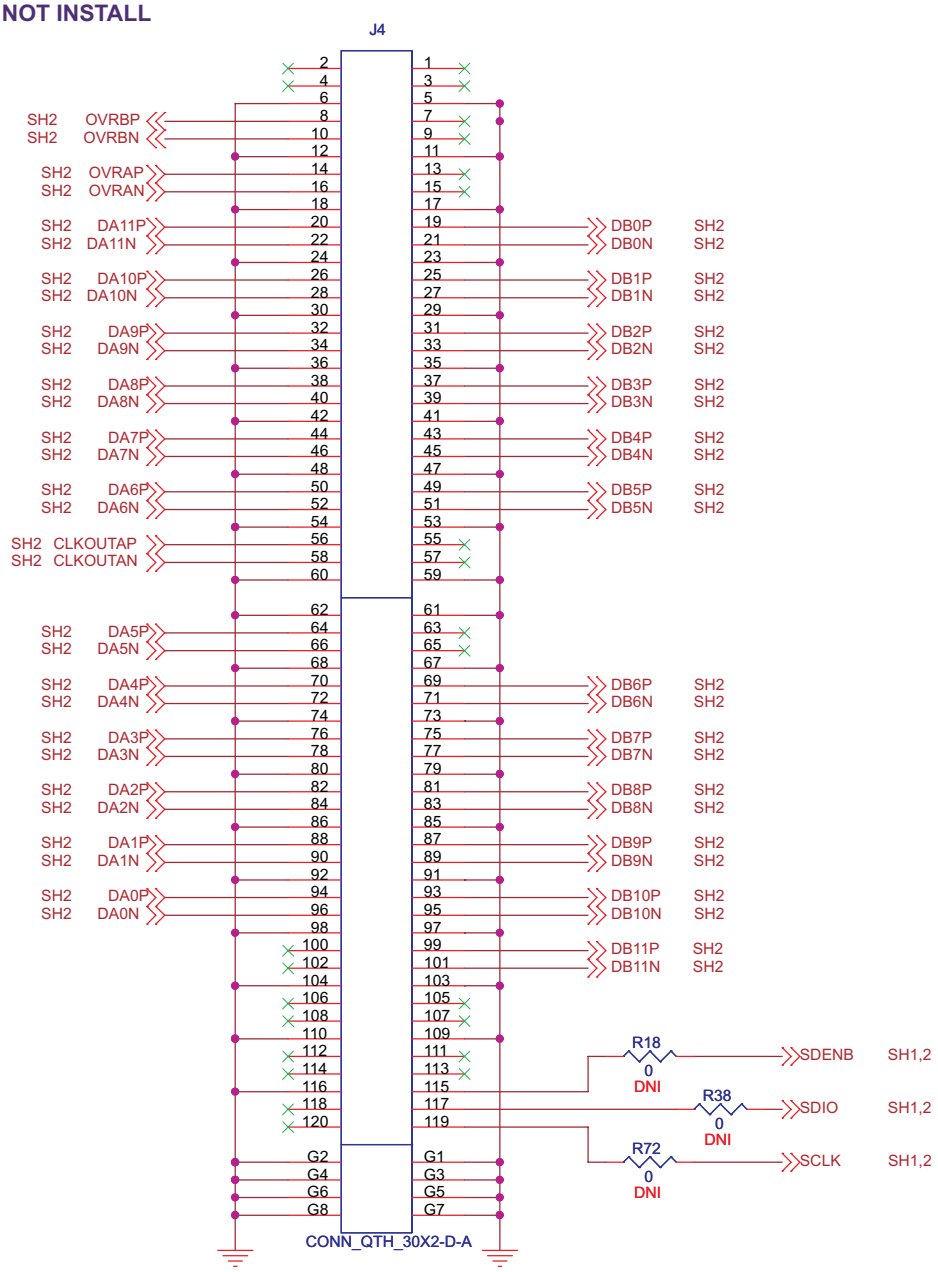

Figure 13. EVM Schematics, Sheet 3

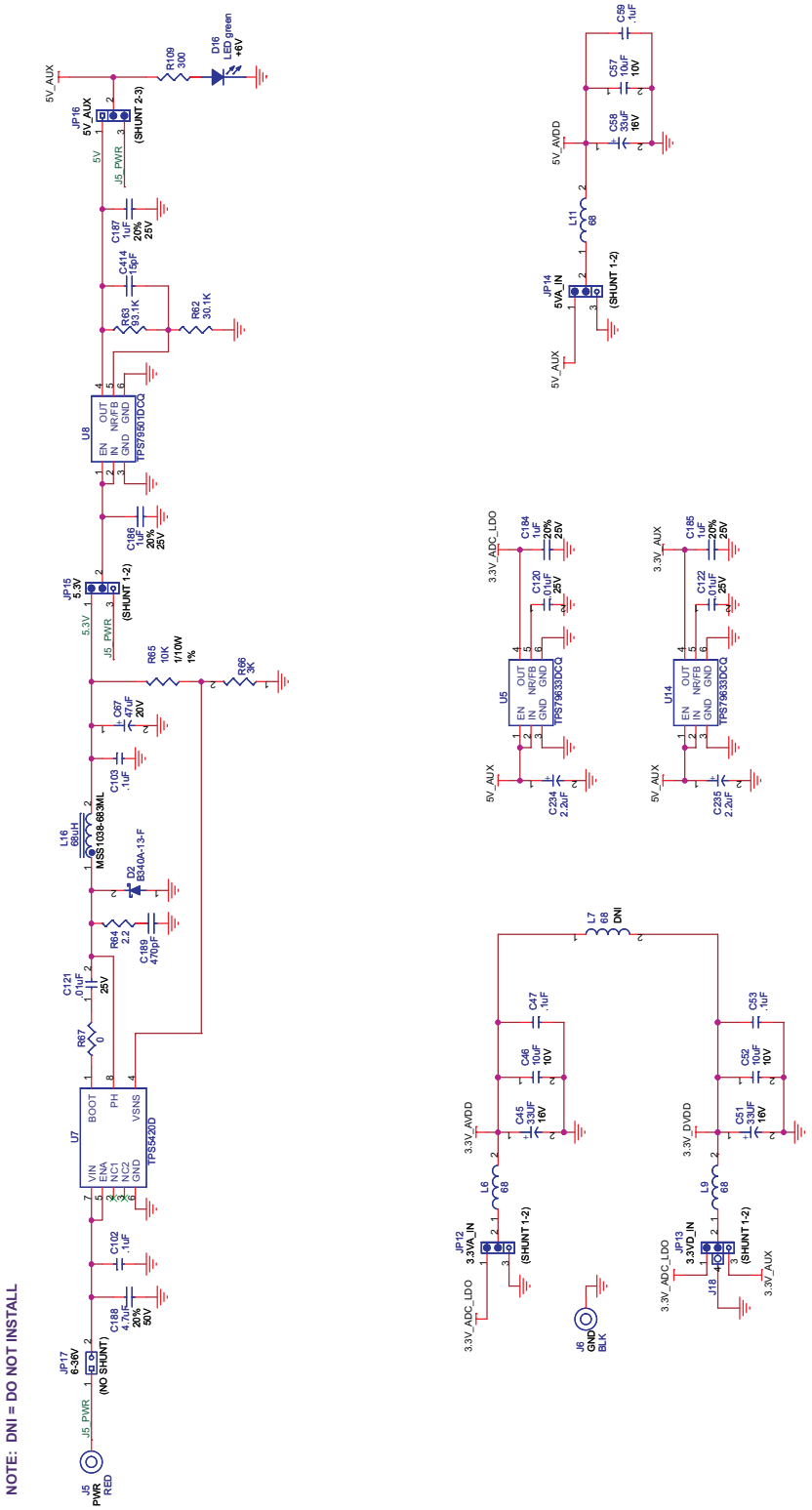

Figure 14. EVM Schematics, Sheet 4

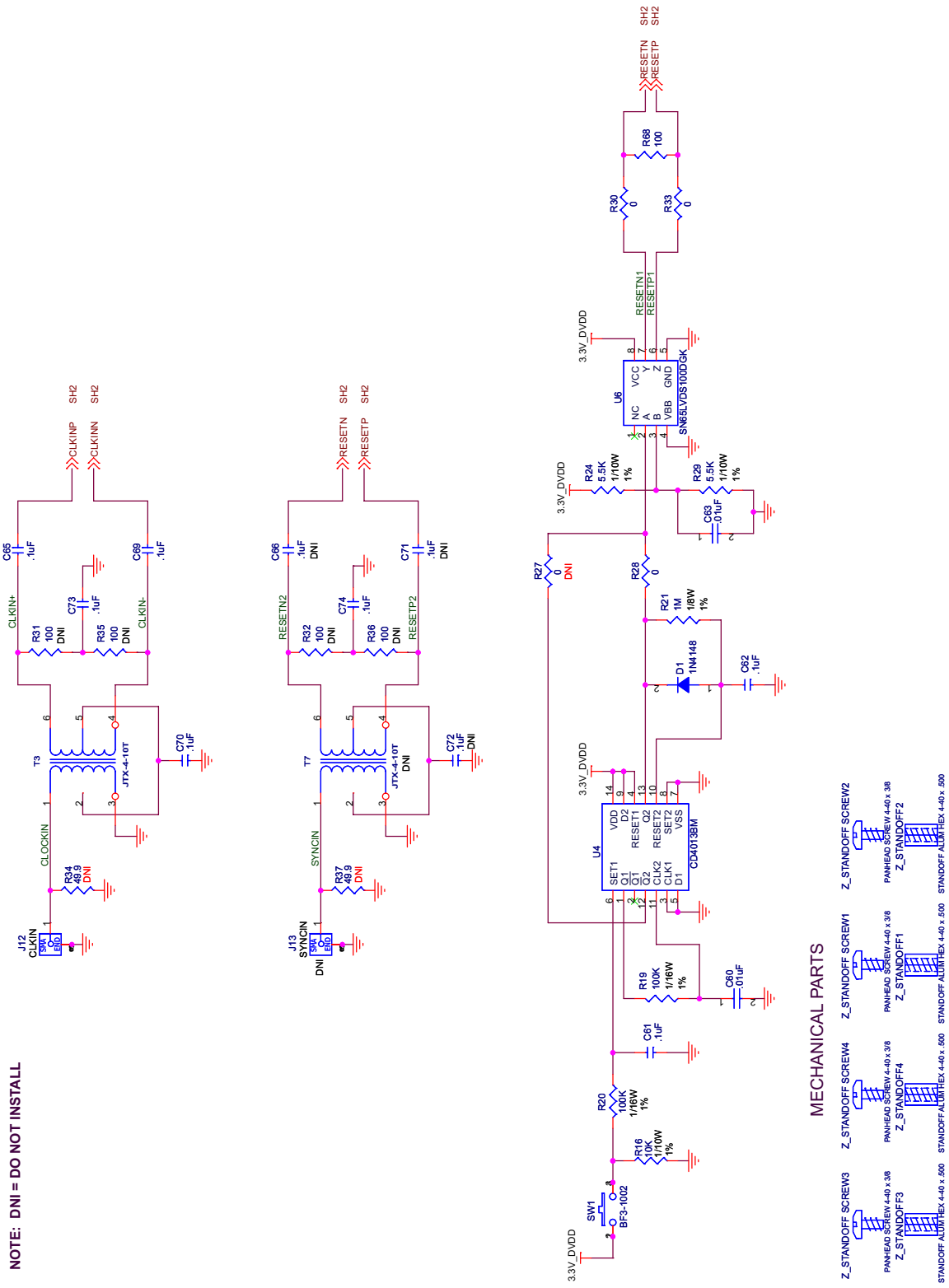

Figure 15. EVM Schematics, Sheet 5

5.2 PCB Layout

The EVM is constructed on a six-layer, 0.062-inch-thick printed-circuit board (PCB) using FR-4 material. The individual layers are shown in Figure 16 through Figure 21. The layout features a common ground plane; however, similar performance can be obtained with careful layout using a split ground plane.

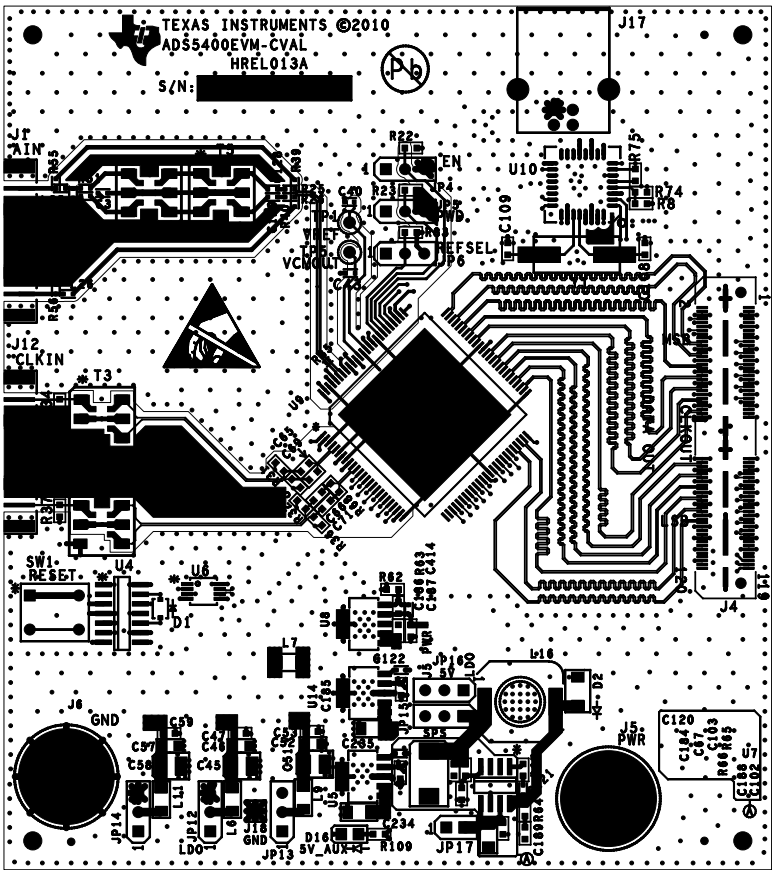

Figure 16. Component Side

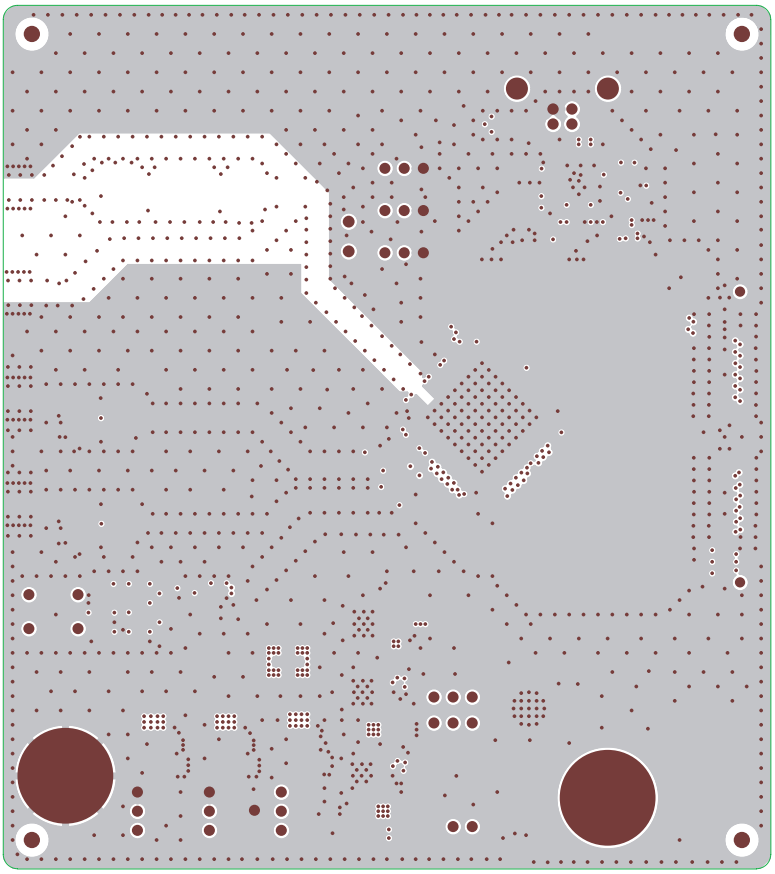

Figure 17. Ground Plane 1

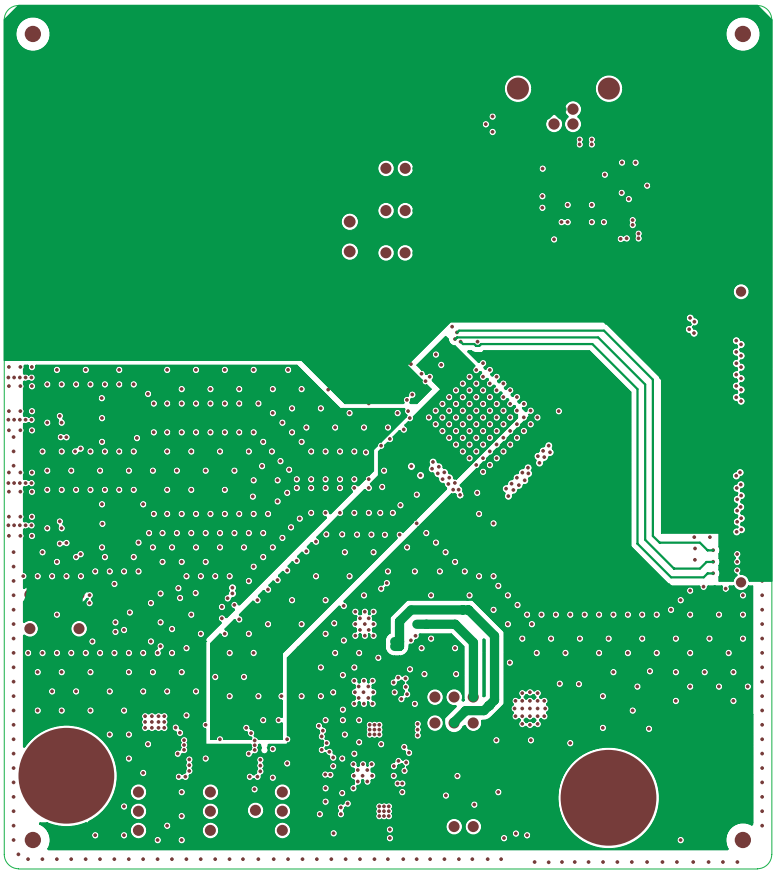

Figure 18. Power Plane 1

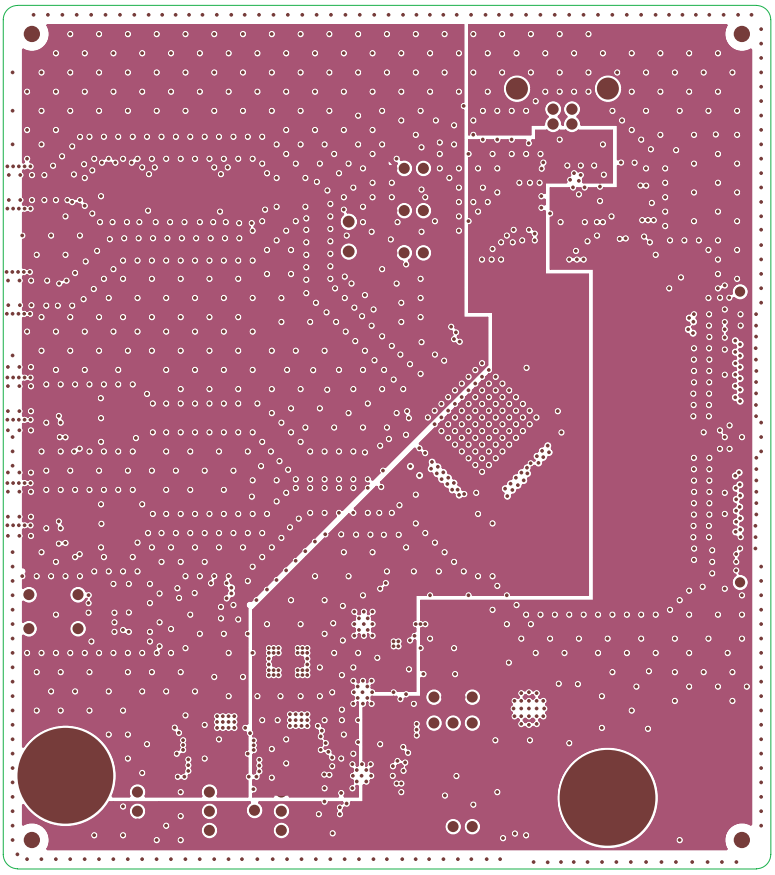

Figure 19. Power Plane 2

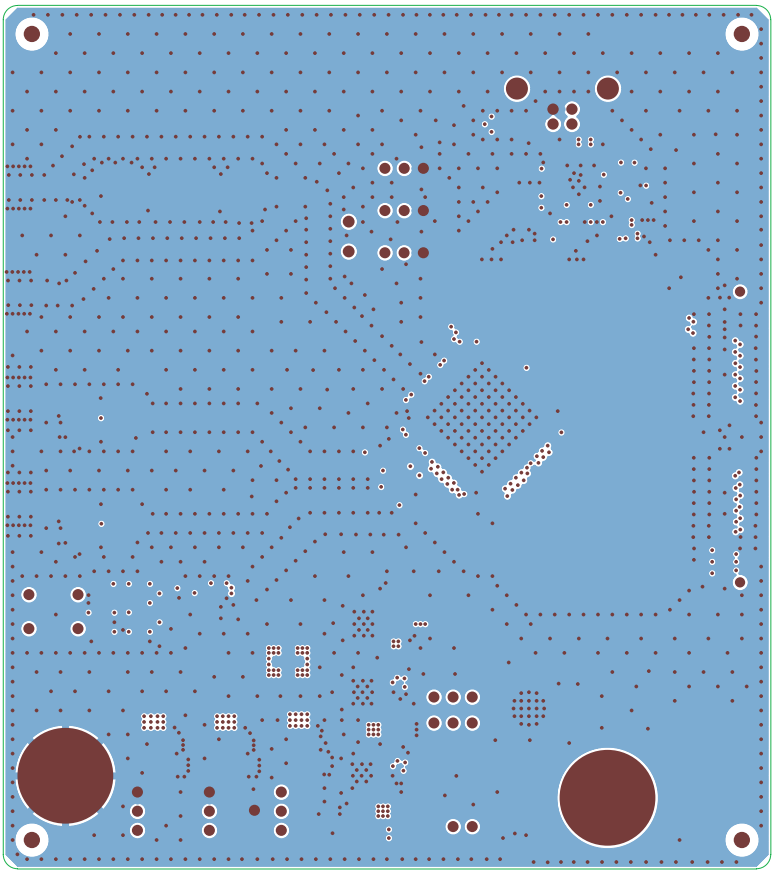

Figure 20. Ground Plane 2

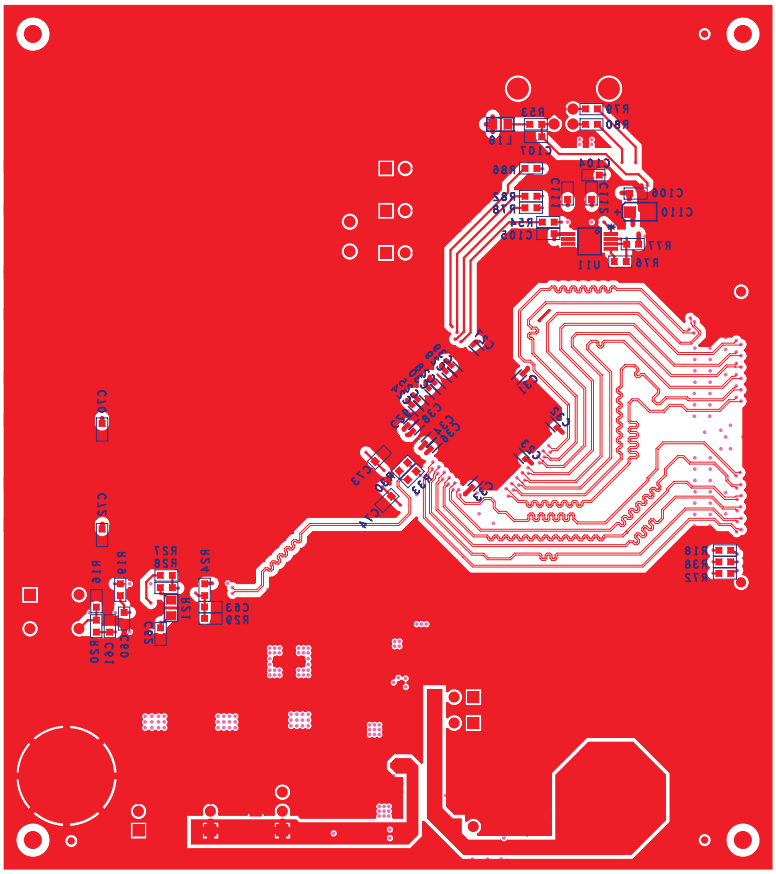

Figure 21. Bottom Side

5.3 Bill of Materials

Item	Qty.	Designator	Value	Description	Package/Case	Manufacturer	Manufacturer P/N
1	1	C3	0.1uF	16V 10% X7R	0402	Murata	GRM155R71C104KA88D
2	19	C23,C24,C25,C26,C27,C28,C29, C30,C31,C32,C33,C34,C36,C38, C39,C43,C120, C121,C122	0.01uF	25V 10% X7R	0402	Panasonic	ECJ-0EB1E103K
3	1	C40	0.1uF	10V 10% X5R	0402	Panasonic	ECJ-0EB1A104K
4	3	C45,C51,C58	33uF	TANTALUM, SOLID, POLARIZED, 10 V, 1411	1411	Panasonic	ECS-T1AX336R
5	3	C46,C52,C57	10uF	10V 10% X5R	0805	Panasonic	ECJ-2FB1A106K
6	12	C47,C53,C59,C61,C62,C65,C69, C70,C73,C74,C102,C103	0.1uF	16V 10% X7R	0603	Panasonic	ECJ-1VB1C104K
7	3	C60,C63,C107	0.01uF	100V X7R	0603	Kemet	C0603C103K1RACTU
8	1	C67	47uF	20V 20% TANT	2917	AVX	TPSE476M020R0150
9	1	C104	33nF	50V 10% X7R	0603	AVX	06035C333KAT2A
10	4	C105,C106,C111,C112	10nF	50V 10% X7R	0603	Murata	GCM188R71H103KA3
11	2	C108,C109	27pF	100V 5% NP0	0603	Murata	GRM1885C2A270JA01D
12	1	C110	10uF	10V 20%, TANT	1206	Kemet	T491A106M010AT
13	2	C128,C129	1uF	10V 20% X5R	0402	Panasonic	ECJ-0EB1A105M
14	4	C184,C185,C186,C187	1uF	25V 20% X5S	0603	Panasonic	ECJ-1V41E105M
15	1	C188	4.7uF	50V Y5V	1206	Murata	GRM31CF51H475ZA01L
16	1	C189	470pF	50V 20% X7R	0603	Murata	GRM188R71H471MA01D
17	2	C234,C235	2.2uF	10V 10% X5R	1206	Panasonic	ECJ-HVB1A225K
18	1	C414	15pF	50V 5% NP0	0402	Panasonic	ECJ-0EC1H150J
19	1	D1	1N4148	DIODE SWITCH 75V 300MA SOD323	DIODE_SM_SOD_323	Micro Commercial Co.	1N4148WX-TP
20	1	D2	B340A-13-F	DIODE SCHOTTKY 3A 40V SMA	DIODE_SM_DO_214AC	Diodes Inc	B340A-13-F
21	1	D16		LED GREEN S-J TYPE 0805	LED_0805	Panasonic	LNJ306G5UUX
22	4	JP4,JP5,JP6,JP16		CONN HEADER 1x3, 0.25 GLD	HDR_THVT_1x3_100_M	SAMTEC	HMTSW-103-07-G-S-240
23	4	JP12,JP13,JP14,JP15		CONN HEADER 1x3, 0.25 GLD	HDR_THVT_1x3_100_M	SAMTEC	HMTSW-103-07-G-S-240
24	1	JP17		CONN HEADER 1x2, 0.100" T/H GOLD	HDR_THVT_1x2_100_M	SAMTEC	HMTSW-102-07-G-S-240
25	2	J1,J12		CONN SMA JACK END LAUNCH PCB	SMA_SMEL_250x215	Emerson Network	142-0711-821
26	1	J4		CONN HEADER 120POS .020" SMT GLD	CONN_QTH_30X2-D-A	SAMTEC	QTH-060-02-F-D-A
27	1	J5		Banana jack red	JACK_THVT_BANANA_500DIA	Allied Electronics	ST-351A
28	1	J6		Banana jack black	JACK_THVT_BANANA_500DIA	Allied Electronics	ST-351B
29	1	J17		CONN RECEPT USB TYPE B PCB	CONN_USB_TYPB_FEM	Milmax	897-43-004-90-000
30	1	J18		CONN HEADER 1POS .100" T/H GOLD	HDR_THVT_1x1_SPECIAL	SAMTEC	HMTSW-101-07-G-S-240
31	3	L6,L9,L11		BEAD CORE 68 OHM 3A 1206 SMD	1206	Panasonic	EXC-ML32A680U
32	1	L16	68uH	SMT power inductors	IND_SM_MSS1038	Coilcraft	MSS1038-683ML
33	1	L18	1K @ 100MHZ	FERRITE CHIP 1000 OHM 200MA 0805	0805	Murata	BLM21AG102SN1D
34	6	R25,L25,R26,L26,R51,R52	0 Ω	1/16W 0402 SMD	0402	Yageo	RC0402JR-070RL
35	3	R16,R65,R77	10 kΩ	1/10W 1% 0603 SMD	0603	Panasonic	ERJ-3EKF1002V
36	2	R19,R20	100 kΩ	1/10W .1% 0603 SMD	0603	Panasonic	ERA-3AEB104V
37	1	R21	1 MΩ	1/8W 1% 0805 SMD	0603	Panasonic	ERJ-6ENF1004V
38	2	R24,R29	5.5 kΩ	1/10W 1% 0603 SMD	0603	Panasonic	ERJ-3EKF5491V

Item	Qty.	Designator	Value	Description	Package/Case	Manufacturer	Manufacturer P/N
39	8	R28,R30,R33,R54,R67,R78,R82, R86	0 Ω	1/10W 0603 SMD	0603	Panasonic	ERJ-3GEY0R00V
40	1	R62	30.1 kΩ	1/10W 1% 0603 SMD	0603	Panasonic	ERJ-3EKF3012V
41	1	R63	93.1 kΩ	1/10W 1% 0603 SMD	0603	Panasonic	ERJ-3EKF9312V
42	1	R64	2.2 Ω	1/10W 1% 0603	0603	Panasonic	ERJ-3RQF2R2V
43	1	R66	3 kΩ	1/10W 1% 0603 SMD	0603	Yageo	RC0603FR-073KL
44	1	R68	100 Ω	1/10W 1% 0603 SMD	0603	Panasonic	ERJ-3EKF1000V
45	1	R74	4.7 kΩ	1/10W 1% 0603 SMD	0603	Panasonic	ERJ-3EKF4701V
46	1	R75	1.5 kΩ	1/10W 1% 0603 SMD	0603	Panasonic	ERJ-3EKF1501V
47	1	R76	2.21 kΩ	1/10W 1% 0603 SMD	0603	Panasonic	ERJ-3EKF2211V
48	2	R79,R80	26.7 Ω	1/10W 1% 0603 SMD	0603	Panasonic	ERJ-3EKF26R7V
49	1	R85	100 Ω	1/20W 1% 0201 SMD	0201	Yageo	RC0201FR-07100RL
50	1	R109	300 Ω	1/10W 1% 0603 SMD	0603	Panasonic	ERJ-3EKF3000V
51	1	SW1		SPST Switch	SW_THVT_SPST_4_B3F	Omron	B3F-1002
52	2	TP1,TP5		TEST POINT PC MINI .040"D WHITE	TP_THVT_060_RND	Keystone	5002
53	1	T3		SMT RF transformer	TFMR_6_RF_DUAL_FOOTPRINT	Minicircuits	JTX-4-10T
54	2	T4,T5	ETC1-1-13	E-Series RF 1:1 Transmission Line Transformer 4.5 - 3000 MHz	TFMR_6_RF_DUAL_FOOTPRINT	MA COM	ETC1-1-13
55	1	U4	CD4013BM	IC DUAL D-TYPE FLIP-FLOP 14-SOIC	SOIC_14_344x157_50	Texas Instruments	CD4013BM
56	2	U5,U14	TPS79633DCQ	IC REG LDO 3.3V 1A SOT223-6	SOT_223_6_TG	Texas Instruments	TPS79633DCQ
57	1	U6	SN65LVDS100DGK	IC DIFF TRANSLATOR/REPEATR 8TSSOP	HTSSOP_8_122x122_26	Texas Instruments	SN65LVDS100DGK
58	1	U7	TPS5420D	IC REG BUCK ADJ 2A 8SOIC	SOIC_8_197x157_50	Texas Instruments	TPS5420D
59	1	U8	TPS79501DCQ	IC REG LDO ADJ .5A SOT223-6	SOT_223_6_TG	Texas Instruments	TPS79501DCQ
60	1	U9	ADS5400HFS/EM	IC ADC 12BIT 1000MSPS 100HTQFP	HFS(S-CQFP-F100)	Texas Instruments	ADS5400HFS/EM
61	1	U10	FT245BM	USB FIFO device	PQFP32	Future Technology	FT245BL
62	1	U11	93C66B	IC EEPROM 4KBIT 2MHZ 8TSSOP	TSSOP_8_177x122_26	Microchip	93C66B-I/ST
63	1	Y1	6.0000MHz	CRYSTAL 6.000MHZ 32PF SMD	smd_csm-7_xtal	ECS	ECS-60-32-5PXDN-TR
64	8			Header shunt, 100 MIL, BLACK	0.1	3M	929950-00
65	4			Screw for standoff, 4-40 x 3/8, SS, panhead		Building Fasteners	PMSSS 440 0038 PH
66	4			Aluminum standoff, hex, 4-40 x 0.5		Keystone	2203
67	1		HREL013	PCB		Any	HREL013
68	0	C66,C71,C72	0.1uF	16V 10% X7R	0603	Panasonic	ECJ-1VB1C104K
69	0	C126	6.8pF	50V NP0	0402	Murata	GJM1555C1H6R8CB01D
70	0	J2,J13		CONN SMA JACK END LAUNCH PCB	SMA_SMEL_250x215	Emerson Network	142-0711-821
71	0	L7		BEAD CORE 68 OHM 3A SMD	1206	Panasonic	EXC-ML32A680U
72	0	R8	10 kΩ	1/10W 1% 0603 SMD	0603	Panasonic	ERJ-3EKF1002V
73	0	R18,R27,R38,R53,R72	0 Ω	1/10W 0603 SMD	0603	Panasonic	ERJ-3GEY0R00V
74	0	R22,R23,R34,R37,R83	49.9 Ω	1/10W 1% 0603 SMD	0603	Panasonic	ERJ-3EKF49R9V
75	0	R31,R32,R35,R36	100 Ω	1/10W 1% 0603 SMD	0603	Panasonic	ERJ-3EKF1000V
76	0	R39,R40,R55,R56	0 Ω	1/16W 0402 SMD	0402	Yageo	RC0402JR-070RL
77	0	T7		SMT RF transformer	TFMR_6_RF_DUAL_FOOTPRINT	Minicircuits	JTX-4-10T

EVALUATION BOARD/KIT/MODULE (EVM) ADDITIONAL TERMS

Texas Instruments (TI) provides the enclosed Evaluation Board/Kit/Module (EVM) under the following conditions:

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING LIMITED WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please visit www.ti.com/esh or contact TI.

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REGULATORY COMPLIANCE INFORMATION

As noted in the EVM User's Guide and/or EVM itself, this EVM and/or accompanying hardware may or may not be subject to the Federal Communications Commission (FCC) and Industry Canada (IC) rules.

For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

【Important Notice for Users of EVMs for RF Products in Japan】

This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

Texas Instruments Japan Limited
(address) 24-1, Nishi-Shinjuku 6 chome, Shinjuku-ku, Tokyo, Japan

http://www.tij.co.jp

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3. 技術基準適合証明を取得後ご使用いただく。

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日本テキサス・インスツルメンツ株式会社
東京都新宿区西新宿６丁目２４番１号
西新宿三井ビル
http://www.tij.co.jp

EVALUATION BOARD/KIT/MODULE (EVM)
WARNINGS, RESTRICTIONS AND DISCLAIMERS

For Feasibility Evaluation Only, in Laboratory/Development Environments. Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. Since the EVM is not a completed product, it may not meet all applicable regulatory and safety compliance standards (such as UL, CSA, VDE, CE, RoHS and WEEE) which may normally be associated with similar items. You assume full responsibility to determine and/or assure compliance with any such standards and related certifications as may be applicable. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
4. You will take care of proper disposal and recycling of the EVM’s electronic components and packing materials.

Certain Instructions. It is important to operate this EVM within TI’s recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

Agreement to Defend, Indemnify and Hold Harmless. You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

Safety-Critical or Life-Critical Applications. If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

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