

Setting a new standard for MCU performance while minimizing energy consumption



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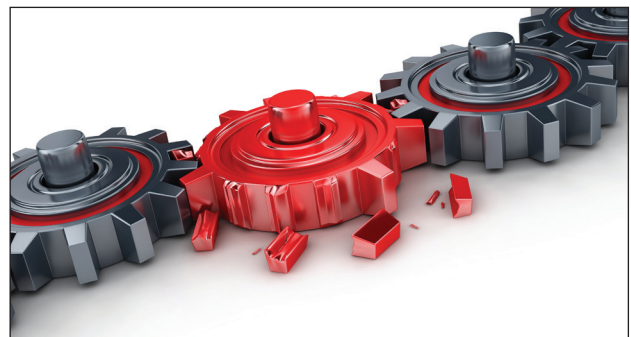
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As products today and in the future become increasingly more intelligent, we see the need to process an ever growing amount of data. In order to gather this data, sensor networks are deployed to record events in a multitude of locations, gathering many different data types from different sources for a number of use cases.

By detecting events such as a door or window opening, home security sensors make residents feel safe. Data from sensors on an industrial pump helps factory owners detect early warning signs to prevent failures and reduce maintenance costs over time. Data from distributed mesh-based sensor networks is even used to process geological events, giving emergency responders more time to act. In most cases, the data recorded in systems like these must be sent to a centralized node for processing, analysis and decision making. This constant data stream can be costly in terms of both power and time. By adding local intelligence to turn individual sensors into smart sensor nodes, more advanced localized processing or edge processing can be used to improve overall system response time and efficiency.

Inferential computations made at the edge of a system can also be communicated to a central node. This reduces the number of necessary wireless transmissions and enables real-time decisions when critical system events occur. As an example, if a gear within a drive system becomes worn and breaks a tooth, the frequency signature of the system will change. By detecting and analyzing these changes, the system can determine whether or not to shut down the motor until it can be examined and, if needed, repaired by a technician. Today, this intelligence is typically implemented as either a low-end digital signal processor (DSP) or a high performance microcontroller (MCU). Each option presents a set of pros and cons and frequently, even a low-end DSP can be overkill for the required performance of a sensor node. Many low-end DSPs need an external analog-to-digital converter (ADC) or external memory to gather and store data. These extra components quickly add undesired overhead to the total application cost and power consumption. As previously mentioned, home security systems serve as a good example given the number



of windows and doors on many buildings. While it would be beneficial, many consumers will be reluctant to pay for multiple, expensive glass-break detection systems. These DSP-based systems utilize fast Fourier transforms (FFT's) for audio vibration data analysis to determine if a window has been broken. Additionally, they are relatively power hungry, so unless every sensor has a permanently wired electricity supply, regular battery changes would be required.

On the microcontroller side, edge processing is often a challenge due to their minimal computational performance capabilities. For example, running a FFT that is implemented in C-code can take much longer

than utilizing a DSP that has dedicated hardware peripherals. This time delta can not only create inefficiencies as the MCU runs in active modes for longer periods of time, but, even more critically, may also lead to delayed results in time sensitive situations. Inherently, this time gap is reducing the viability of the Internet of Things (IoT) because the concept is predicated on two ideas:

1. Central hubs can communicate with and process data from billions of connected devices
2. Connected devices are smart enough to enable a simple end-user experience

Here is another example to consider. Personal assistant wireless speakers and mobile handset devices are able to process a user's natural language to select songs or order pizza. This presents an incredibly complex challenge since people speak in a variety of accents, tones and dialects. Digital signal processing at the end nodes could certainly be used to interpret the enormous number of potential phrases from a user, but this would require a costly and likely physically large solution that could affect the device's portability. Battery life is also a key consideration as charging more than once each day might cause consumers to lose interest. Today, this issue is addressed by enabling portable devices to simply listen for a code word or phrase that triggers the system to start streaming data to a central server for advanced analysis and routing back to the connected device. This is a commonly used technique for these types of advanced processing applications, but power inefficiencies lead us to consider what charging interval a user would find acceptable?

Depending on the application, daily charging may be tolerable, but consumers would obviously prefer solutions that could run for a week or more on a single charge. Let's again consider the glass-break detectors and motor monitors. Even a week between battery changes would not be a practical solution across thousands of motors in a large factory. Ultimately, combining the low-power benefits of

an MCU with the enhanced performance of a DSP delivers significant advances for the intelligence and data processing capabilities of inferential edge computing. This is where more advanced hardware is required.

A new solution to an old problem

Imagine if MCUs could take on some of the pre-processing capabilities of digital signal processing engines with dedicated hardware accelerators. These MCUs could wake up quickly to filter data or perform an FFT, but could also leverage comparators and ADCs in standby mode to understand when to wake up. This could enable real-time results in various applications for both the industrial and consumer spaces, but could also reduce power consumption of systems to enable a battery life of years, not days.

Although some MCUs today do enable a selection of DSP accelerators, their tendency to push the central processing unit (CPU) to its limit causes them to consume a considerable amount of energy. New enabling DSP co-processors in MCUs, such as the low-energy accelerator (LEA) introduced on the [MSP430™ MCU platform](#), address the gap between MCUs and low-end DSPs by adding performance capabilities in a power conscious and cost effective way. An MCU featuring the LEA module can perform DSP functions in dedicated hardware, allowing it to go into lower-power modes, thus reducing overall system power while performing more complex inferential calculations. This would allow the application to either:

- A. Spend more time in low-power modes, effectively lowering the total application power.
- B. Focus on computation, increasing the application's frequency.
- C. Allow the application to perform other functions such as communicating with the master node wirelessly for IoT applications.

Over time, all of these options will be critical for enabling a broader proliferation of connected

devices, especially as smarter MCUs enable connected devices to quickly and conveniently provide data for users at low cost and high energy efficiency.

The LEA module is a vector math engine hosted within various MSP430 devices. This module can perform signal processing, matrix multiplications and other operations that normally take large amounts of time and energy to calculate during application runtime. Operating without any CPU interventions, the LEA module is a low-power coprocessor that performs operations and triggers an interruption when the function is completed. The LEA module operates based on the commands that are provided during configuration, by which the commands serve as pointers to memory input or output buffers and the type of operation. These commands are made easy to use through the [MSP DSP Library](#), which is specifically built and optimized for MSP430 MCU's to enable DSP applications of the programmers choosing. When the LEA module is available on a device, the compiler will automatically use it to optimize performance beyond the MSP C-code optimization techniques that have already been implemented.

Applications that utilize digital signal processing have a variety of different techniques that are required to enable an end-to-end solution. However, the process can be broken down into three main steps:

- 1) A way to acquire data. This can be an ADC interfacing with a sensor or a communication module such as SPI, I2C or UART.
- 2) After acquiring the data, you then perform signal processing techniques to extract desired information from the dataset. This can be a finite impulse response (FIR) filter to clean a signal, an FFT to extract various frequency artifacts or any other popular DSP-type process.
- 3) Once information has been extracted from the dataset, you then want to act on it. This can take the form of making a decision based on a result from an FFT or FIR or simply exporting the information you have calculated via a wired or wireless connection like Wi-Fi®, Sub-1 GHz networks, UART, I2C, SPI, etc.

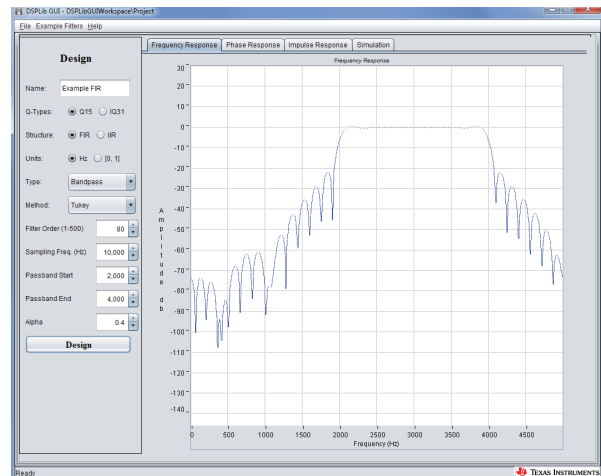


Figure 1. DSPLib GUI

In the past, step two has been implemented in embedded C-code that is often very intensive for the CPU and can dominate a majority of the applications computation period due to the math involved (such as a demanding FIR computation).

Optimized for both power and vector-based computational performance, the LEA module hardware accelerator crunches CPU taxing functions in a fast and efficient manner, greatly enhancing the overall system performance.

A practical implementation of this performance improvement can be seen in the TI Design reference design: [Filtering and Signal Processing with Low Energy Accelerator \(LEA\) on MSP FRAM Microcontroller](#).

Figure 2 below, shows that the FFT function takes 9.64ms when the processing is carried out by the main CPU.

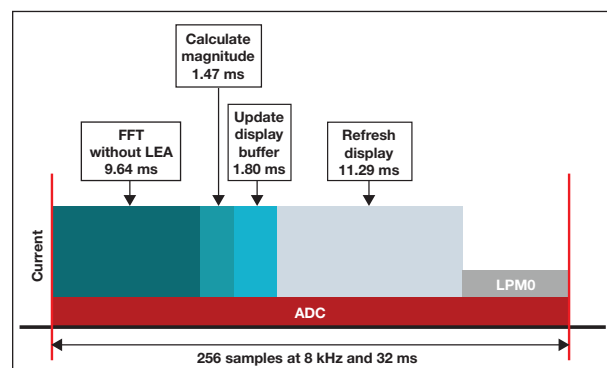


Figure 2. FFT based application without the LEA module

Figure 3 depicts the significant benefit that the LEA module brings, reducing the FFT processing time reduced to 700us.

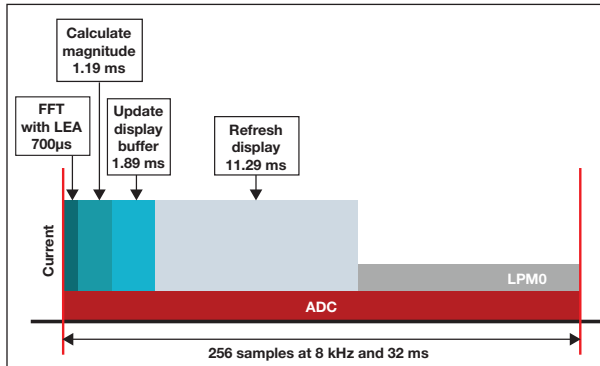


Figure 3. FFT based application utilizing the LEA module

In testing and application, we have seen up to more than 15 times greater performance in comparison to traditional C-based 16-bit MCU implementations of various signal processing functions. We have even experienced up to 40 times greater performance than ARM® Cortex®-M0+ devices using the CMSIS DSP Library.

Not only does the LEA module perform these intensive signal processing operations faster than optimized C-code, but with the combination of the lower power capabilities of hardware accelerators and the fact that the LEA module enables you to operate in low-power mode 0 (LPM0) on our MSP430 MCUs energy consumption improvements of up to nine times compared to similar MSP430 MCU's running C-code and an improvement of up to 12 times when compared with ARM Cortex-M0+ MCUs using the CMSIS DSP Library.

	Clock Frequency	Energy (µJ)			
		128-Point Complex FFT	256-Point Complex FFT	512-Point Complex FFT	FIR
MSP430FR5994 with LEA	8 MHz	1.228	2.219	4.424	4.378
MSP430FR5994 with LEA	16 MHz	1.182	2.092	4.184	4.065
ARM Cortex-M0+ MCU	12MHz with DC/DC	10.722	24.777	52.806	32.295
Performance improvement of MSP		9.07x	11.84x	12.6x	7.94x

Table 1. Performance comparison

The performance advantage of the LEA module varies based on the type of signal processing technique you are implementing. For instance, the performance of an FFT operation can vary based on a few components such as vector length and whether you are computing a complex FFT or real FFT.

When implementing a FIR filter, the performance depends on a number of variables, including vector length, order and whether or not you are doing a complex or real FIR calculation. However, it is important to note that on all available vector math operations in the LEA module you will see an overall improvement to traditional C-code signal processing techniques.

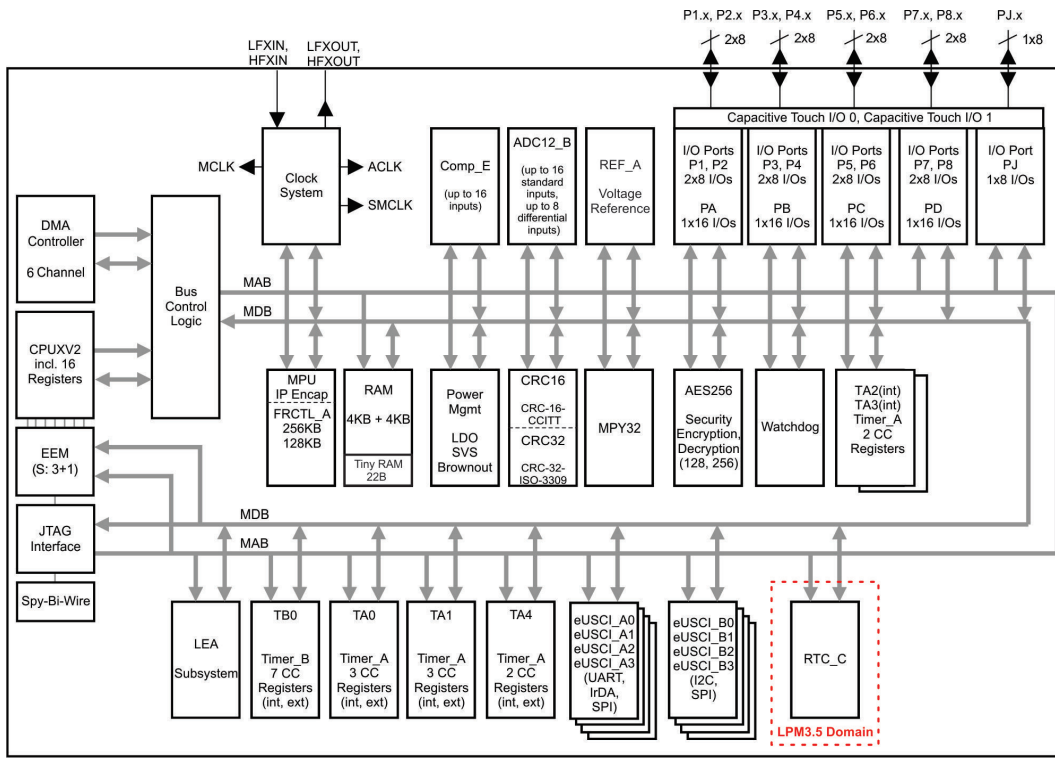
For more information on the performance benefits and benchmarking of the low-energy accelerator, please reference this application note: [Benchmarking the Signal Processing Capabilities of the Low-Energy Accelerator.](#)

MSP430FR5994 MCUs with LEA

The MSP430F599x microcontrollers are the first devices to feature this new the LEA module peripheral. These high performance 16-bit MCU's combine an award winning ultra-low-power architecture with up to 256KB of embedded ferroelectric random access memory (FRAM) and an array of efficient yet flexible peripherals to form an excellent MCU platform for many digital signal processing applications.

The 256KB of embedded ultra-low power FRAM provides the user customizable partition program and data memory, enabling the creation of large non-volatile data buffers.

Get started with development today by using the [MSP430FR5994 MCU LaunchPad™ development kit](#) (pictured in **Figure 5**). This kit includes all the necessary hardware to start evaluating and developing with this powerful MCU.



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Figure 4. MSP430FR5994 MCU block diagram

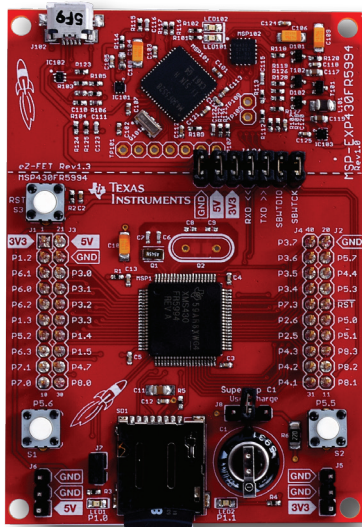


Figure 5. MSP-EXP430FR5994 MCU LaunchPad™ development kit

Summary

Overall, there are a multitude of available applications that leverage either an MCU or a low-end DSP. Vocoders, presence detection, echo/noise cancelation, blood glucose monitors and structural or environmental monitor networks can all be broken down to a variety of different signal processing functions that interpret a situation through sorting and data analysis, detecting and, if necessary, acting on an event or pending situation. In each case, TI's low-energy accelerator (LEA) can provide benefits by enabling faster and more efficient data analysis to expand battery lifetime, raise performance or increase functionality!

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