Single Event Effects Testing for the ADC12DJ3200QML-SP 12-bit, Dual 3.2-GSPS or Single 6.4-GSPS, RF-Sampling, JESD204B, Analog-to-Digital Converter (ADC)

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***Abstract*—The effects of heavy-ion irradiation on the single-event effect performance of the Texas Instruments ADC12DJ3200QML-SP and its JESD204B serialized interface were characterized using the K500 Cyclotron facility at Texas A&M University. The results demonstrate latch-up immunity up to LET_{EFF} = 120 MeV-cm^2/mg at T_J = 125°C while operating at the maximum recommended operating supply voltages. Dynamic cross sections for the code error rate of the device and the serialized interface are also presented.**

***Index Terms*—analog-to-digital converter, heavy ion testing, JESD204B, RF-sampling, serialized interface, single event effects**

I. Introduction

THE TEXAS INSTRUMENTS ADC12DJ3200QML-SP is the first JESD204B-compliant, RF-sampling, 12-bit analog-to-digital data converter (ADC) for aerospace and high-reliability applications. In dual channel mode the ADC can sample up to 3200-MSPS, while in single channel mode the ADC interleaves both internal cores to achieve sampling rates up to 6400-MSPS. The ADC12DJ3200QML-SP can directly sample input frequencies from DC to above 10 GHz. See Fig. 1 for the block diagram.

The ADC12DJ3200QML-SP uses a high speed JESD204B output interface with up to 16 serialized lanes and subclass-1 compliance for deterministic latency and multi-device synchronization. The serial output lanes support bit rates up to 12.8 Gbps and can be configured to trade-off bit rate versus number of lanes. The JESD204B interface enables a reduction in board space and layout complexity compared to traditional LVDS data converters, while also enabling higher channel density and more cost-effective hardware (Fig. 2).

The ADC12DJ3200QML-SP is built using the Texas Instruments C021.A 65 nm CMOS process technology and utilizes a time interleaved architecture that allows for low power consumption (1.5 W per channel), high data conversion rates (up to 6400-MSPS), and high full-power (-3 dB) input bandwidth (7 GHz).

The ADC12DJ3200QML-SP provides foreground and background calibration options for gain, offset and static linearity errors. Foreground calibration is run at system startup or at specified times during which the ADC is offline and not sending data to the logic device. Background calibration allows the ADC to run continually while the cores are calibrated in the background so that the system does not experience downtime. The calibration routine is also used to match the gain and offset between sub-ADC cores to minimize spurious artifacts from time interleaving.

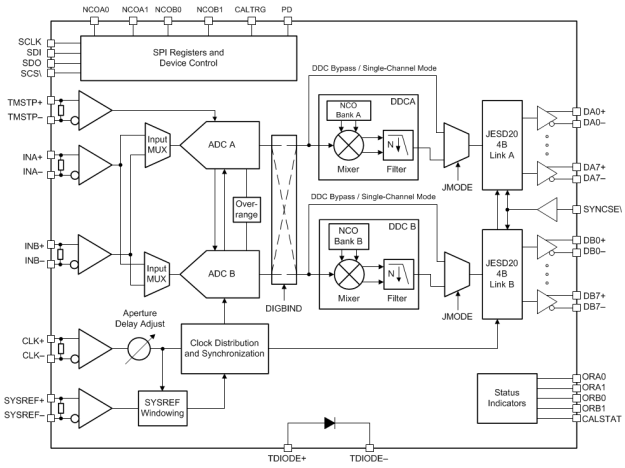

Fig. 1. Block diagram of the ADC12DJ3200QML-SP. The two JESD204B links enable up to 16 output lanes. The ADC cores can be interleaved to achieve 2x the sampling rate in single channel mode.

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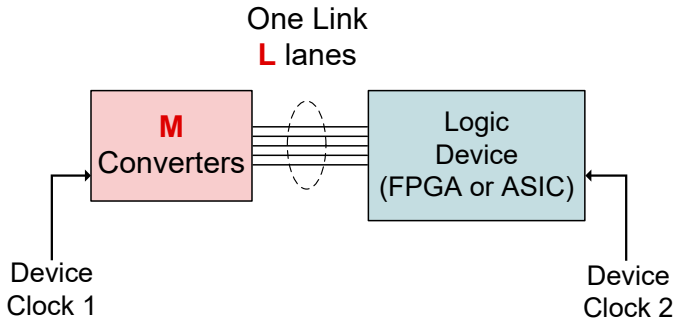

Fig. 2. Simplified block diagram of the JESD204B link. The JESD204B interface enables reduced lane counts between the converter and FPGA compared to traditional LVDS devices. There are no data clocks or strict trace length-matching requirements.

II. Mechanisms of Single Event Effects

The primary concerns for the ADC12DJ3200QML-SP are its resilience against the destructive single-event effects (SEE) such as single-event latch-up (SEL) and non-destructive single-event functional interrupts (SEFI).

The ADC12DJ3200QML-SP was characterized for SEL events as the 65 nm CMOS process used for the ADC12DJ3200QML-SP introduces a potential for SEL susceptibility [1][2]. The ADC12DJ3200QML-SP exhibited no SEL with heavy-ions of up to LET_{EFF} = 120 MeV-cm^2/mg at a fluence of 10^7 ions/cm^2 and a die temperature of 125°C while operated in the recommended supply voltage range.

Another concern in a high reliability, high performance application is the SEFI characteristics of the ADC, especially in the high-speed JESD204B serialized interface which has not been used in high-reliability, radiation environment applications previously. The ADC12DJ3200QML-SP SEFI performance was characterized beyond an LET_{EFF} = 120 MeV-cm^2/mg.

III. DUT Preparation & Test Setup

The flip-chip die of the ADC12DJ3200QML-SP must be de-capped and thinned for exposure to heavy ions. The de-capped unit exposes the Silicon substrate directly. The die were back-grinded to <40um for proper ion penetration through the Silicon substrate and a custom open-top RF socket is utilized to mount the device on the evaluation module (EVM). This socket opening allows for large beam angles beyond 45° (Fig. 3).

The test setup block diagram is shown in Fig. 4. We used low phase noise (LPN) signal generators to produce the clock and ADC input signals, along with band-pass filters (BFPs) to achieve the best possible ADC dynamic performance. Four-wire Kelvin-sensing power supplies were used to account for IR drops in the power supply cables and EVM power planes.

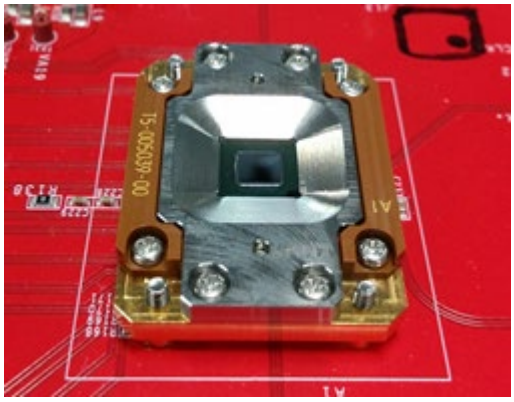

Fig. 3. ADC12DJ3200QML-SP mounted in the test socket on the DUT-EVM. The open top socket allows fast changing of devices and beam angles beyond 45°.

The test conditions for SEL testing and SEFI testing are outlined as follows:

1. For SEL testing, the ADC was operated at T_J = 125°C and datasheet maximum recommended voltage supplies (V_{MAX}).
    a. VA19 = 2.0V, VA11 = 1.15V, VD11 = 1.15V
2. For SEFI testing, the ADC was operated under the following conditions:
    a. Mission-mode "JMODE1" utilizing 16-lanes at 6.4 Gbps (JESD204B)
        i. JMODE1 is a single channel mode
    b. F_S = 6.4 GSPS (F_{CLK} = 3.2GHz)
    c. F_{IN} = 2.488GHz at -1 dBFS applied to Input Channel A
    d. Datasheet minimum recommended voltage supplies (V_{MIN})
        i. VA19 = 1.8 V; VA11 = VD11 = 1.05 V
    e. Ambient room temperature (roughly 25C)
    f. T_J = 80C when running foreground calibration (FG)
    g. T_J = 90C when running background calibration (BG)
    h. SYSREF calibration and processing enabled
    i. JTIMER watchdog feature set to 10

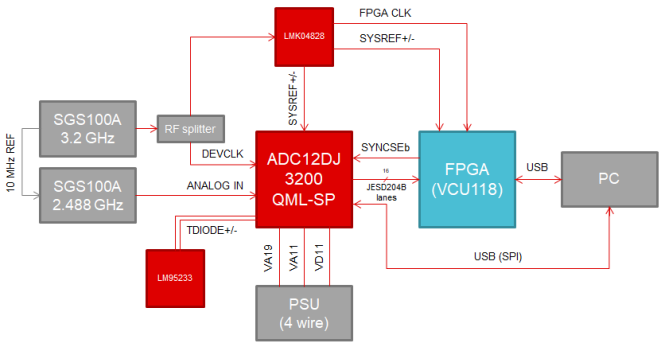

Fig. 4. Block diagram of the SEL and SEFI test setup. The LM95233 and LMK04828 chips are on-board with the DUT. The VCU118 FPGA is mounted on a separate EVM and the DUT-EVM interfaces with the FPGA through an FMC+ connector.

IV. Irradiation Facility

The ADC12DJ3200QML-SP was put through heavy ion testing using the TAMU 15 MeV K500 Cyclotron (Fig. 5). The device was monitored for SEL, SEFI and single-event upset (SEU).

The effective LET (LET_{EFF}), depth and range was determined with the custom RADsim-IONS application developed at Texas Instruments and based on the latest SRIM2013 models [3]. The application accounts for energy loss through the 1-mil thick Aramica beam port window and the air gap between the DUT and the heavy-ion exit port. Table I summarizes the ions and beam angles used to achieve a wide range of LETs for the ADC12DJ3200QML-SP's SEE characterization.

All beam runs stop at a total fluence of 10^7 ions/cm^2 with a target flux of 10^5 ions/cm^2/s (unless otherwise noted). Cross section data points represent an average of multiple runs and/or DUTs at each LET. The average Si thickness of the entire die was used to compute the effective LET.

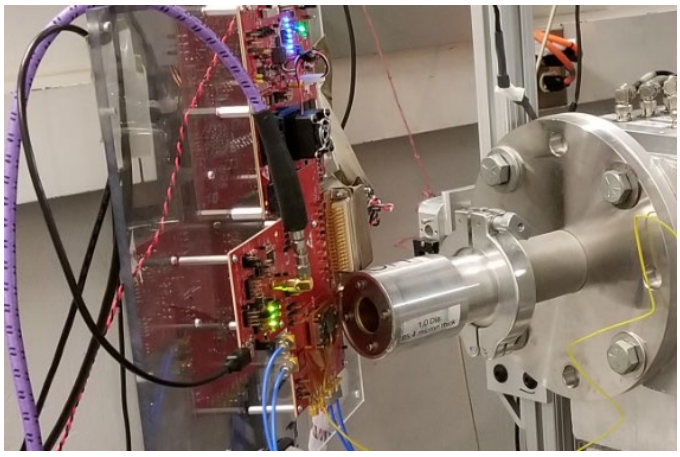

Fig. 5. DUT-EVM and capture card mounted for heavy-ion exposure in free-air. Hot air was used to increase the junction temperature of the DUT for SEL testing.

TABLE I
Ions, Angles, and Airgaps Used At TAMU for SEFI Testing

Ion	Angle	Air gap (mm)
Au	45	50
	30	50
	0	50
Ho	0	50
Xe	0	50
Kr	45	50
	0	50
Cu	30	50
	0	50
Ar	45	50
	0	50
N	0	50

V. Single-Event Latch-up Testing

The ADC12DJ3200QML-SP has three voltage supplies. These are VA19 (1.9V nominal analog supply), VA11 (1.1V nominal analog supply), and VD11 (1.1V nominal digital supply). The product specification allows for a supply voltage variance of +/-5% from the nominal values [4].

The supplied current to the DUT from the Kelvin-sensing power supply was constantly monitored through a LabView GUI. The junction temperature of the DUT was monitored using the on-die temperature diode through the on-board Texas Instruments LM95233 temperature sensor [5].

With the ADC in normal operating mode, no SEL was observed on any supply at T_J = 125°C with all supplies raised simultaneously up to +10% above the datasheet max operating spec. No SEL was observed up to an LET of 120 MeV-cm^2/mg at a flux of approximately 10^4 ions/cm^2/s to 10^5 ions/cm^2/s to a fluence of 10^7 ions/cm^2.

The robustness of the ADC to SEL was further characterized by placing the DUT into power-down mode and elevating the voltage supplies beyond their maximum recommended operating voltages. All supplies started out at the datasheet maximum recommended operating voltage or +5% of the nominal values, e.g. VA19 = 2.0V, VA11 = 1.15V, VD11 = 1.15V, and then were slowly ramped individually during separate beam runs until latch-up was observed.

Latch-up occurred on the VA11 supply at 1.55V, and on the VD11 supply at 1.60V, each greater than +30% above the specified maximum supply voltage. No damage was observed, however, low current compliance was used on the supplies for these SEL tests to prevent damage from occurring.

The latch-up holding voltage for VD11 was 1.155V and for VA11 was 1.30V.

As seen in Fig. 6, no SEL was observed on the VA19 supply despite raising it to 2.8V (+40% above the maximum rated voltage).

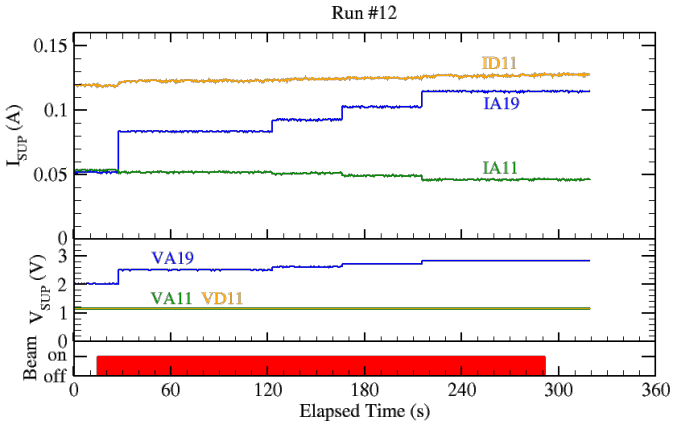

Fig. 6. Current and Voltage plots for attempted forced latch-up on the VA19 supply. The maximum operating supply voltage for VA19 is 2.0 V. No latch-up was observed; the current increase shown is due to leakage currents and DUT self-heating.

In later beam runs with the device in an active mission-mode and all supplies simultaneously raised to +15% above the specified maximum recommended operating voltage resulted in a higher-current latch-up of VA11 and a holding

voltage of 1.160V. The device was not damaged with the VA11 supply current compliance set to 1.0A.

VI. Single-Event Functional Interrupt Testing

A custom FPGA firmware image, including a fully compliant JESD204B receiver (RX), was developed to measure the code error rate (CER) of the ADC and to characterize the JESD204B transmitter (TX) of the ADC12DJ3200QML-SP in a radiation environment. The firmware image runs on a Xilinx VCU118 FPGA and is controlled by a custom LabView GUI.

In addition to CER testing, specific SEFI tests were performed to validate ADC functionality in a radiation environment. The ADC configuration registers were programmed and stored using a serial peripheral interface (SPI) GUI. The contents of the configuration registers were read before and after beam runs and compared. No changes to user-programmed or auto-loaded (default) registers were observed. Also, as shown in Fig. 7, Fast Fourier Transforms (FFTs) were captured and calculated during beam runs at the highest LET tested in order to confirm that the dynamic performance parameters of the DUT did not degrade while the beam was running.

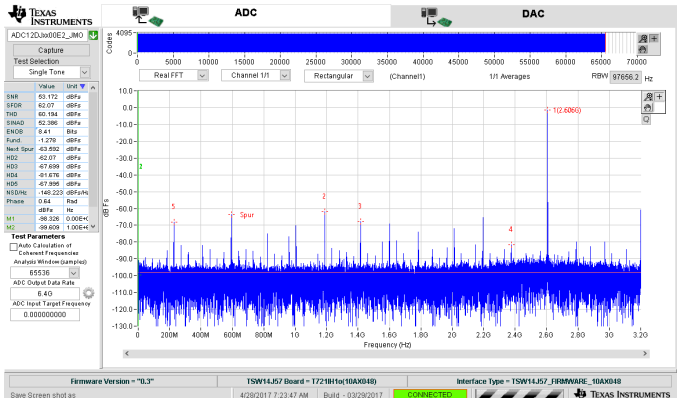

Fig. 7. Example FFT during SEFI testing showing a consistent ENOB > 8 for a 2.6 GHz full-scale input sample at 6.4 GSPS.

A. Code Error Rate Testing

If the sampling frequency and input signal frequency are coherent and the number of the continuous time signal cycles after N discrete time samples is a prime number, then sample numbers n and n + N are equal if there are no code errors. However, if there are code errors in the ADC's output codes, then the difference between these two samples is non-zero. Thus any non-zero value resulting from subtracting the corresponding samples n and n + N is flagged as a code error [6]. The magnitude of the error is compared with a threshold value to determine the severity of the error and then counted by a threshold-specific error counter.

Error thresholds are set at 10 user-defined levels. We used thresholds of 16, 24, 32, 64, 128, 256, 512, 1024, 2048, and 3072 LSBs.

Due to inherent thermal and environmental noise, we observe CER errors at up to the 128-LSB threshold without the beam running. We will consider CER errors above the 256-LSB threshold as an SEE event. JESD204B transmitter errors are also included in the CER measurements.

Fig. 8 and 9 show the 256-LSB CER cross-section plots for Foreground and Background calibration modes. We see roughly equivalent cross-section performance regardless of the calibration mode used. The Weibull fit parameters are shown in Table II.

It is important to note that the shape of the measured cross-section curve reflects the multiple CER contributors including analog upsets, digital upsets and JESD204B interface upsets, each with different probability distributions of CER magnitude.

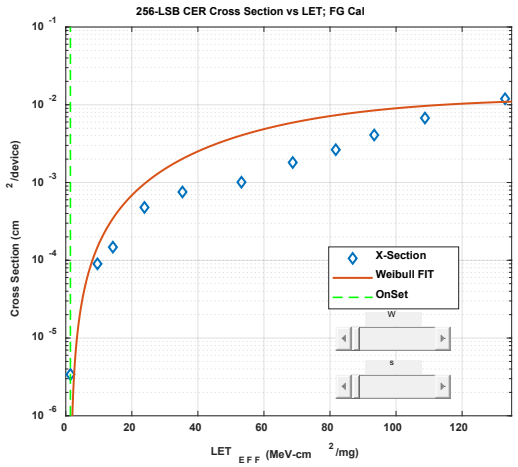

Fig. 8. 256-LSB CER cross section for the device running in Foreground calibration mode.

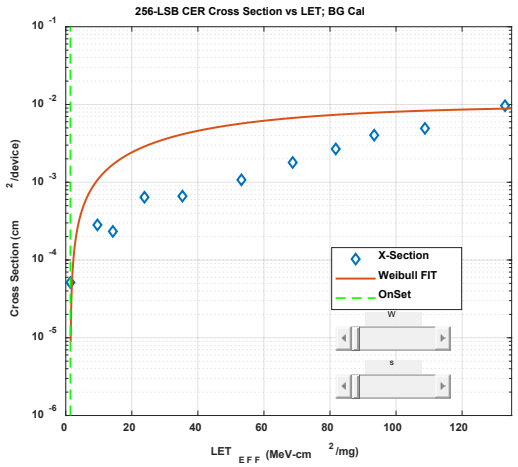

Fig. 9. 256-LSB CER cross section for the device running in Background calibration mode.

TABLE II
Weibull Parameters for the 256-LSB CER Cross Sections

Parameter	Foreground Calibration	Background Calibration
Onset (MeV-cm^2/mg)	1.4	1.4
σ_{SAT} (cm^2)	1.19E-2	9.64E-3
W	82.5	57.5
s	1.9	1.1

B. JESD204B Link Characterization

The custom FPGA firmware acts as a JESD204B compliant receiver (RX). If the RX detects an error in the transmission of data from the ADC or the ADC corrects an error in its transmission, then the link is automatically reestablished (Fig. 10). The RX will assert a signal called JESD204B "SYNC" when the link needs to be reestablished. The active-low SYNC signal is used to indicate if the RX has achieved code group synchronization (CGS) and is ready to decode data [7]. We recorded the number of times the link was reestablished in a given beam run along with the time it took to reestablish the link once an error was detected. Note that the JESD204B "SYSREF" signal will help both TX and RX recover after an upset [8]. A continuous SYSREF signal running at 16MHz is always present during our testing and is recommended in practice. The SYSREF signal was derived from the device clock by the Texas Instruments LMK04828 [9] and distributed to both the DUT and the FPGA.

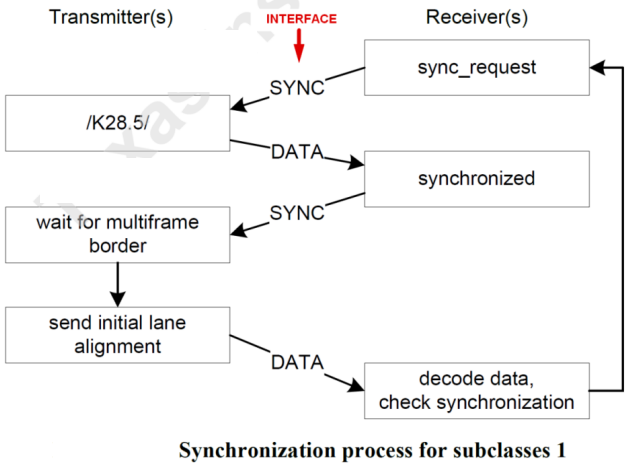

Fig. 10. The synchronization procedure to establish the JESD204B 8b/10b link. A fully compliant receiver plays a most critical role in reestablishing the link when it is upset.

Fig. 11 and 12 show the SYNC Assert cross-section plots for Foreground and Background calibration modes. We observe no difference in the behavior of the link between ADC calibration modes. The Weibull fit parameters are shown in Table III. The JESD204B link was observed to always recover automatically from an upset without user intervention in the tested operating mode (JMODE1).

The average recovery time, once an upset or error was detected that causes SYNC to be asserted, across all tested LETs was around 1.3 µs and is shown in Fig. 13.

The maximum recorded SYNC assert recovery time was 11 µs for LET_{EFF} = 53. This measurement was not recorded for LETs above 53 MeV-cm^2/mg as this feature was unavailable when we tested with heavier ions.

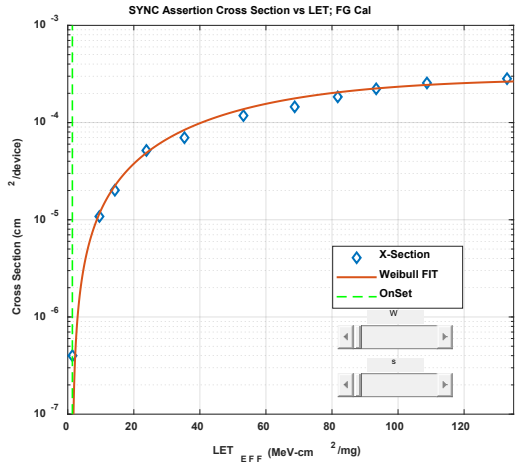

Fig. 11. SYNC Assert cross section for the device running in Foreground calibration mode.

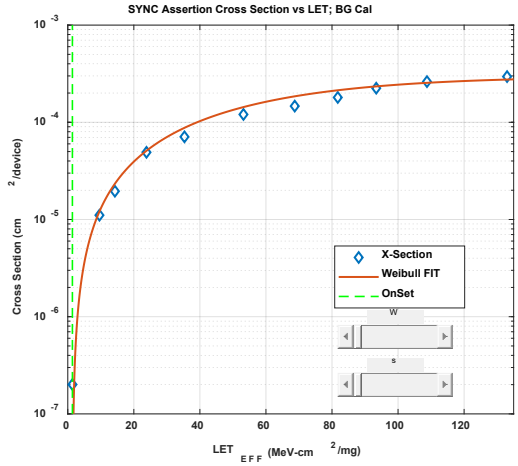

Fig. 12. SYNC Assert cross section for the device running in Background calibration mode.

TABLE III
WEIBULL PARAMETERS FOR THE JESD204B SYNC ASSERT CROSS SECTIONS

Parameter	Foreground Calibration	Background Calibration
Onset (MeV-cm^2/mg)	1.4	1.4
σ_{SAT} (cm^2)	2.83E-4	2.95E-4
W	68	68
s	1.5	1.5

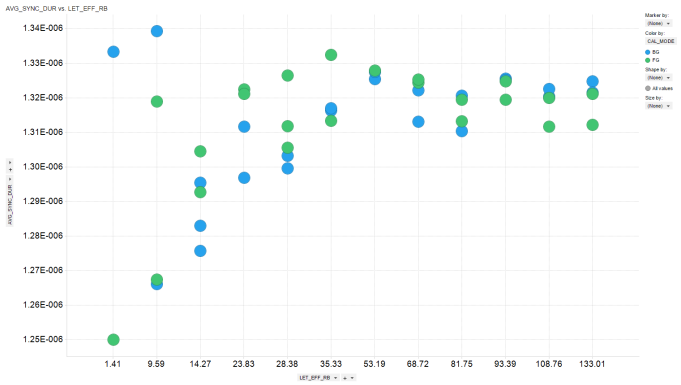

Fig. 13. Average JESD204B link recovery time after an upset is detected that causes SYNC to be asserted. There is no significant difference in the average recovery time across LETs or ADC calibration modes (blue = BG, green = FG).

VII. Total Ionizing Dose

The ADC12DJ3200QML-SP has a TID rating of 300 krad(Si) tested according to MIL-STD-883, Test Method 1019. The device shows no performance degradation at 300 krad(Si) across multiple wafer-lots. Pre- and post-performance measurements were taken on automated test equipment (ATE). All ATE measurements meet datasheet specifications after the TID testing. Fig. 14 shows the signal-to-noise ratio (SNR) of the ADC operating in dual-channel mode with all post-TID test results meeting the datasheet specification of 52 dBFS.

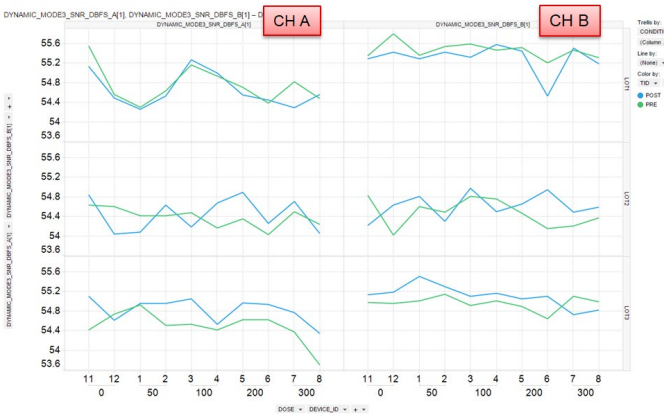

Fig. 14. SNR measurements for Pre- (green) and Post- (blue) irradiation taken across three different fab-lots. Six samples per dose (two per fab-lot) were tested. All ATE measurements meet datasheet specifications after the TID testing.

VIII. Summary

A summary of the ADC12DJ3200QML-SP SEE testing is as follows:

- The ADC's JESD204B link in the tested 16-lane JMODE1 always self-recovers from radiation events and without user intervention.
- The ADC in the tested 16-lane JMODE1 exhibits no unrecoverable functional interrupts (SEFI) or permanent performance degradations under the beam.
- No user-programmable or fuse-backed device configuration registers are upset under the beam.
- Calibration vectors are not corrupted under the beam while running in either calibration mode.
- No SEL occurs up to an LET of 120 MeV-cm^2/mg using the datasheet recommended maximum supply voltages and T_J = 125°C.
- The total ionizing dose (TID) rating of the ADC12DJ3200QML-SP is 300 krad(Si).

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