WHITE PAPER

TEXAS INSTRUMENTS

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3D packaging advancements drive performance, power and density in power devices

Introduction

Since its emergence, the semiconductor industry has consistently followed a trajectory whereby it managed to do more with less. Continually shrinking process technologies made it possible for chip designers to integrate greater levels of innovation in the same or smaller device dies. Successively smaller sub-micron process geometries have had an inverse effect on the chip design domain: the physical size of chips has shrunk while the palette where chip designers work has expanded.

Now, the industry is challenged by the laws of physics. Stepping down the silicon process ladder does not automatically produce the same marginal performance enhancements that it once did. Of course, the appetite of the marketplace for increased chip performance is insatible. Upper-end computing and telecommunications systems demand power devices and other types of chips that are constantly pressing against the outer edges of high performance.

Many forces are pushing chip designers to search for and find innovation in all aspects of semiconductor technology, including device packaging. How a chip is packaged can make just as critical a contribution to a power device's performance characteristics as what is packaged inside. A chip's package should not be seen as the boundaries for its capabilities. Instead, the performance characteristics of a particular device must be extended and enhanced by its package technology if the device is to reach its fullest potential.

Innovative chip packaging technology is just as critical to the overall characteristics and performance parameters of power devices as the contents of particular die. This is certainly the case in many of the power devices that are implemented in high-performance computing and telecommunications systems where power efficiency, small footprint, high current levels, thermal management and reliability are of utmost importance.

For example, improving the power efficiency of the numerous DC/DC converters in the many switches, servers, gateways and other systems that make up the telecomm/Internet infrastructure would lower the power consumption of each system and thereby significantly reduce the operating expenses of the service providers that operate major portions of the infrastructure. There are many other such examples that point out the importance of a power device's performance characteristics. Device packaging, including the migration from 2D to 3D technology, plays a major role in achieving optimum performance.

TI's PowerStack™ packaging technology is a simple yet unique 3D packaging solution which improves the performance of power devices in a variety of applications and system types. This white paper will describe the benefits of PowerStack technology, results from the first implementation of it, and why more versions of this leading-edge packaging technology can be expected in the future.

A new dimension in innovation

In the past, designing a system's power subsystem might involve finding components with the right performance specifications and then arranging them in the most effective means possible. Given the requirements of today's high-performance computing and telecom systems, designing a power subsystem can be one of the most challenging aspects for a design team. Multiple and quite diverse voltage requirements, smaller form factors, the 'green' movement with its requirements for environmentally-friendly materials and reduced energy consumption, and other considerations are affecting the design and composition of power subsystems.

For example, the approach for designing switching DC/DC power converters has altered in response to the many changes in the system environment. For low-end, low-current applications mostly in the mobile market, a one-die solution or a dual-die converter featuring a single lateral MOSFET and a driver/controller device will most often suffice. When an additional MOSFET is needed, it would typically be placed alongside the first MOSFET and interconnected to the driver/controller. This side-by-side arrangement of two MOSFET devices (as seen in figure 1, which also includes a controller IC) consumes a significant portion of board real estate and impacts the converter's performance by introducing electrical parasitics as a result of the side-by-side connections among the two or three devices.

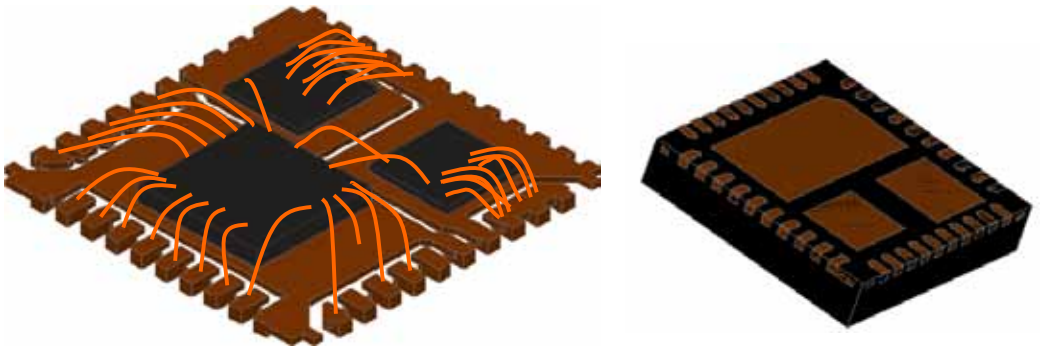

Figure 1: A side-by-side implementation of two MOSFETs with a controller IC

The benefits of a stacked, clipped MOSFET approach

To overcome the deficiencies of discrete implementations, TI has developed PowerStack packaging technology. Rather than restricted by two dimensions, PowerStack packaging solutions take advantage of all three dimensions by stacking MOSFETs in a single innovative device package. Similarly to other packaging technologies, the fundamental – but not the only – benefit of stacking is it takes advantage of 3D integration. Stacking reduces a device's 2D size and its required board space. PowerStack packaging certainly offers this space-saving benefit, but there are others in relation to the specific way the packaging is implemented.

The additional benefits of PowerStack packaging enhance electrical and thermal performance. As mentioned above, stacking naturally eliminates several electrical parasitics by placing the common terminals in immediate contact. Copper clip bonding, which is essential to PowerStack packaging, is a very practical implementation that is based on well established packaging capabilities and provides very low resistance on all of the current paths. In addition, TI's NexFET™ Power MOSFET technology are uniquely suited to stacking because the ground terminal can be in contact with the exposed pad of the package to effectively transfer heat to the printed circuit board. Moreover, PowerStack packaging capitalizes on widely accepted packaging processes and materials, making it extremely adaptable to greater levels of integration.

One example of PowerStack packaging is TI's NexFET™ Power Block Synchronous Buck MOSFETs which incorporates two MOSFETs in the footprint of one small outline no-lead package. Integrating a driver/controller into the same package creates a complete power stage solution in one small package.

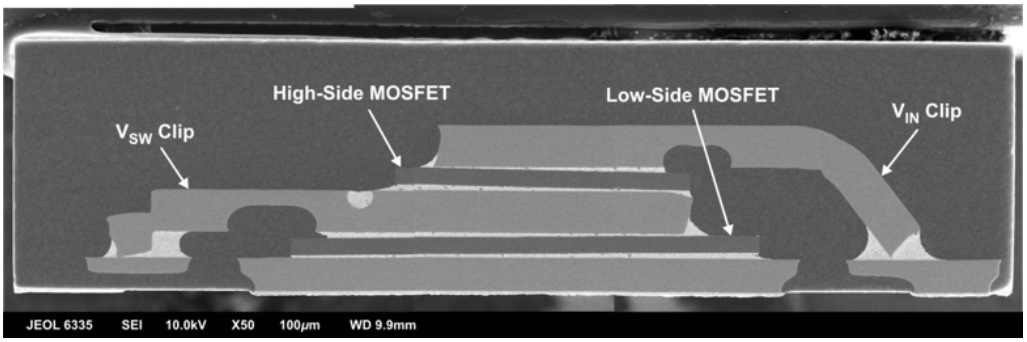

Figure 2: A cross-section of a device using a PowerStack package.

A cross-section (figure 2) of a Power Block device utilizing the PowerStack technology reveals high-side and low-side MOSFETs held in place by thick copper clips. The low-side die is attached to the foundational pad of the lead frame and this provides the ground connection for the low-side MOSFET. Such a construction delivers substantial benefits to power subsystem designers in terms of board space savings, current levels, power efficiencies and thermal management.

Board space savings

Reducing board space is particularly critical today as many high-performance computing and telecommunications products migrate to smaller form factors. The board space savings made possible by a 3D packaging innovation are substantial. Unlike previous generations of packaging technologies that were largely limited to the width and depth (x and y) dimensions, PowerStack builds on these while ascending along the height (z) or third dimension. Vertical assembly fabricating of two MOSFETs in the same package reduces the footprint of a synchronous buck converter to more than half that of an implementation featuring two discrete MOSFETs. Integrating a driver/controller into the same PowerStack package reduces board space requirements even further. The flexibility and scalability of PowerStack packaging is such that a catalog off-the-shelf driver/controller device can be readily integrated into the same package or a customized solution can be developed to meet the specific needs of a certain application.

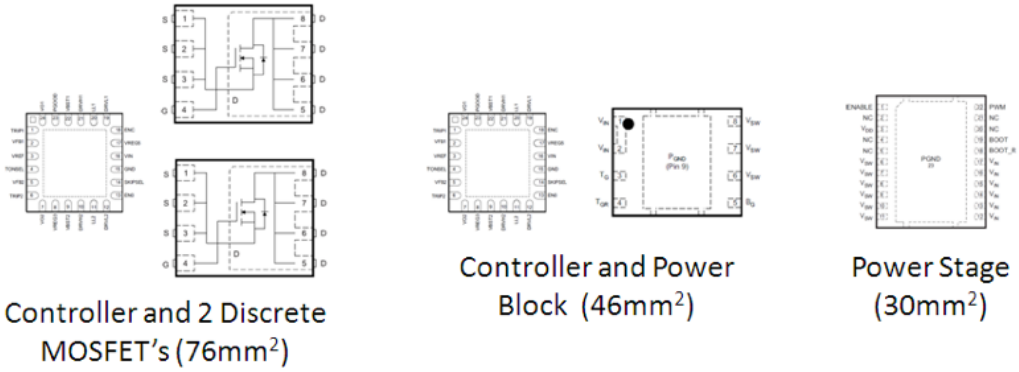

Figure 3: Board space savings for a typical circuit resulting from PowerStack.

High current levels

The schematic in figure 4 illustrates the very low levels of electrical parasitic elements found in a device placed in a PowerStack package. In this case, both the magnitudes and occurances of parasitic resistances, R, and inductances, L, are reduced. As a result, higher currents and switching rates are enabled as well as reduced conduction and switching losses. Faster switching speeds are especially valuable for power management subsystems because the size of the external inductor can be reduced and the inductor is often the largest and most expensive device in a power management subsystem. This further reduces board space requirements and illustrates that innovative power management subsystem design with PowerStack technology can have benefits far beyond the PowerStack component itself.

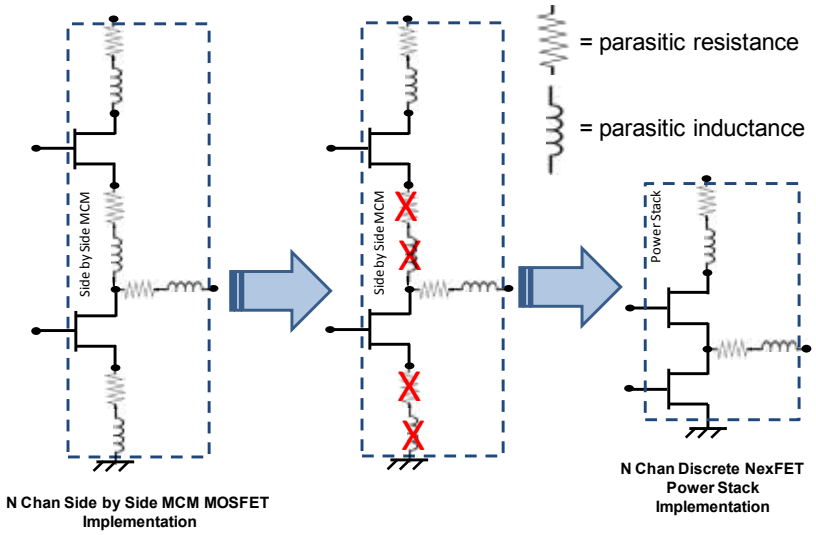

Figure 4: PowerStack delivers low parasitic losses to support high current levels and high switching frequency.

Power efficiency

Because PowerStack enables reductions in electrical parasitic switching and conduction losses, stacking two MOSFETs in a PowerStack package actually achieves higher conversion efficiencies when compared to a converter which implements two discrete MOSFETs. The power efficiency curves below (figure 5) shows that the integrated stacked packaging technology dissipates less energy in its circuitry than would two MOSFETs side-by-side on a circuit board.

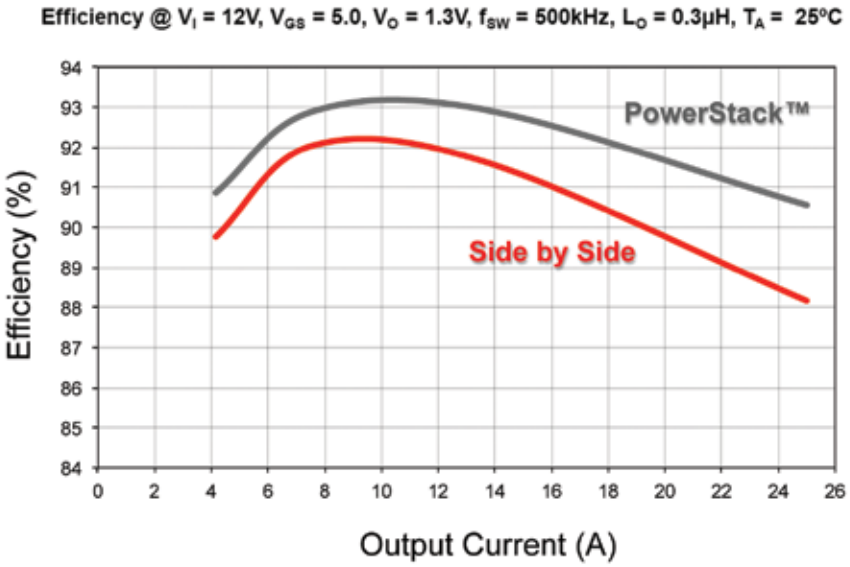

Figure 5: Power efficiency curves for PowerStack and a discrete two-MOSFET implementation.

Thermal management

Another advantage of PowerStack packaging technology is its thermal performance. Because of PowerStack's low electrical parasitics, switching and conduction losses can be reduced, resulting in less power dissipation or heat generated. Reduced power dissipation is one of the most critical system design factors in computing and telecom applications because total energy and cooling costs can be reduced, and a portion of the system's thermal budget is freed up for the high-performance and heat-generating DSPs and microprocessors that may be present.

The thermal performance of systems with PowerStack technology is also improved as a result of the construction of the package itself. With NexFET MOSFETs in a PowerStack package the exposed pad on the bottom of the package is at ground potential and the ground plane or planes are typically the largest and most significant thermal-spreading planes on a system board. That is, PowerStack packaging has been thermally optimized by leveraging the best thermal-spreading layer or layers available (as seen in figure 6). In contrast, traditional discrete MOSFETs or side-by-side co-packaged MOSFET devices place the MOSFETs on the Switch Node (Sync FET) and the Input Node (Control FET). These nodes are not nearly as effective at spreading heat (as seen in figure 7) as the ground node because they are electrically noisy and this dictates that they must be small and isolated on the board. This is clearly demonstrated with the thermal measurement data shown in figure 8.

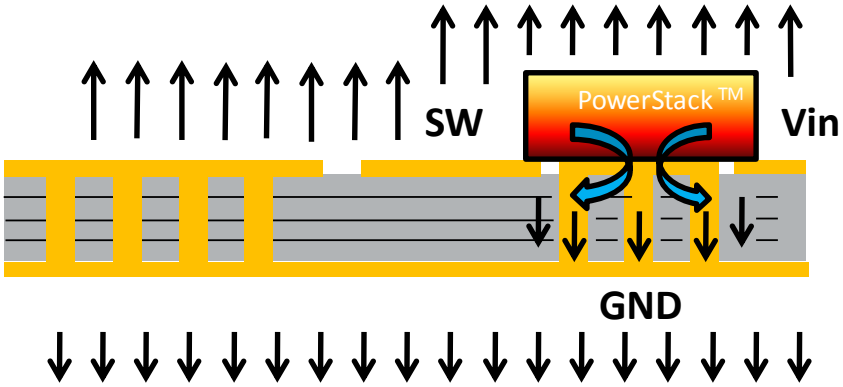

Figure 6: Optimal thermal path through grounded thermal pad of PowerStack Package.

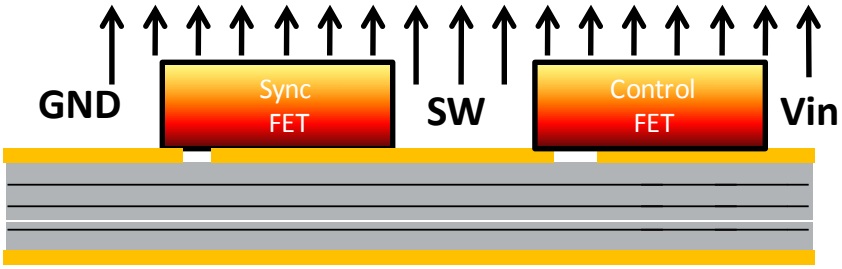

Figure 7: Limited thermal path through SW node and Vin node of side by side MOSFET's.

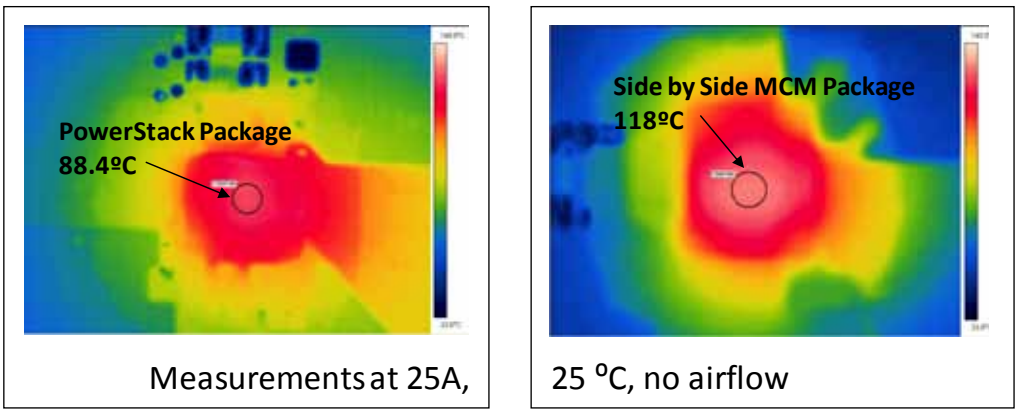

Figure 8: Thermal measurements comparing PowerStack and side by side MCM.

Reliability

Reliability is an important requirement in power management packaging, and therefore worth mentioning here, because it is typically a very high priority in the applications where power management is deployed. PowerStack packaging technology has demonstrated its reliability performance in Power Block devices and the fully integrated products that have been comprehensively tested and meet or exceed TI's stringent standards for quality, durability and reliability. The efficient heat dissipation capabilities of the PowerStack packaging technology contributes to the reliability of devices like Power Block and others, because it helps to reduce the operational temperature of the component over its entire life.

The role of packaging

TI's PowerStack packaging technology demonstrates that a chip's package plays a critical role in the performance parameters and overall specification characteristics of semiconductor devices. Particularly in TI's Power Block family of synchronous buck converters, PowerStack has shown that newly emerging 3D stacking innovations can optimize the most important aspects of a power device, including board space footprint, power efficiency, high current levels and thermal management. In many applications such as high-performance computing, telecommunications and battery management, PowerStack technology is able to greatly enhance the performance of the system and reduce the form factor of end products. Additional advancements in packaging technologies in general and PowerStack technology in particular will certainly continue in the future.

For more information

Visit **www.ti.com/powerstack**

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