Application Report
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Mode Pin Precautions for TPD2S701-Q1 and TPD2S703-Q1

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ABSTRACT

In the TPD2S701-Q1 and TPD2S703-Q1 overvoltage protection devices, the MODE corner pin must be set up correctly to ensure the devices enter the correct mode. If the MODE pin loses connection, breaks, or is otherwise floating there is potential for damage to downstream devices. This application report will show the MODE pin functionality, effects of faults associated with the MODE pin, and solutions that protect all devices connected.

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1 Introduction

The TPD2S701-Q1 and the TPD2S703-Q1 family of devices are used for overvoltage and ESD protection of the USB data lines D+ and D–. The TPD2S701-Q1 has short-to-V_{BUS} protection while the TPD2S703-Q1 has short-to-V_{BUS} and short-to-battery protection.

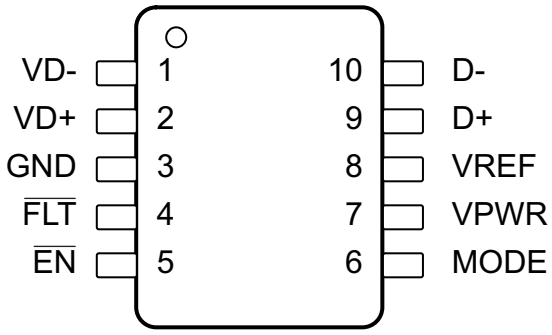

Figure 1. Pinout of TPD2S701-Q1 and TPD2S703-Q1

Both TPD2S701-Q1 and TPD2S703-Q1 have the same pinout as in Figure 1. Pin 6 in both the DGS and the DSK packages is the MODE pin. This pin selects between the two device modes: Mode 0 where there is an external supply to the VREF pin that sets the overvoltage protections, and Mode 1 that can be thought of as an internal voltage regulator for VREF whose output is controlled by the feedback being produced in the resistor divider at the MODE pin. In essence, this pin is the deciding factor for whether pin 8, VREF, is an input being supplied with an external reference or if VREF is an output to which an internal LDO is outputting nominally 3.3 V. This functionality can be modeled in Figure 2

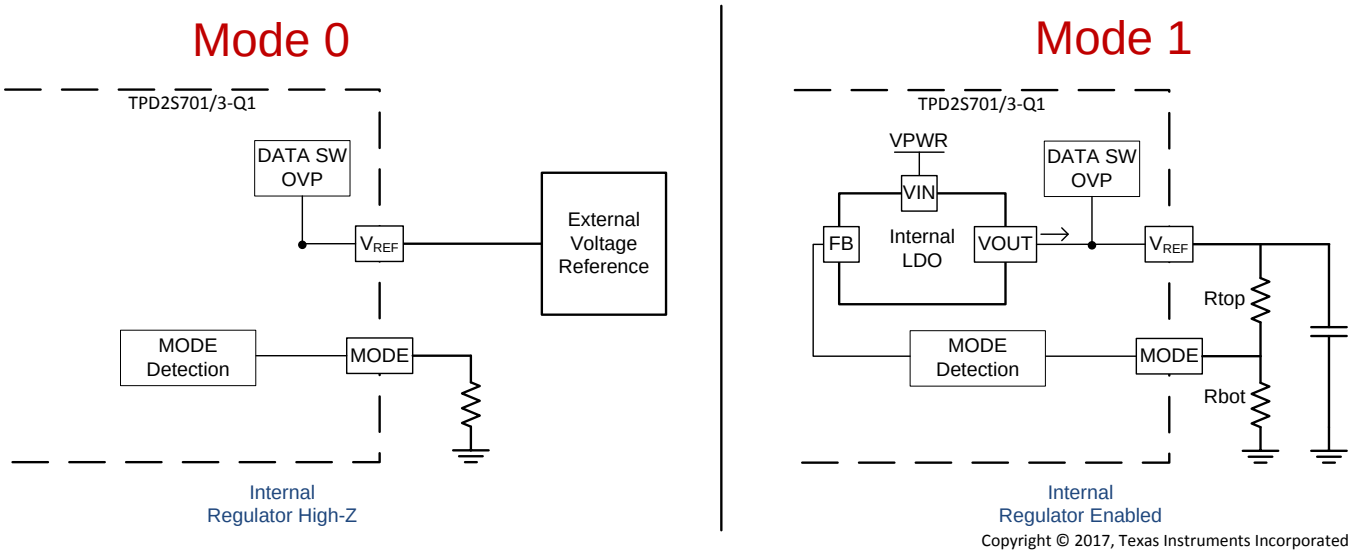

Figure 2. Mode Functionality Block Diagram

2 How to Set Mode

The way that the TPD2S701/3-Q1 can distinguish between the two modes is through the resistance the MODE pins see with respect to ground. If it sees that the resistance to ground is less than 2.6 kΩ, it knows that an external power supply will power VREF which is classified as mode 0. For the device to know that it is in mode 1, the parallel resistance of the resistor from the MODE pin to VREF, Rtop, and MODE pin to ground, Rbot is greater than 14 kΩ. When the device powers up, it delays 150 µs to measure the resistance from the MODE pin to ground to see what mode it should be set in. Additionally, it will take extra time to turn on if set in mode 1 because the capacitor on VREF has to be charged. This

charging time is outlined in the data sheet in Section 9.2.2.2. The reason that mode 1 has to do with the parallel resistance of Rtop and Rbot instead of just Rbot is that when the device is initially powered the VREF pin, when not externally powered, is considered as ground too. Therefore, to be certain the device is in a known state, the resistor from MODE to ground must be less than 2.6 kΩ or the parallel resistance of MODE to VREF and MODE to ground must be greater than 14 kΩ.

3 Mode Pin Faults

However, even when the schematic for this device is properly set up, faults can still occur if the MODE pin somehow becomes disconnected or is otherwise floating. For example, system damage may occur if the device is intended to be in mode 0 where an external 3.3-V supply is connected to VREF. If the MODE pin then becomes floating, there is a chance that the mode detection circuitry could mistakenly put the device into mode 1 where it would then try to drive an output on VREF.

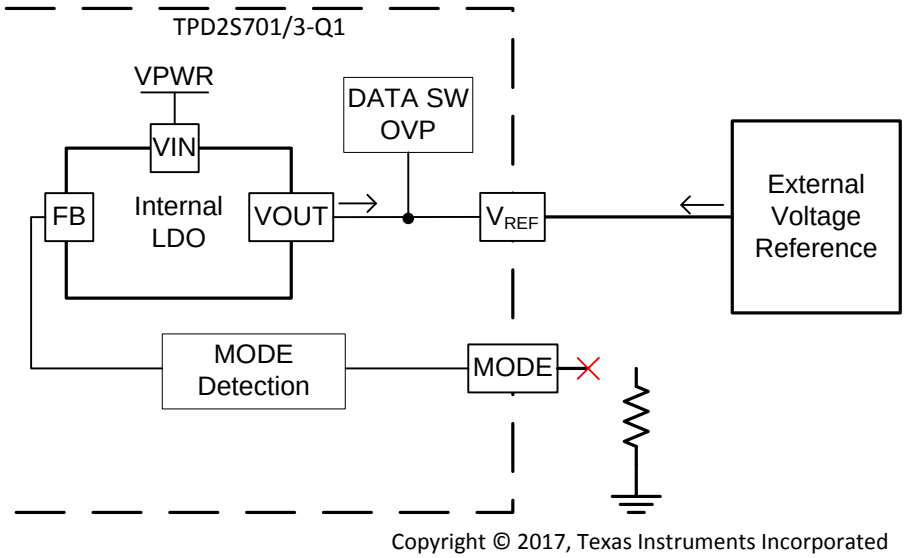

Figure 3. MODE Pin Fault

As Figure 3 shows, the MODE pin is disconnected from the resistor to ground and the mode detection circuitry has provided feedback to the internal regulator which caused the regulator to come out of High-Z mode and start driving against the external voltage reference. The internal regulator is based on V_{PWR} which can be up to 7 V. If the output of the internal regulator to V_{REF} is at or near 7 V, the external voltage reference would begin sinking 50 mA of current (set by the internal current limit of V_{REF}) since the potential of V_{REF} is higher than its own output. If any other components were connected to the same rail as the external voltage reference, they would all be brought up to V_{REF}, which could also damage some devices without a maximum rated voltage of > 7 V.

4 Solutions

Solutions to this issue are simple. The first solution that can be done is put a blocking diode from the external voltage reference to V_{REF}. This diode will protect all downstream devices if the MODE pin fault occurs. Consideration should be given to the voltage drop across the diode. This is shown in Figure 4.

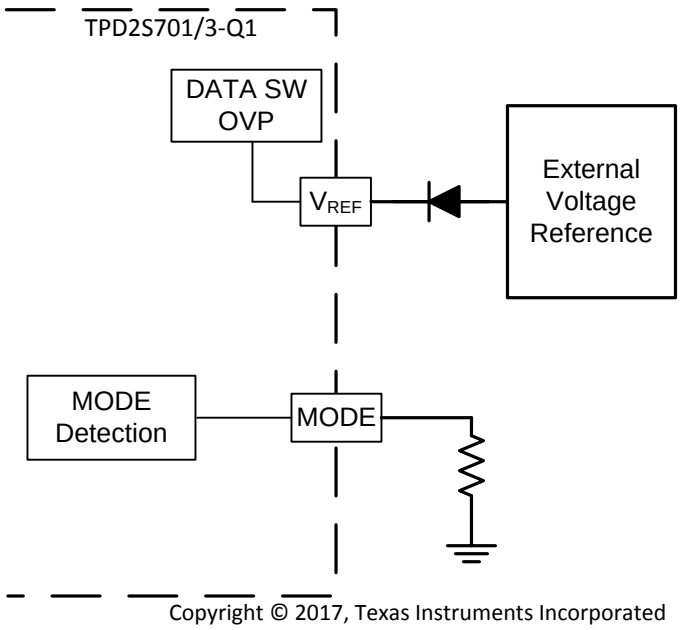

Figure 4. Diode Fix

However, this solution will not completely solve the issue because the TPD2S701/3-Q1 OVP threshold will not be at the same value as intended by the output of the external voltage reference. Therefore, another solution is to place a bias resistor and a zener diode from the external reference to V_{REF}, shown in Figure 5.

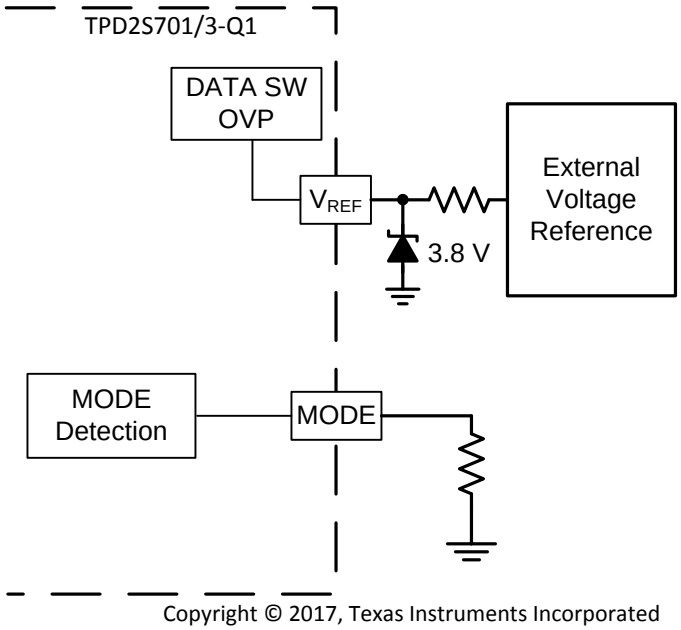

Figure 5. Zener Diode Fix

This would mean that V_{REF} would always stay in the recommended operating range keeping the device in a good state. Note that the zener diode can be set to whatever rail voltage the external voltage reference is at as long as it is within the recommended operating conditions of the device.

5 Summary

When functioning properly, the TPD2S701-Q1 and TPD2S703-Q1 are excellent devices for overvoltage and ESD protection on the data lines of a USB controller. While environmental factors can cause the device to be in a different mode than expected, taking preliminary actions as outlined can protect downstream circuitry and the device itself.

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