Application Note

High-Speed Layout Guidelines for Signal Conditioners and USB Hubs

ABSTRACT

As modern interface frequencies scale higher, care must be taken in the printed circuit board (PCB) layout phase of a design to maintain a robust design. This document focuses on high speed layout guidelines relating to USB, USB Hubs, HDMI, DisplayPort®, PCIe, and SATA.

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1 Introduction

Scope

This application report can help system designers implement best practices and understand PCB layout options when using different high speed signals. This document is intended for audiences familiar with PCB manufacturing, layout, and design.

Critical Signals

A primary concern when designing a system is accommodating and isolating high-speed signals. As high-speed signals are most likely to impact or be impacted by other signals, high-speed signals must be laid out early (preferably first) in the PCB design process to verify that prescribed routing rules can be followed.

Table 1-1. Critical Signals

Signal Name	Description
DP/DM	USB 2.0 differential data pair
SSTXP/N,SSRXP/N	SuperSpeed differential data pair
SATA_RXP/N, SATA_TXP/N	Serial ATA (SATA) differential data pair
PCIe_RXP/N, PCIe_TXP/N	PCI-Express (PCIe) differential data pair
HDMI_CLK+/-	High-Definition Multimedia Interface (HDMI) differential clock pair, positive or negative
HDMI_Data+/-	High-Definition Multimedia Interface (HDMI) differential data pair, positive or negative
DP_Lane#+/-	DisplayPort differential data pair, Lane 0 through 3, positive or negative

2 Protocol Specific Layout Guidelines

There are many differences in the various high-speed standards that need to be taken into account when designing the layout of a system. These differences include parameters like data-rates/frequency, AC coupling capacitors, inter-pair skew, intra-pair skew, and trace impedance. Below are standard values for the different high standards. The following values are guidelines and are not always exact values.

2.1 USB 2.0

Parameter	Value
Frequency	Low speed: 750KHz (1.5Mbps)
	Full Speed: 6MHz (12Mbps)
	High Speed: 240MHz (480Mbps)
AC Coupling Capacitors	No AC capacitors allowed
Polarity Reversal	Not allowed
Trace Impedance	90Ω ±15% differential, 45Ω ±15% single ended
Max Cable Length	5m

2.2 USB 4.0 3.2 Gen1/Gen2

Parameter	Value
Frequency	SuperSpeed: 2.5Ghz (5Gbps)
	SuperSpeed: 5Ghz (10Gbps)
	USB 4.0 Gen3: 10Ghz (20Gbps NRZ)
	USB 4.0 Gen4: 20Ghz (40Gbps PAM3)
AC Coupling Capacitors	AC capacitors required on the TX data lane. (Optional on the RX data lane)
Polarity Reversal	Allowed on SSTX and SSRX
Max Intra-Pair Skew	15 ps/m (TI recommends 5 mils
Max Inter-Pair Skew	NA
Trace Impedance	90Ω ±15% differential; 45Ω ±15% single ended
Max Cable Length	3m

2.3 HDMI

Parameter	Value
Frequency	HDMI 1.4b: HDMI_CLK: up to 340MHz
	HDMI 1.4b: HDMI_Data: up to 1.7Ghz
	HDMI 2.0b: HDMI_CLK: up to 150MHz
	HDMI 2.0b: HDMI_Data: up to 3Ghz
	HDMI 2.1b: HDMI_Data: up to 6Ghz
AC Coupling Capacitors	No AC capacitors allowed
Polarity Reversal	Not allowed
Max Intra-Pair Skew for Source	0.15 × Tbit
Max Inter-Pair Skew for Source	0.20 × Tcharacter
Trace Impedance	100Ω ±15% differential; 50Ω ±15% single ended

2.4 DisplayPort

Parameter	Value
Frequency	DisplayPort 1.2: 2.7GHz (5.4Gbps)
	DisplayPort 1.4: 4.05GHz (8.1Gbps)
	DisplayPort 2.1 UHBR10: 5GHz (10Gbps)
	DisplayPort 2.1 UHBR13.5: 5.76GHz (13.5Gbps)
	DisplayPort 2.1 UHBR20: 10GHz (20Gbps)
AC Coupling Capacitors	AC capacitors required
Polarity Reversal	No built in support
Max Intra-Pair Skew for Source	20ps (TI recommends about 5 mils)
Trace Impedance	100Ω ±10% differential; 50Ω ±15% single ended

3 General High-Speed Signal Routing

3.1 Trace Impedance

For high speed signals trace impedance needs to designed as to minimize the reflections in traces. There are two types of trace impedance that need to be taken into consideration when designing high speed signals. Single ended impedance is the trace impedance with reference to ground. Differential impedance is the impedance between two differential pair signal traces.

The high speed protocol that is being designed for determines what the single and differential trace impedance the traces need to meet as well as the tolerance for the impedance (for example, 50Ω ±15%). To have designs be robust from PCB manufacturing errors and defects design the traces impedance be as close to the recommended value. The geometry of the traces, the permittivity of the PCB material and the layers surrounding the trace all impact the impedance of the signal trace.

There are many tools available to calculate the trace impedance on high speed traces. Most board manufactures have a preferred tool that PCB designers can use to calculate the impedance but there are also many available online.

3.2 High-Speed Signal Trace Lengths

As with all high-speed signals, keep total trace length for signal pairs to a minimum. Some standards have a maximum trace/ cable length which is specified in the various specifications.

3.3 High-Speed Signal Trace Length Matching

Match the etch lengths of the relevant differential pair traces. Intra-pair skew is the term used to define the difference between the etch length of the + and - lane of a differential pair. Inter-pair skew is used to describe the difference between the etch lengths of a differential pair from another differential pair of the same group. The etch length of the differential pair groups do not need to match. For example the etch lengths of USB 3.0 TX and RX do not need to match. There are also standards that do not have a Inter-pair skew requirement because the different lanes do not have to be the same length. When matching the intra-pair skew of the high-speed signals, add serpentine routing to match the lengths as close to the mismatched ends as possible refer to Figure 3-1.

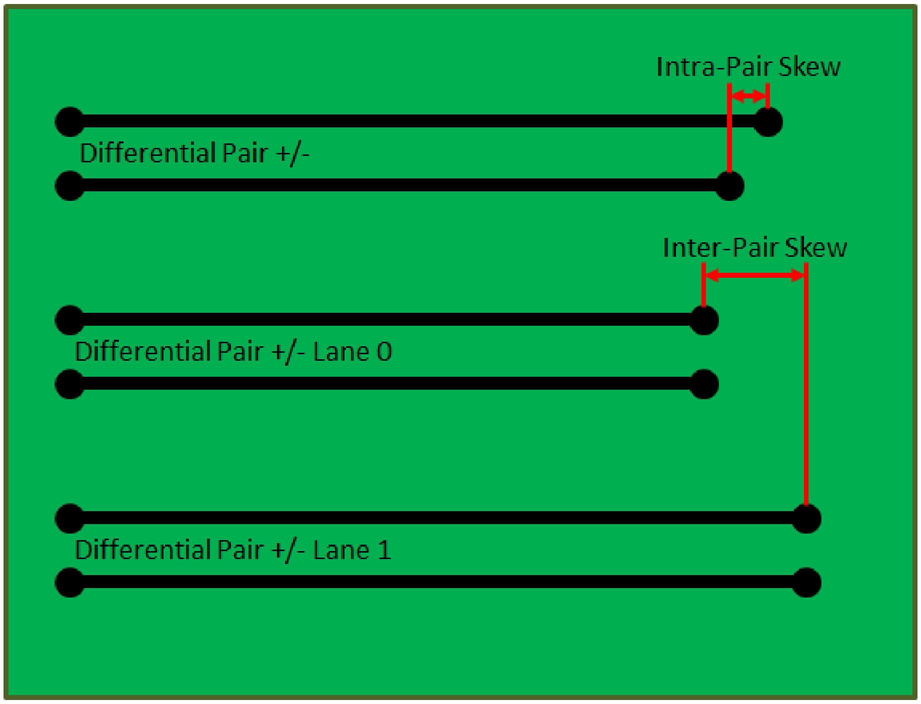

Figure 3-1. Inter versus Intra Pair Skew

Use the above recommendations for the traces serpentine geometry. For example the width of the trace(W) is 6 mils and the distance between the differential pair(A) is 8 mils. These mean that the width of the serpentine(B) is at least 16 mils and the length of C is at least 18 mils.

3.4 Return Path

An electrical circuit must always be a closed loop system. With DC, the return current takes the way back with the lowest resistance for DC signals.

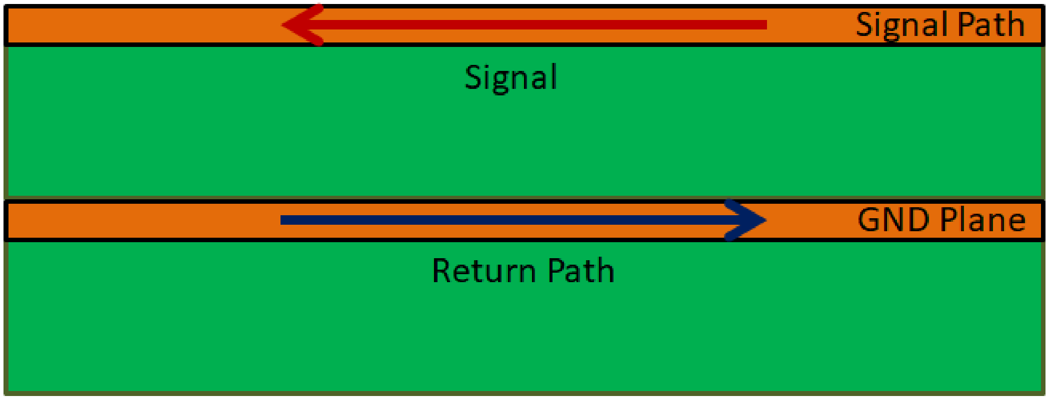

Figure 3-2. Return Path

At higher frequencies, the return current flows along the lowest impedance path, this lowest impedance path is usually the reference plane adjacent to the signal see Figure 3-3. For this reason, always have a ground plane or power plane on the layer above or below a signal layer. This return path helps to reduce impedance changes and decrease EMI issues. The red arrows are the signal path and the blue arrows are the return path.

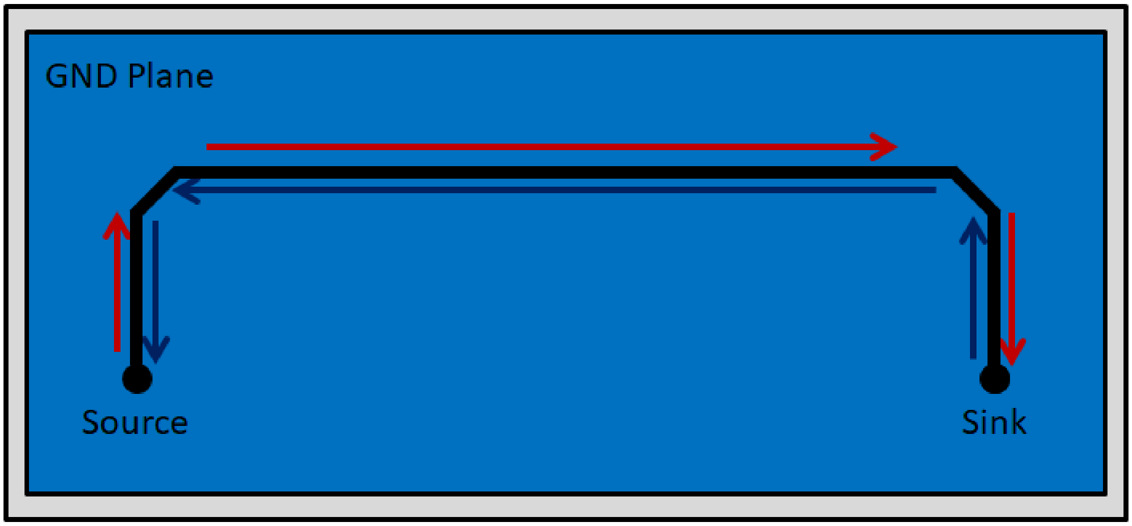

Figure 3-3. High Frequency Return Path

3.5 High-Speed Signal Reference Planes

High-speed signals should be routed over a solid GND reference plane and not across a plane split or a void in the reference plane unless absolutely necessary. TI does not recommend high-speed signal references to power planes unless completely unavoidable.

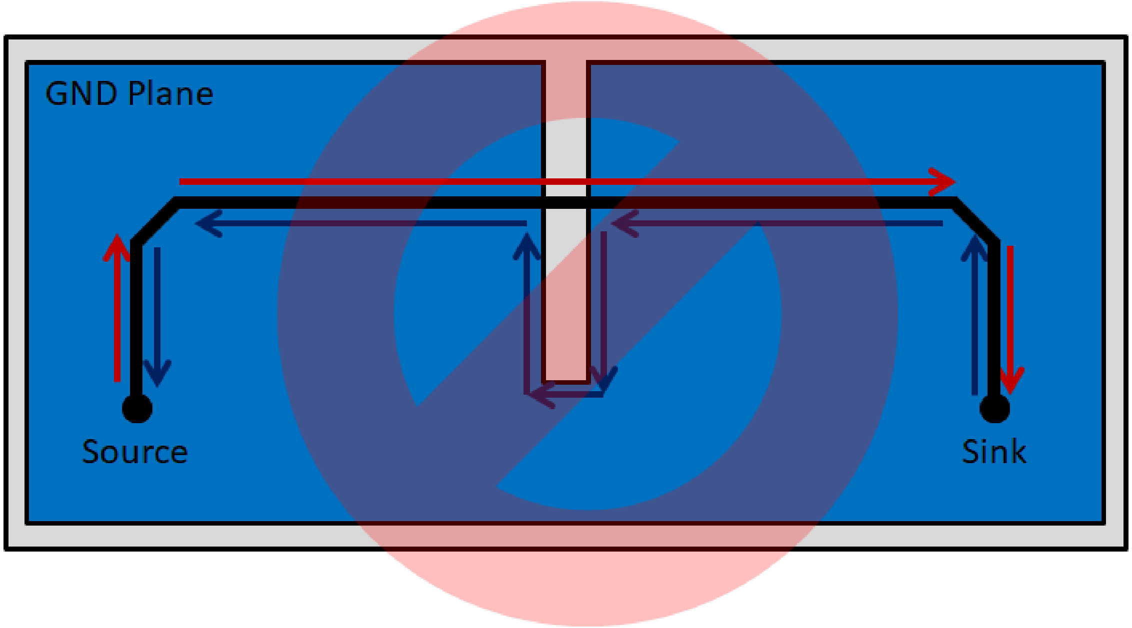

Figure 3-4. Rerun Across Split Plane

Routing across a plane split or a void in the reference plane forces return high-frequency current to flow around the split or void. Figure 3-4 shows that the return path must take a longer route than the signal path this can result in the following conditions:

- Excess radiated emissions from an unbalanced current flow
- Delays in signal propagation delays due to increased series inductance
- – Interference with adjacent signals
  – Degraded signal integrity (that is, more jitter and reduced signal amplitude)

  If routing over a plane-split is completely unavoidable, place stitching capacitors across the split to provide a return path for the high-frequency current. These stitching capacitors minimize the current loop area and any impedance discontinuity created by crossing the split. These capacitors should be 1μF or lower and placed as close as possible to the plane crossing.

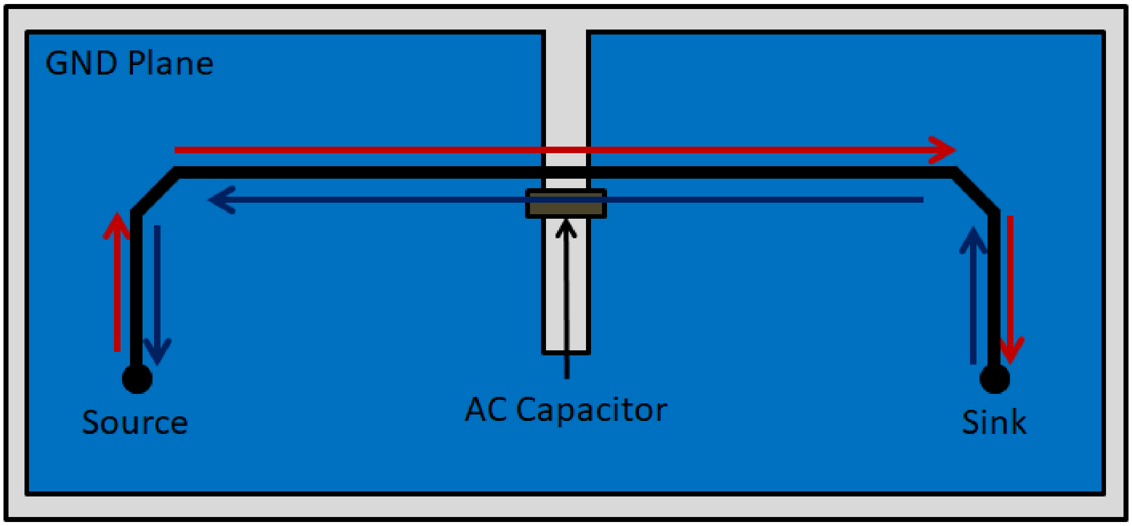

Figure 3-5. AC Capacitor Across Split Plane

When planning a PCB stackup, verify that planes that do not reference each other are not overlapped because this produces unwanted capacitance between the overlapping areas.

Avoid routing across different reference planes because this can cause impedance issues as well as EMI issues.

Do not change the reference plane of the high speed signal trace unless completely unavoidable. *The red arrows are the signal path and the blue arrows are the return path.*

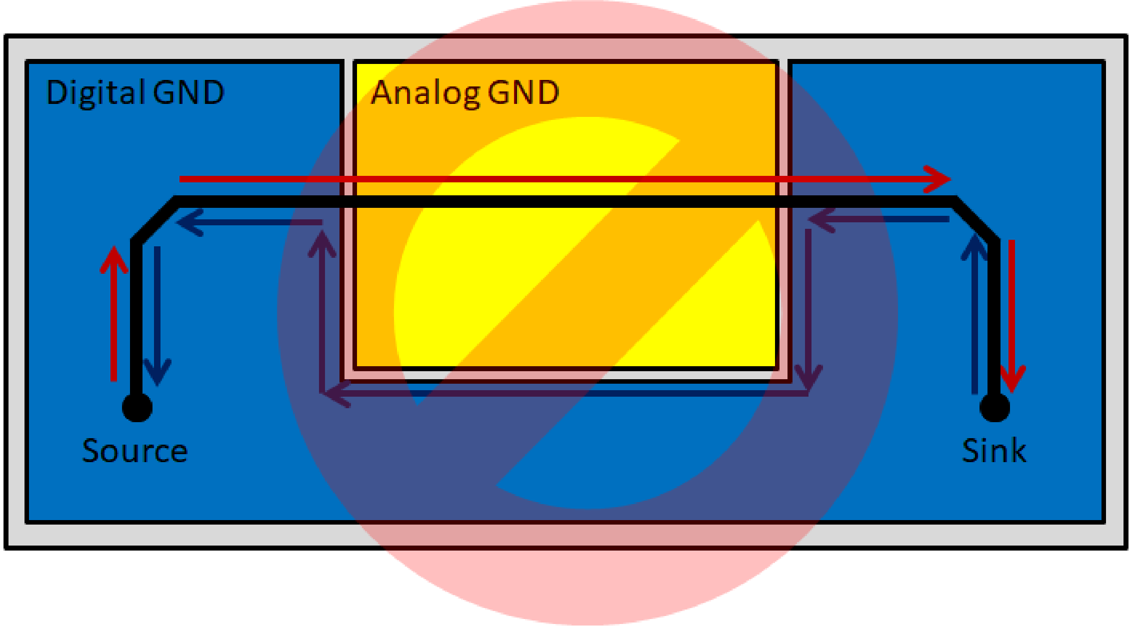

Figure 3-6. Routing Across Different Reference Planes

If routing across different reference planes cannot be avoided use AC capacitors to allow the return current to have a pathway.

The red arrows are the signal path and the blue arrows are the return path.

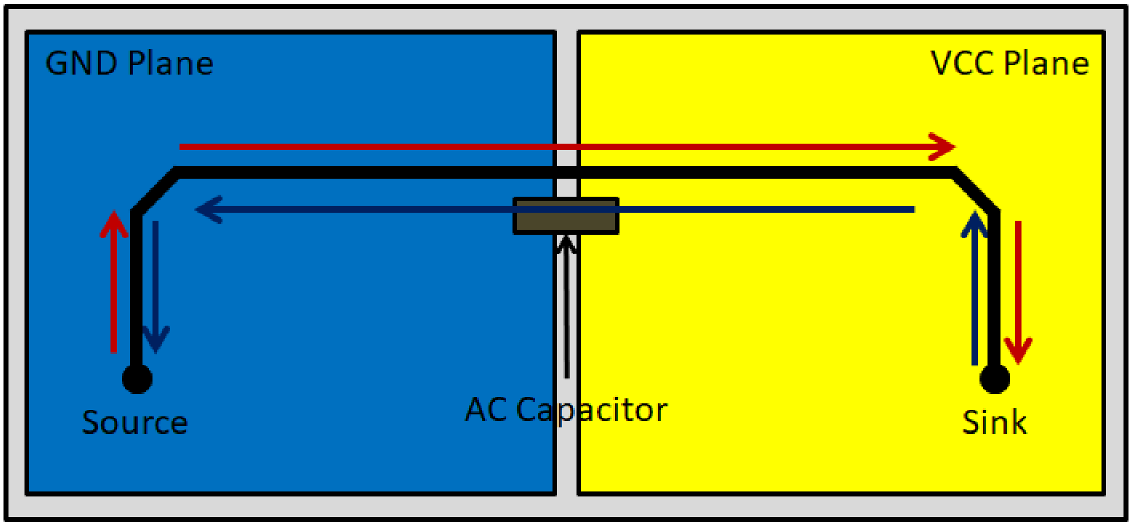

Figure 3-7. Routing Across Different Reference Planes with AC Capacitor

The entirety of any high-speed signal trace must maintain the same GND reference from origination to termination. If unable to maintain the same GND reference, via-stitch both GND planes together to maintain continuous grounding and uniform impedance. Place these stitching vias symmetrically within 200 mils (center-to-center, closer is better) of the signal transition vias.

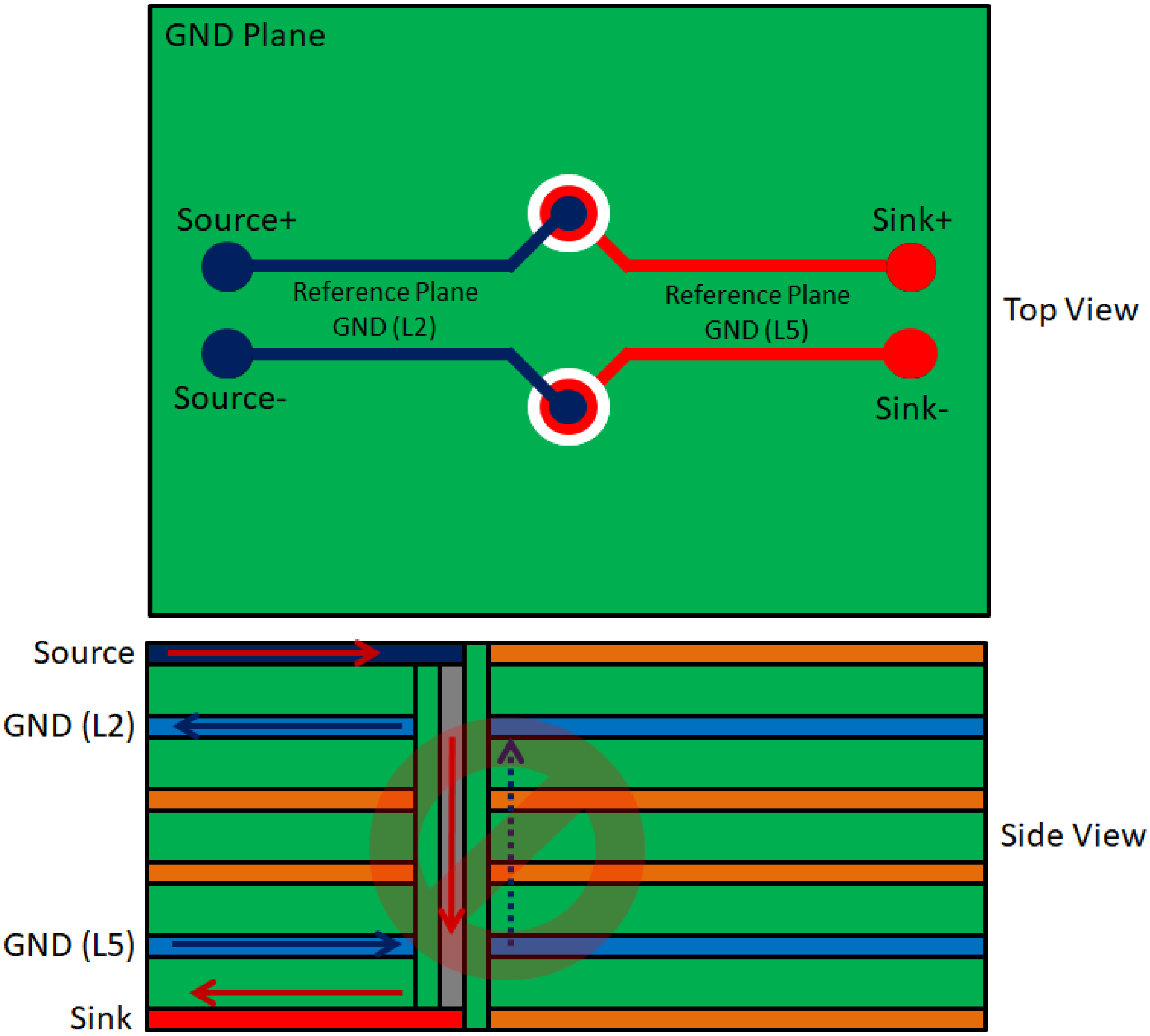

Figure 3-8. Differential Pair Via Return Path Without GND Vias

The red arrows are the signal path and the blue arrows are the return path

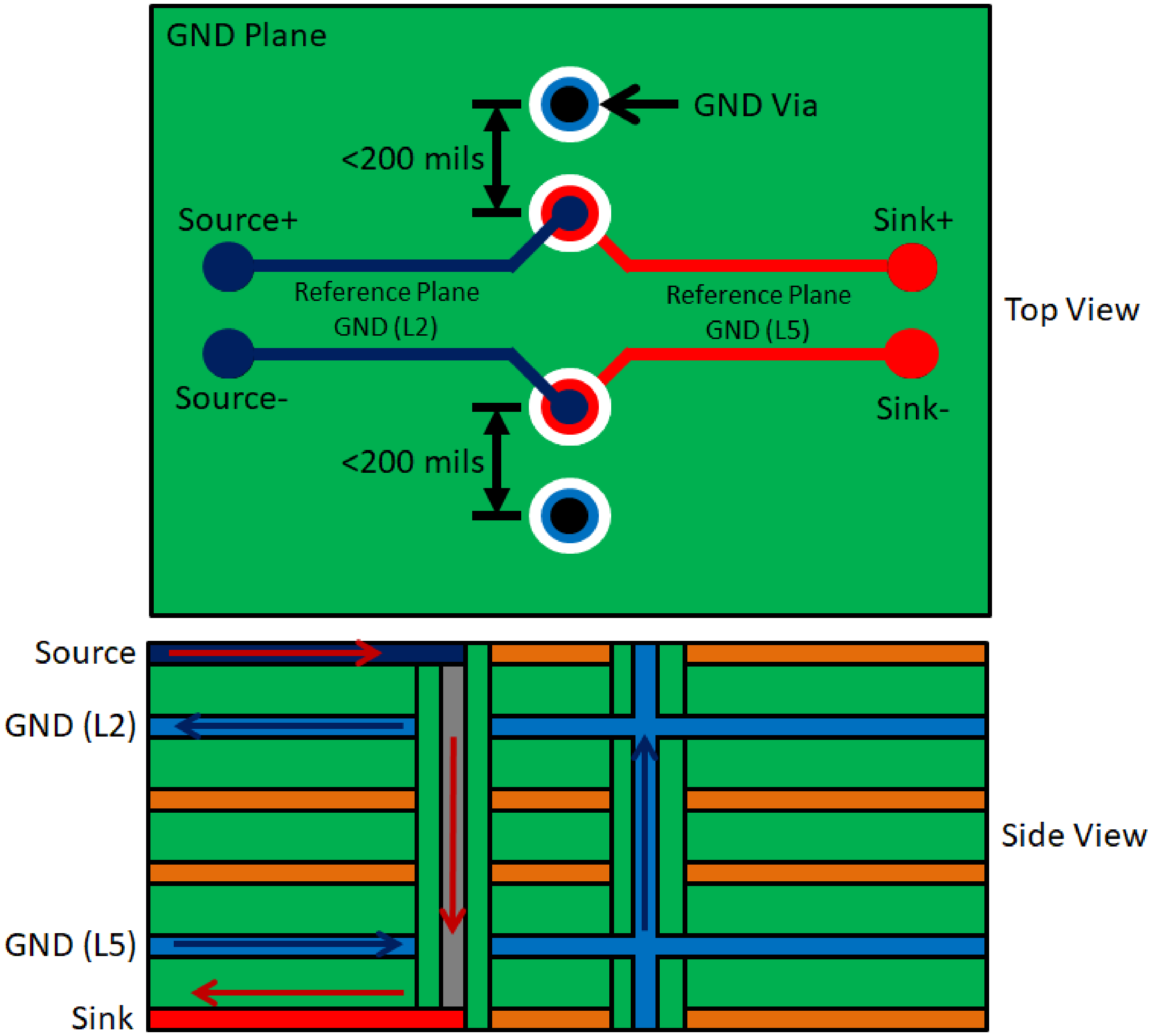

Figure 3-9. Differential Pair Via Return Path With GND Vias

TI does not recommend high-speed signal references to power planes unless completely unavoidable. If unavoidable, use AC coupling capacitors and ground vias to allow the return signal to have a path back from the sink to the source. Figure 3-10 depicts the use of AC coupling capacitors and ground vias for the return path. *The red arrows are the signal path and the blue arrows are the return path*.

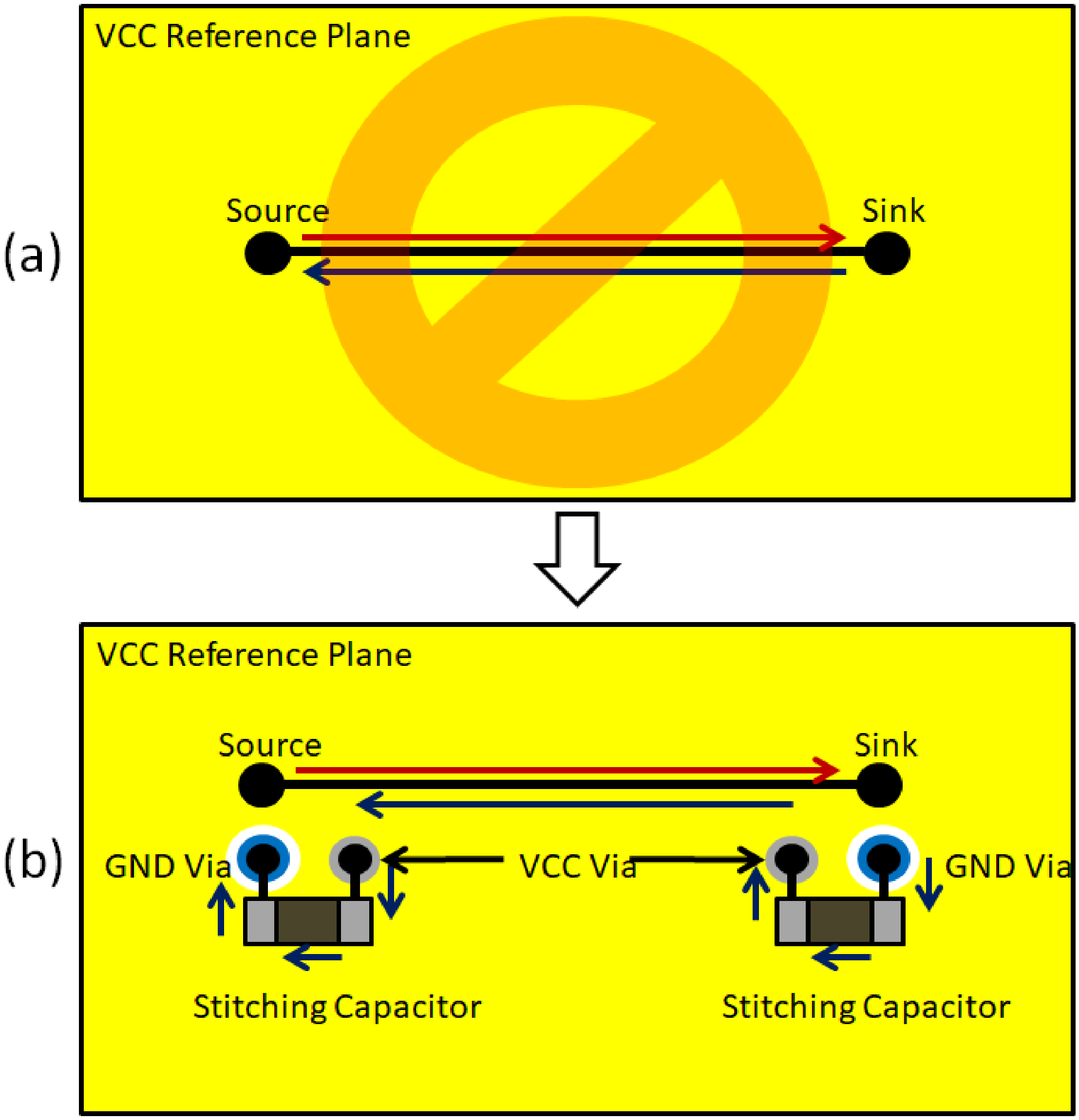

Figure 3-10. VCC Reference Plane

4 High-Speed Differential Signal Routing

4.1 Differential Signal Spacing

To minimize crosstalk in high-speed interface implementations, the spacing between the signal pairs must be a minimum of 5 times the width of the trace. This spacing is referred to as the 5W rule. A PCB design with a calculated trace width of 6 mils requires a minimum of 30 mils spacing between high-speed differential pairs. Also, maintain a minimum keep-out area of 30 mils to any other signal throughout the length of the trace. Where the high-speed differential pairs come adjacent to a clock or a periodic signal, increase this keep-out to a minimum of 50 mils to maintain proper isolation. For examples of high-speed differential signal spacing, see Figure 4-1 and Figure 4-2.

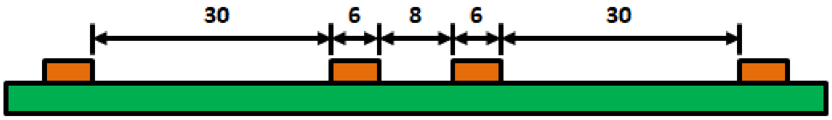

Figure 4-1. Differential Pair Spacing Next to Other Signals

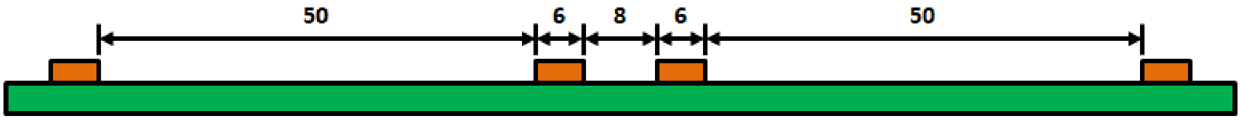

Figure 4-2. Differential Pair Spacing Next to Clock or a Periodic Signal

In devices that include multiple high-speed interfaces, avoiding crosstalk between these interfaces is important. To avoid crosstalk, maintain that each differential pair is not routed within 30 mils of another differential pair after package escape and before connector termination.

4.2 Additional High-Speed Differential Signal Rules

- Do not place probe or test points on any high-speed differential signal.
- Do not route high-speed traces under or near crystals, oscillators, clock signal generators, switching power regulators, mounting holes, magnetic devices, or ICs that use or duplicate clock signals.
- After BGA breakout, keep high-speed differential signals clear of the SoC because high current transients produced during internal state transitions can be difficult to filter out.
- When possible, route high-speed differential pair signals on the top or bottom layer of the PCB with an adjacent GND layer. TI does not recommend stripline routing of the high-speed differential signals.
- Verify that high-speed differential signals are routed ≥ 90 mils from the edge of the reference plane.
- Verify that high-speed differential signals are routed at least 1.5W (calculated trace-width × 1.5) away from voids in the reference plane. This rule does not apply where SMD pads on high-speed differential signals are voided.
- Maintain constant trace width after the SoC BGA escape to avoid impedance mismatches in the transmission lines.
- Maximize differential pair-to-pair spacing when possible.

4.3 Symmetry in the Differential Pairs Reference

Route all high-speed differential pairs together symmetrically and parallel to each other. Deviating from this requirement occurs naturally during package escape and when routing to connector pins. These deviations must be as short as possible and package break-out must occur within 0.25 inches of the package.

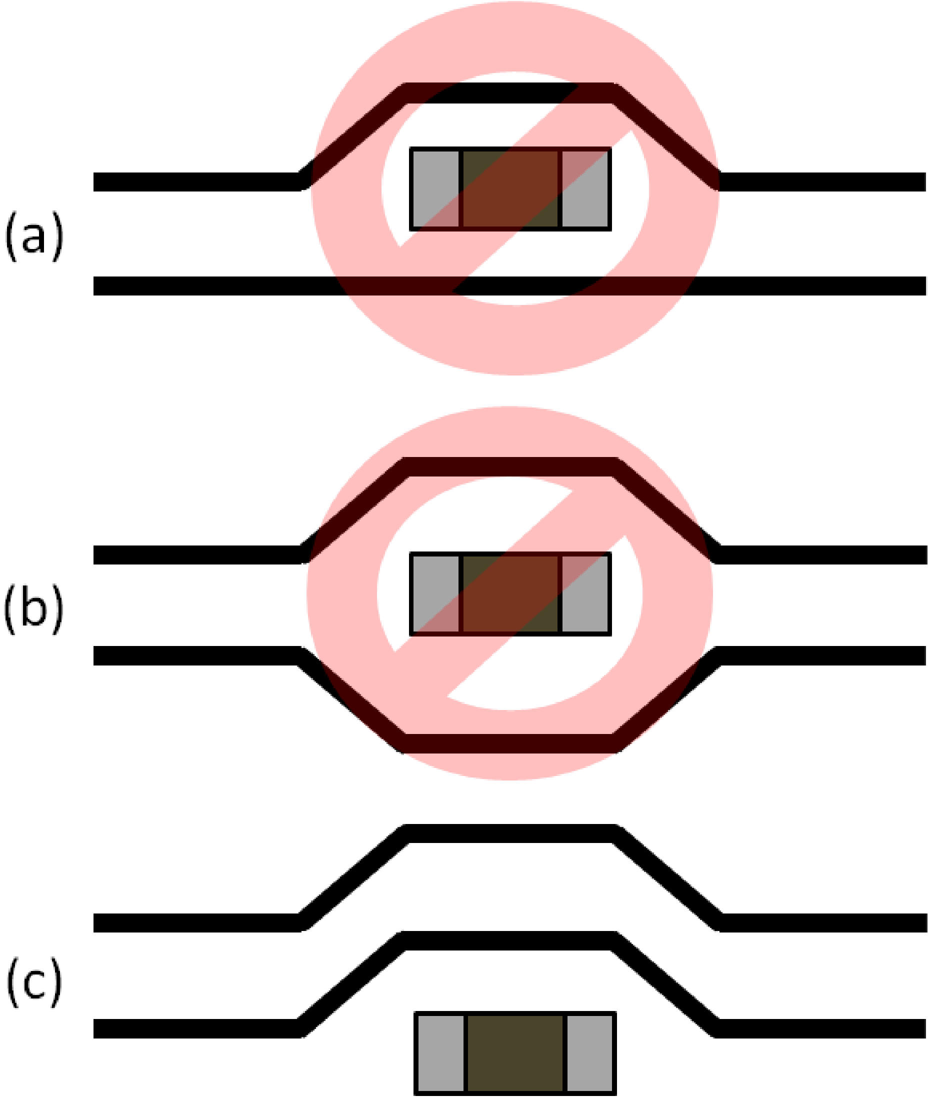

Figure 4-3. Differential Pair Symmetry

4.4 Connectors and Receptacles

When implementing a through-hole receptacle (like a USB Standard-A), TI recommends making high-speed differential signal connections to the receptacle on the bottom layer of the PCB. Making these connections on the bottom layer of the PCB prevents the through-hole pin from acting as a stub in the transmission path. For surface-mount receptacles such as USB Micro-B and Micro-AB, make high-speed differential signal connections on the top layer. Making these connections on the top layer eliminates the need for vias in the transmission path. For examples of USB through-hole receptacle connections.

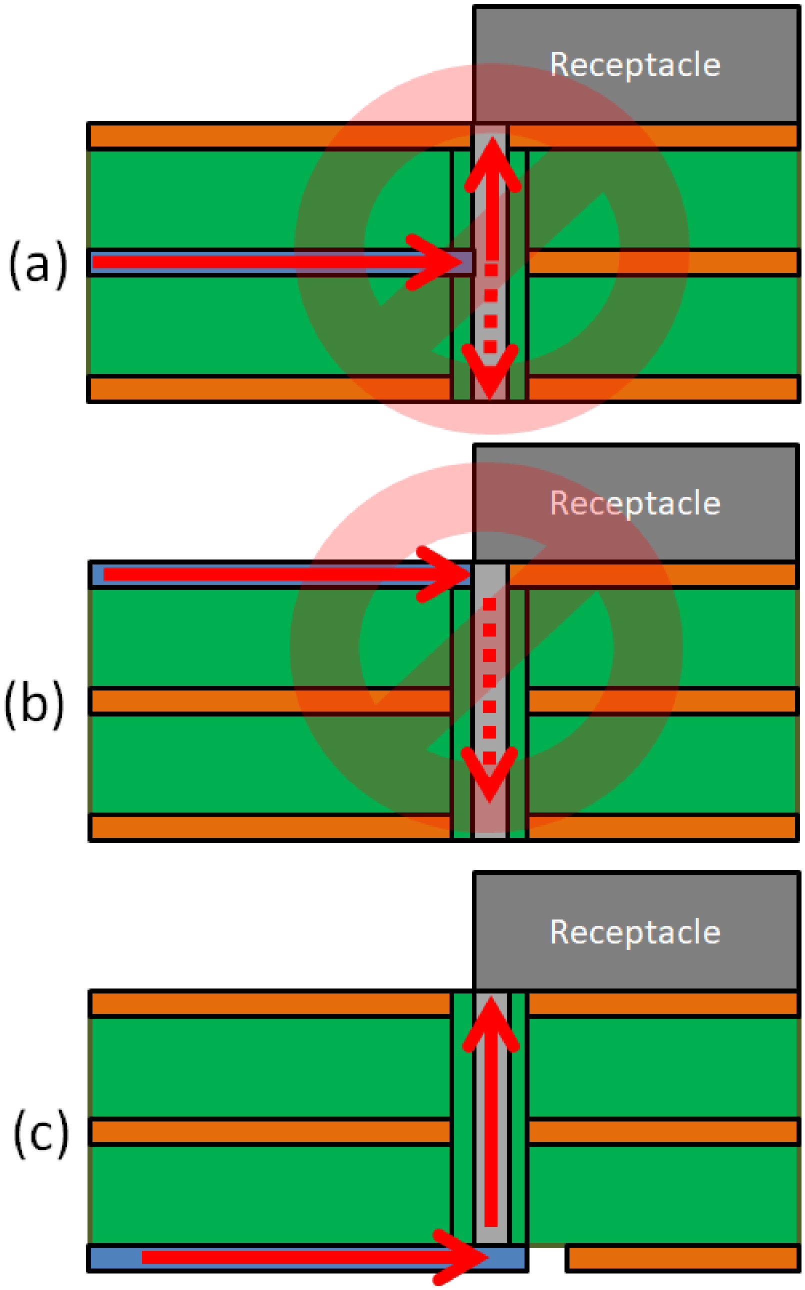

Figure 4-4. Receptacle Stubs Mitigation

- A: Signal coming from the middle of the PCB
- B: Signal coming from the top of the PCB
- C: Signal coming from the bottom of the PCB

4.5 Via Discontinuity Mitigation

A via presents a short section of change in geometry to a trace and can appear as a capacitive and/or an inductive discontinuity. These discontinuities result in reflections and some degradation of a signal as the signal travels through the via. Reduce the overall via stub length to minimize the negative impacts of vias (and associated via stubs).

Because longer via stubs resonate at lower frequencies and increase insertion loss, keep these stubs as short as possible. In most cases, the stub portion of the via present significantly more signal degradation than the signal portion of the via. TI recommends keeping via stubs to less than 15 mils. Longer stubs must be back-drilled. For examples of short and long via lengths, see Figure 4-5 and Figure 4-6.

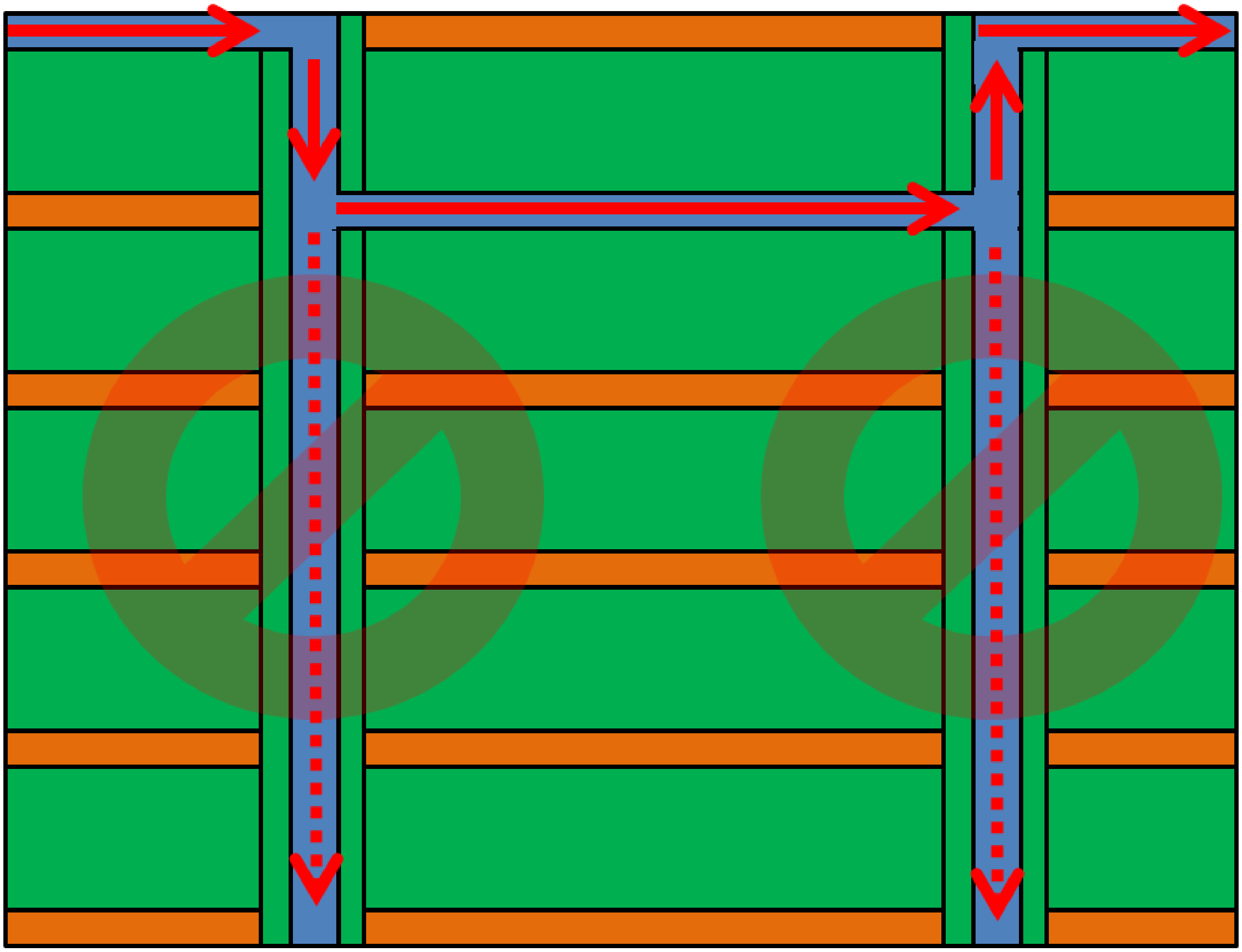

Figure 4-5. Vias With Long Stubs

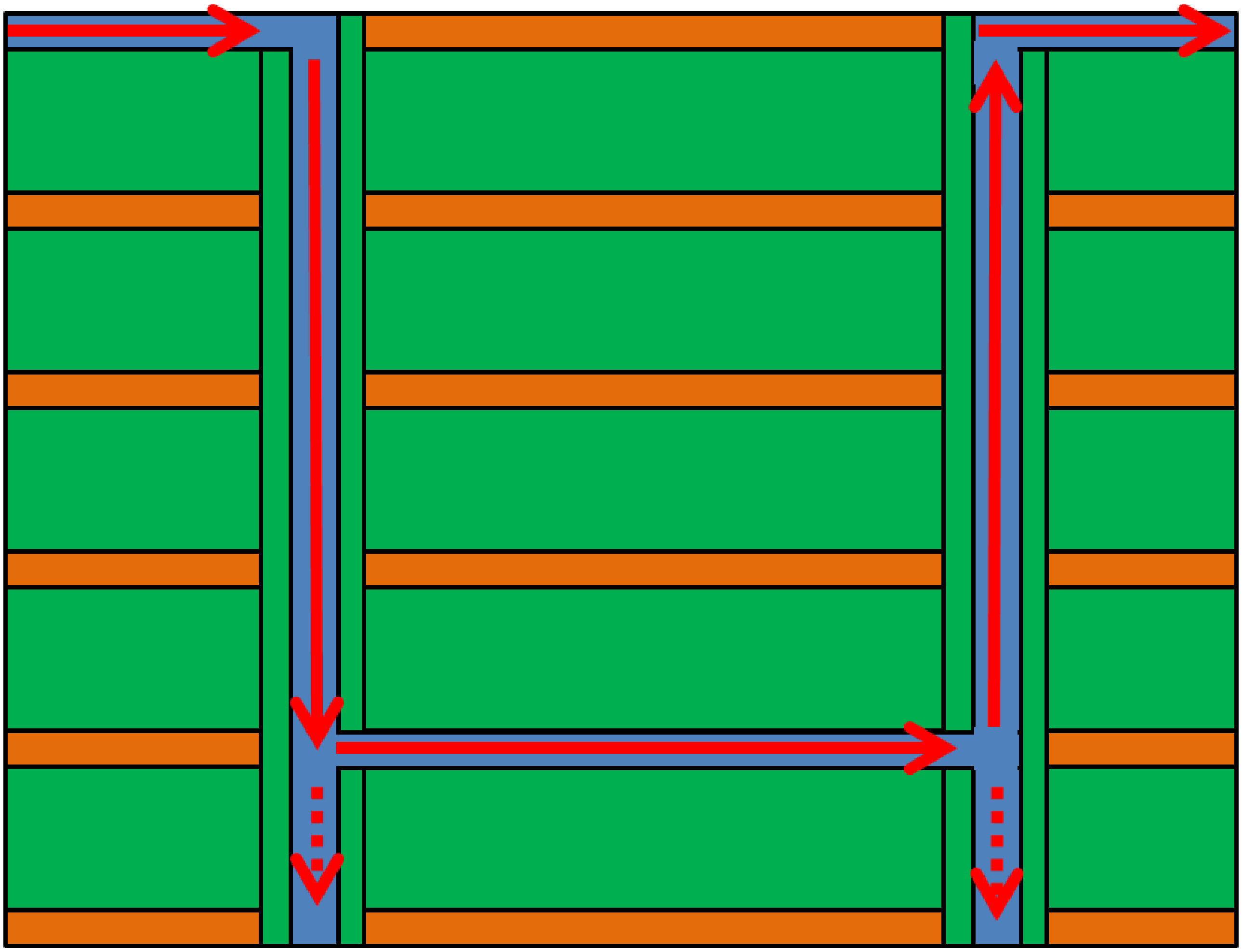

Figure 4-6. Vias With Short Stubs

4.6 Back-Drill Stubs

Back-drilling is a PCB manufacturing process in which the undesired conductive plating in the stub section of a via is removed. To back-drill, use a drill bit slightly larger in diameter than the drill bit used to create the original via hole. When via transitions result in stubs longer than 15 mils, back-drill the resulting stubs to reduce insertion losses and to verify that they do not resonate.

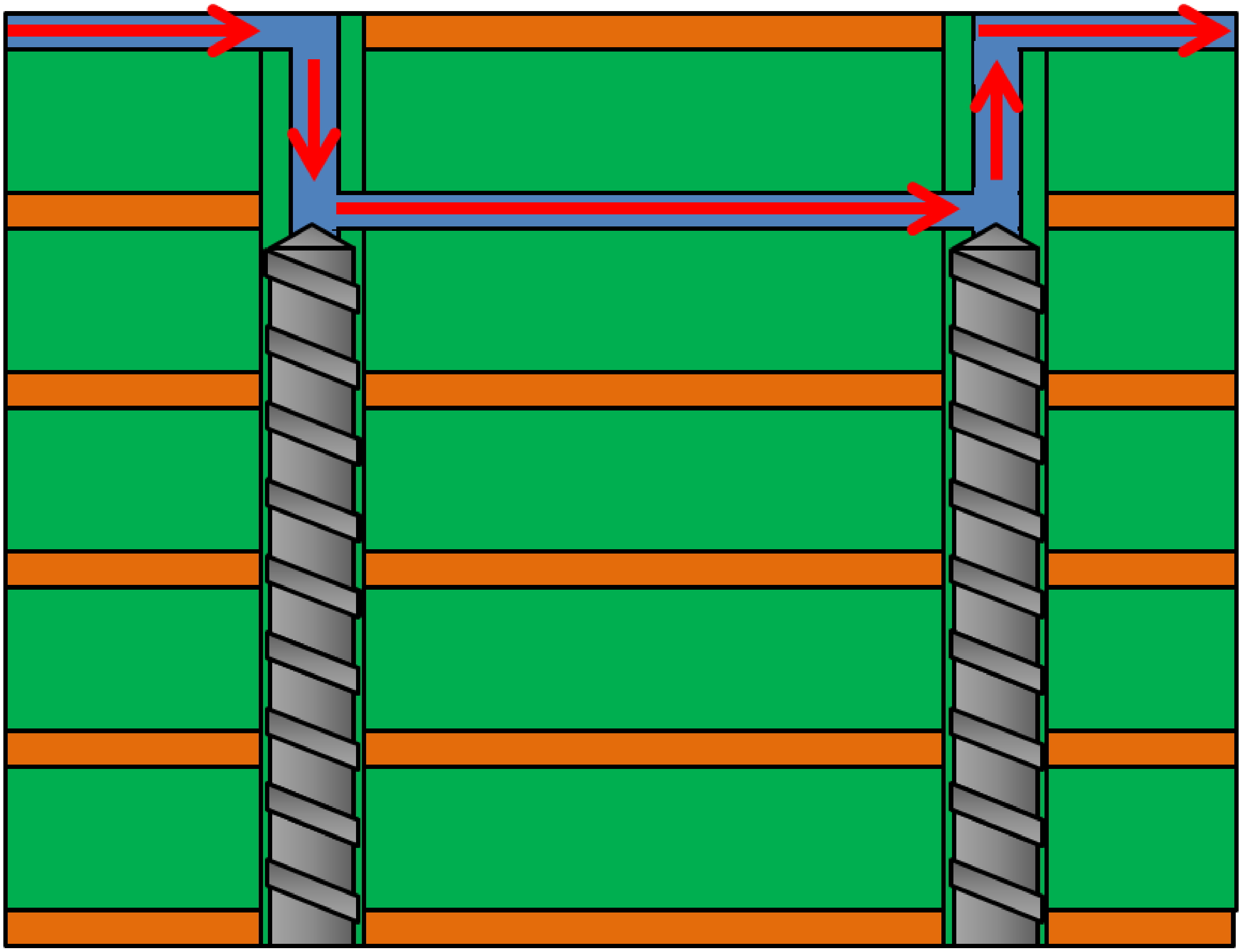

Figure 4-7. Long Vias With Back-Drilled Stubs

4.7 Trace Stubs

For high speed signals, minimize stubs on high speed traces to reduce increased insertion loss. Figure 4-8 depicts a high speed trace with a component on a stub. This stub can be reduced to:

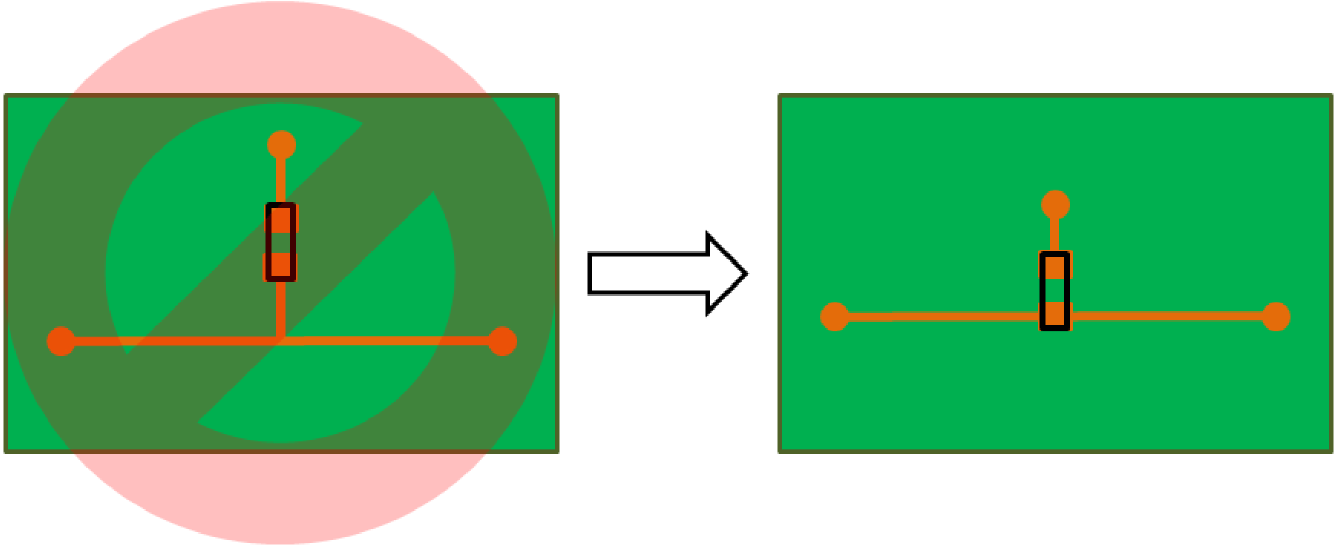

Figure 4-8. Reducing Stub Length

4.8 Increase Via Anti-Pad Diameter

Increasing the via anti-pad diameter reduces the capacitive effects of the via and the overall insertion loss. Verify that anti-pad diameter for vias on any high-speed signal are as large as possible (30 mils provides significant benefits without imposing undue implementation hardship). The copper clearance, indicated by this anti-pad, must be met on all layers where the via exists, including both routing layer and plane layers. The traces connecting to the via barrel contain the only copper allowed in this area; non-functional or unconnected via pads are not permitted. For an example of a via anti-pad diameter, see Figure 4-9.

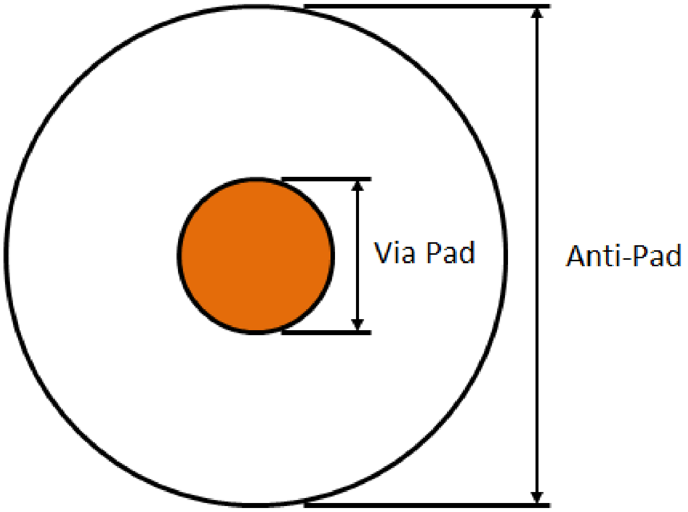

Figure 4-9. Via Anti-Pad

4.9 Equalize Via Count

If using vias is necessary on a high-speed differential signal trace, verify that the via count on each member of the differential pair is equal and that the vias are as equally spaced as possible. Make sure that the different lanes that lengths need to match have the same amount of vias on the lines. Also designers must take into account the length of the vias when verifying parameters such as inter pair skew.

4.10 Surface-Mount Device Pad Discontinuity Mitigation

Avoid including surface-mount devices (SMDs) on high-speed signal traces because these devices introduce discontinuities that can negatively affect signal quality. When SMDs are required on the signal traces (for example, the USB SuperSpeed transmit AC coupling capacitors) the maximum permitted component size is 0603. TI strongly recommends using 0402 or smaller. Place these components symmetrically during the layout process to maintain optimum signal quality and to minimize reflection. For examples of correct and incorrect AC coupling capacitor placement.

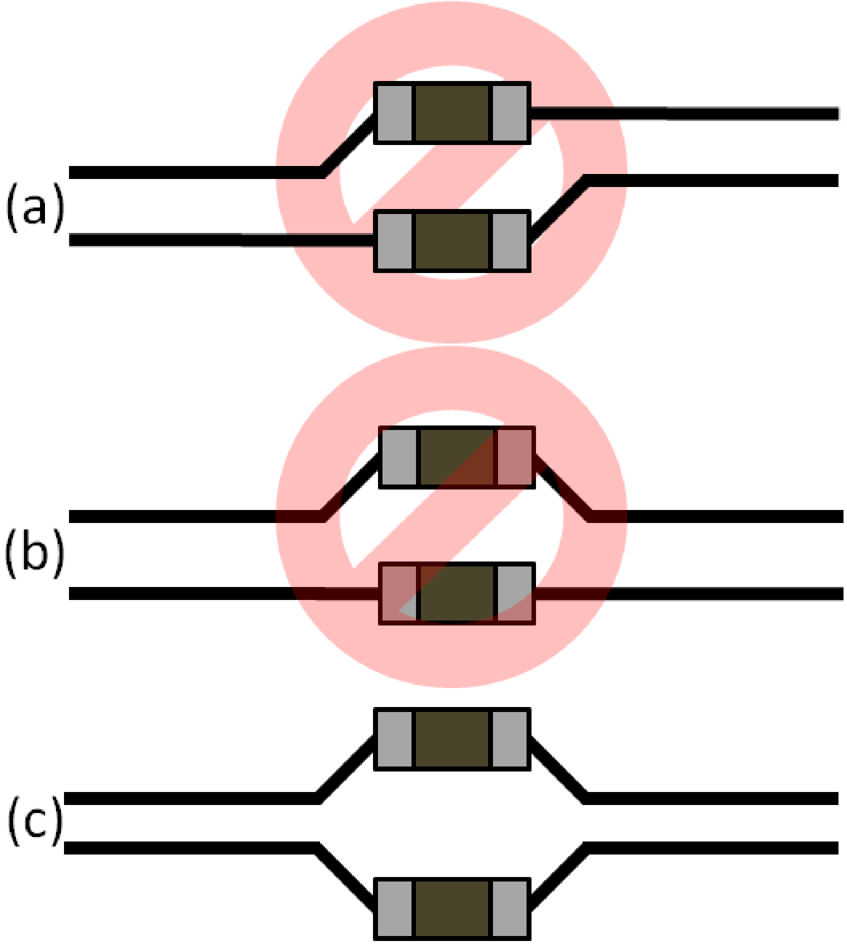

Figure 4-10. AC-Coupling Capacitor Placement

To minimize the discontinuities associated with the placement of these components on the differential signal traces, TI recommends voiding the SMD mounting pads of the reference plane by 100%. This void should be at least two PCB layers deep. For an example of a reference plane voiding of surface mount devices, see Figure 4-11.

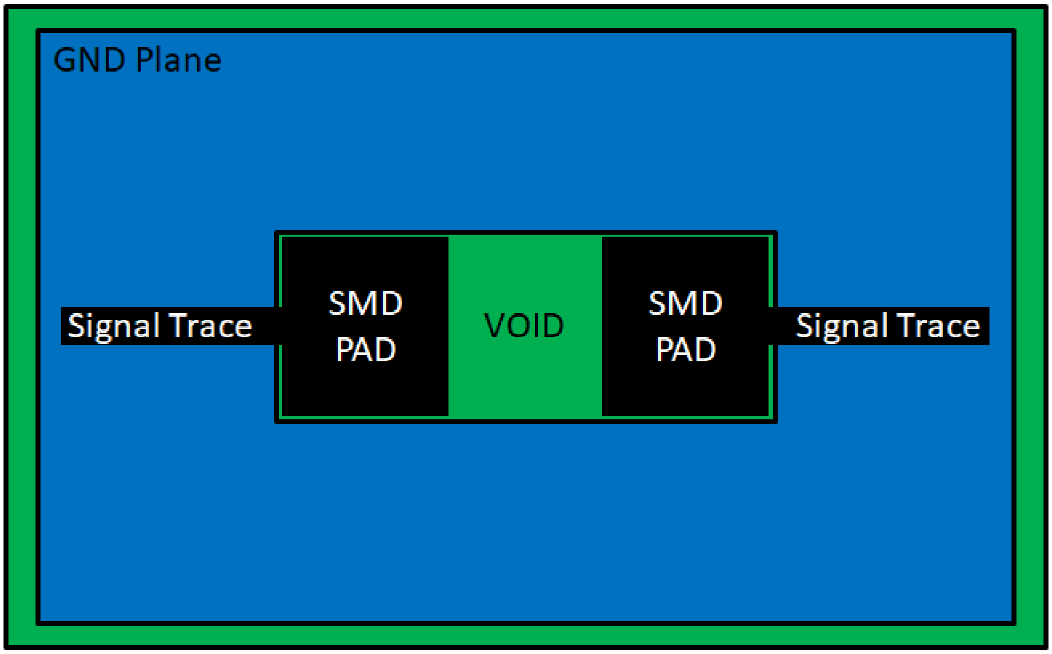

Figure 4-11. Void Below Surface Mount Devices

Also to minimize the inductance of the AC coupling capacitors use 0201 capacitor sizes.

4.11 Signal Bending

Avoid the introduction of bends into high-speed differential signals. When bending is required, maintain a bend angle greater than 135° to maintain that the bend is as loose as a possible. For an example of high-speed signal bending rules see Figure 4-12.

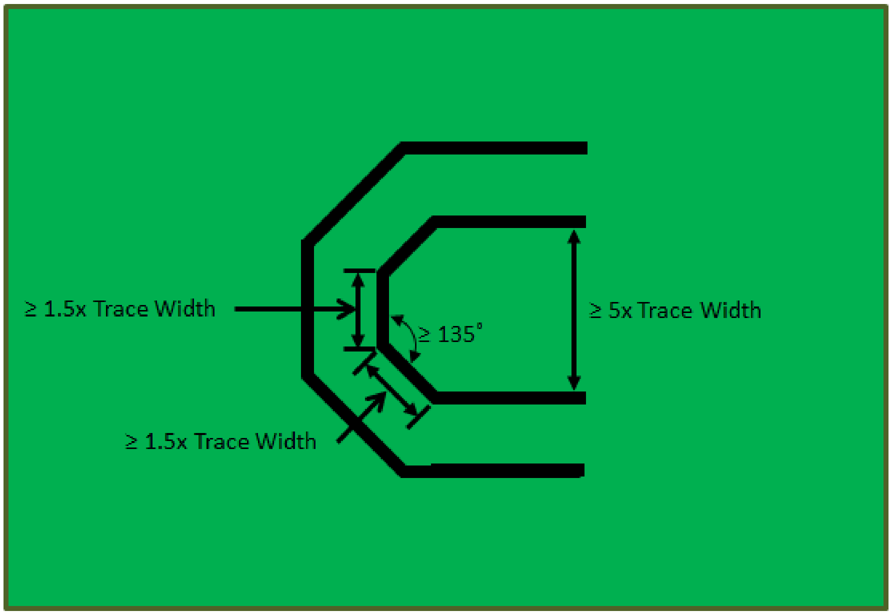

Figure 4-12. Signal Bending Rules

4.12 Suggested PCB Stackups

TI recommends a PCB of at least six layers for PCBs with high speed signals. Table 4-1 provides example PCB stackups.

Table 4-1. Possible Board Stack-up on a Six-Layer PCB

	Model 1	Model 2	Model 3	Model 4	Model 5	Model 6	Model 7
Layer 1	SIGNAL	SIGNAL	SIGNAL	GROUND	SIGNAL	SIGNAL	SIGNAL
Layer 2	GROUND	SIGNAL	GROUND	SIGNAL	GROUND	GROUND	GROUND
Layer3	SIGNAL	POWER	POWER	SIGNAL	POWER	POWER	POWER
Layer 4	SIGNAL	GROUND	SIGNAL	SIGNAL	SIGNAL	GROUND	GROUND
Layer 5	POWER	SIGNAL	GROUND	POWER	GROUND	NOT USED	SIGNAL
Layer 6	SIGNAL	SIGNAL	SIGNAL	GROUND	SIGNAL	SIGNAL	SIGNAL
Decoupling	Good	Good	Good	Good	Good	Good	Good
EMC	Satisfactory	Bad	Good	Satisfactory	Satisfactory	Good	Good
Signal Integrity		Bad	Good	Bad	Good	Good	Bad

If four layer PCBs are required, Table 4-2 provides example PCB stackups.

Table 4-2. Possible Board Stack-up on a Four-Layer PCB

	Model 1	Model 2	Model 3	Model 4
Layer 1	SIGNAL	SIGNAL	SIGNAL	GROUND
Layer 2	SIGNAL	GROUND	GROUND	SIGNAL
Layer 3	POWER	POWER	SIGNAL	POWER
Layer 4	GROUND	SIGNAL	POWER	SIGNAL
Decoupling	Good	Good	Bad	Bad
EMC	Bad	Bad	Bad	Bad
Signal Integrity	Bad	Bad	Good	Bad

For more than 6 PCB Layers Stack-ups use the following examples.

Table 4-3. Example PCB Stack-ups

8-LAYER	10-LAYER
SIGNAL	SIGNAL
GROUND	GROUND
SIGNAL	SIGNAL
SIGNAL	SIGNAL
POWER/GROUND	POWER
SIGNAL	SIGNAL
GROUND	SIGNAL
SIGNAL	SIGNAL
	GROUND
	SIGNAL

4.13 ESD/EMI Considerations

When choosing ESD/EMI components, TI recommends selecting devices that permit flow-through routing of the USB differential signal pair because they provide the cleanest routing. For example, the TI TPD4EUSB30 can be combined with the TI TPD2EUSB30 to provide flow-through ESD protection for both USB2 and USB3 differential signals without the need for bends in the signal pairs.

4.14 ESD/EMI Layout Rules

- Place ESD and EMI protection devices as close as possible to the connector.
- Keep any unprotected traces away from protected traces to minimize EMI coupling.
- Incorporate 60% voids under the ESD/EMI component signal pads to reduce losses.
- Use 0402 0Ω resistors for common-mode filter (CMF) no-stuff options because larger components typically introduce more loss than the CMF.
- Place any required signal pair AC coupling capacitors on the protected side of the CMF and as close as possible to the CMF.
- If vias are needed to transition to the CMF layer, verify that the vias are as close as possible to the CMF.
- Keep the overall routing of AC coupling capacitors + CMF + ESD protection as short and as close as possible to the connector.

5 References

- Hall, Stephen H., and Garrett W. Hall. *High Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices*. New York: Wiley, 2000.
- Johnson, Howard W., and Martin Graham. *High-speed Signal Propagation: Advanced Black Magic*. Upper Saddle River, NJ: Prentice Hall/PTR, 2003
- Hall, Stephen H., and Howard L. Heck. *Advanced Signal Integrity for High-speed Digital Designs.* Hoboken, N.J.: Wiley , 2009.
- Texas Instruments, *High-Speed Interface Layout Guidelines* application note
- Texas Instruments, *High-Speed Layout Guidelines* application report

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