Application Report
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TDP142 Schematic Checklist

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ABSTRACT

This schematic checklist provides a brief explanation of each TDP142 device pin, and the recommended configuration of TDP142 device pins for default operation. The TDP142 is a DisplayPort™ (DP) linear redriver that is able to snoop AUX and HPD signals. The device complies with the VESA DisplayPort standard Version 1.4, and supports a 1-4 lane Main Link interface signaling up to HBR3 (8.1 Gbps per lane). Additionally, this device is position independent. It can be placed inside source, cable, or sink, effectively providing a "negative loss" component to the overall link budget. The TDP142 has the ability to be configured via GPIO or I2C.

This document is intended to aid design at the system level for general applications, but must not be the only resource used. In addition to this list, use the information in the *TDP142 DisplayPort™ 8.1 Gbps Linear Redriver* , *TDP142EVM User's Guide*, and associated documents to gain a full understanding of device functionality.

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PIN NAME	PIN NUMBER(S)	PIN DESCRIPTION	RECOMMENDATION	ADDITIONAL PIN CONSIDERATIONS
Main Link Input Pins				
INDP[0:3]p/n	9,10,12,13,15, 16,18,19	DP main link differential input	AC-coupled connection from GPU to the TDP142	In the case of the DP connector connected to the TDP142 input, the AC-coupling cap may already be populated on the GPU side. If so, then the TDP142 input may be DC-coupled. If the TDP142 input is still AC-coupled, please make sure the total capacitance does not violate the DP specification.
Main Link Output Pins				
OUTDP[0:3]p/n	40,39,37,36,33 ,34,30,31	DP main link differential output	75 nF to 200 nF AC-coupled connection from the TDP142 to the sink or the connector	
HOT PLUG DETECT PINS				
HPDIN/RSVD9	32	Hot plug detect input from sink side / Reserved	When I2C_EN = 0, connect to the HPD output of the display or connector. For snoop mode: Connect directly to the directly connected HPD line of the sink or GPU (Check GPU supported voltage).	When I2C_EN = 1, HPDIN/RSVP9 is RSVD9, which can be left as No Connect.
AUXILIARY				
AUXp	24	Source side bidirectional DisplayPort auxiliary bus	For source: AUXP must have a 100 kΩ pull-down resistor on the TDP142 side of the 100 nF capacitors. For sink: AUXP must be a 1 MΩ pull-up resistor on the TDP142 side of the 100 nF capacitors. For cable: AUXP directly connected to AUX bus between the source and the sink.	
AUXn	25	Source side bidirectional DisplayPort auxiliary bus	For source: AUXN must have a 100 kΩ pull-up resistor on the TDP142 side of the 100 nF capacitors. For sink: AUXN must be 1 MΩ pull-down resistor on the TDP142 side of the 100 nF capacitors For cable: AUXN directly connected to AUX bus between the source and the sink..	
CONTROL PINS				
DPEQ1	2	DisplayPort receiver EQ control	When I2C_EN = 0, Tie 1 kΩ or directly to GND for a level ‘0’. Tie 20 kΩ to GND for a level ‘R’ No connect for level ‘F’ Tie 1 kΩ or directly to VCC for level ‘1’	When I2C_EN = 1, leave it unconnected
DPEN/HPDIN	23	Input receive equalization	When I2C_EN = 0, pull down with 10 kΩ to disable DisplayPort. Pull up with 10 kΩ to enable DisplayPort.	When I2C_EN = 1, connect to the HPD output of the display or connector.. For snoop mode: Connect directly to the directly connected HPD line of the sink or GPU (Check CPU supported voltage)
TEST1/SCL	21	Test pin/I2C clock signal	When I2C_EN = 0, pull down with 10 k or directly to GND	When I2C_EN = 1, 2k pull-ups or value required by I2C master to the VCC I2C supply of the I2C master.
TEST2/SDA	22	Test pin/I2C data signal	When I2C_EN = 0, pull down with 10 k or directly to GND	When I2C_EN = 1, 2k pull-ups or value required by I2C master to the VCC I2C supply of the I2C master.

PIN NAME	PIN NUMBER(S)	PIN DESCRIPTION	RECOMMENDATION	ADDITIONAL PIN CONSIDERATIONS
I2C_EN	17	I2C control mode	Tie 1kΩ or directly to GND for GPIO mode Tie 20kΩ to GND for TI Test Mode No connect for I2C enabled at 1.8V Tie 1kΩ or directly to VCC for I2C enabled at 3.3V	
A0	11	I2C address pin 0	When I2C_EN = 0, leave it unconnected	When I2C_EN = 1, 1 kΩ Pull-up resistor to 3.3 V and 1 kΩ pull-down resistor to GND set the TDP142 I2C address bit 0. If I2C_EN = “F”, then this pin must be set to “F” or “0”.
DPEQ0/A1	14	DisplayPort receiver EQ control/I2C address pin 1	When I2C_EN = 0, Tie 1kΩ or directly to GND for a level ‘0’ Tie 20kΩ to GND for a level ‘R’ No connect for level ‘F’ Tie 1kΩ or directly to VCC for level ‘1’	When I2C_EN = 1, 1 kΩ Pull-up resistor to 3.3 V and 1 kΩ pull-down resistor to GND set the TDP142 I2C address bit 1. If I2C_EN = “F”, then this pin must be set to “F” or “0”.
SNOOPENZ/RSVD8	29	AUX Snoop/Reserved	When I2C_EN = 0, pull down with 10 kΩ to enable AUX snoop. Pull up with 10 kΩ to enable AUX snoop.	When I2C_EN = 1, SNOOPENZ/RSVD8 is RSVD8 which can be left as No Connect
RSVD1,2,3,4,5,6,7,10,11	3,4,5,7,8,26,27,35,38	Reserved	No connect	
POWER PINS				
VCC	1,6,20,28	3.3-V power supply	One 100 nF cap for each power pin. One bulky 4.7 uF or greater bulk capacitor for VCC	
Thermal Pad	GND	Ground	Connect to board ground	

2 References

- *TDP142 DisplayPort 8.1 Gbps Linear Redriver*
- *TDP142EVM User's Guide*

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