*Application Report*

# *ISO7710/ISO7710-Q1 Functional Safety FIT Rate, FMD and Pin FMA*

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## Table of Contents



## Trademarks

# 1 Overview

This document contains information for ISO7710/ISO7710-Q1 (8-D and 16-DW package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

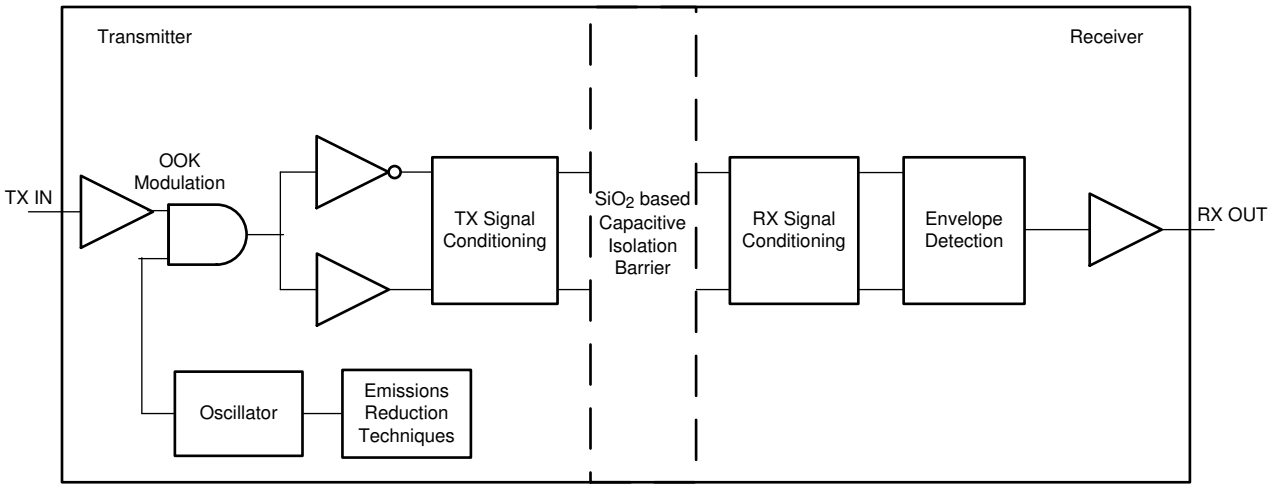


**Figure 1-1. Functional Block Diagram**

ISO7710/ISO7710-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

# 2 Functional Safety Failure In Time (FIT) Rates

## 2.1 8-D (narrow body SOIC) Package

This section provides Functional Safety Failure In Time (FIT) rates for 8-D package of ISO7710/ISO7710-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

**Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

| FIT IEC TR 62380 / ISO 26262 | FIT (Failures Per $10^9$ Hours) |
|---|---|
| Total Component FIT Rate | 10 |
| Die FIT Rate | 3 |
| Package FIT Rate | 7 |

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 50 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2**

| Table | Category | Reference FIT Rate | Reference Virtual $T_J$ |
|---|---|---|---|
| 5 | CMOS, BICMOS<br>Digital, analog / mixed | 20 FIT | 55 °C |

The Reference FIT Rate and Reference Virtual $T_J$ (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

## 2.2 16-SOIC (wide-body SOIC) Package

This section provides Functional Safety Failure In Time (FIT) rates for the 16-SOIC package of ISO7710/ ISO7710-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

**Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

| FIT IEC TR 62380 / ISO 26262 | FIT (Failures Per $10^9$ Hours) |
|---|---|
| Total Component FIT Rate | 26 |
| Die FIT Rate | 2 |
| Package FIT Rate | 24 |

The failure rate and mission profile information in Table 2-3 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 50 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4

- EOS FIT rate assumed: 0 FIT

**Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2**

| Table | Category | Reference FIT Rate | Reference Virtual $T_J$ |
|---|---|---|---|
| 5 | CMOS, BICMOS<br>Digital, analog / mixed | 20 FIT | 55 °C |

The Reference FIT Rate and Reference Virtual $T_J$ (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

# 3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for ISO7710/ISO7710-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

**Table 3-1. Die Failure Modes and Distribution**

| Die Failure Modes | Failure Mode Distribution (%) |
|---|---|
| OUT state undetermined | 40% |
| OUT not in voltage or timing specification | 30% |
| OUT stuck to default state | 24% |
| OUT stuck high | 3% |
| OUT stuck low | 3% |

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

# 4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the ISO7710/ISO7710-Q1 (8-D and 16-SOIC package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2 and Table 4-6)
- Pin open-circuited (see Table 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin ( see Table 4-4 and Table 4-8)
- Pin short-circuited to supply ( see Table 4-5 and Table 4-9)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1. Note that when pin short to ground case is discussed, only same side ground shorts are considered.

**Table 4-1. TI Classification of Failure Effects**

| Class | Failure Effects |
|---|---|
| A | Potential device damage that affects functionality |
| B | No device damage, but loss of functionality |
| C | No device damage, but performance degradation |
| D | No device damage, no impact to functionality or performance |

## 4.1 8-D (narrow-body SOIC) Package

Figure 4-1 shows the ISO7710/ISO7710-Q1 pin diagram for the 8-D package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the ISO7710/ISO7710-Q1 data sheet.

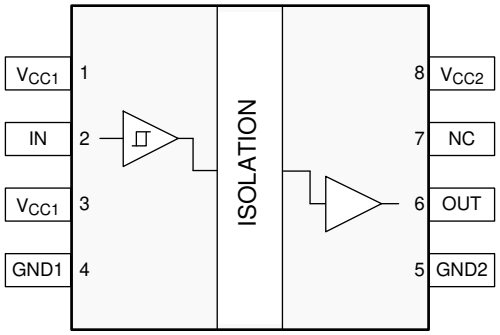


**Figure 4-1. Pin Diagram (8-D) Package**

**Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| $V_{CC1}$ | 1 | With pin3 getting supply from PCB, device damage is possible if high current from pin3 Vcc1 enters the device due to potential difference between pin1 and pin3. | A |
| IN | 2 | Input signal shorted to ground, so output (OUT) stuck to low. Communication from IN to OUT corrupted. | B |
| $V_{CC1}$ | 3 | With pin1 getting supply from PCB, device damage is possible if high current from pin1 Vcc1 enters the device due to potential difference between pin1 and pin3. | A |
| GND1 | 4 | Device continues to function as expected. Normal operation | D |
| GND2 | 5 | Device continues to function as expected. Normal operation | D |
| OUT | 6 | OUT stuck low. Data communication from IN to OUT lost. Device damage possible if IN is driven high for extended period of time. | A |
| NC | 7 | Device continues to function as expected. Normal operation. | D |
| $V_{CC2}$ | 8 | No power to the device on side-2. OUT pin state undetermined. | B |

**Table 4-3. Pin FMA for Device Pins Open-Circuited**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| $V_{CC1}$ | 1 | Device remains powered through pin3. | D |
| IN | 2 | No communication to device possible. OUT stuck to default state (High for ISO7710-Q1 and Low for ISO7710F-Q1). | B |
| $V_{CC1}$ | 3 | Device remains powered through pin1. | D |
| GND1 | 4 | Device unpowered on side-1. OUT goes to default state(High for ISO7710-Q1 and Low for ISO7710F-Q1) | B |
| GND2 | 5 | Device unpowered on side-2. OUT state undetermined. | B |
| OUT | 6 | State of OUT undetermined. No data communication possible. | B |
| NC | 7 | Device continues to function as expected. Normal operation. | D |
| $V_{CC2}$ | 8 | Device unpowered and state of OUT undetermined. | B |

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

| Pin Name | Pin No. | Shorted to | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|---|
| $V_{CC1}$ | 1 | IN | IN stuck high. External bit-stream for communication to IN pin corrupted. | B |
| IN | 2 | $V_{CC1}$ | IN stuck high. External bit-stream for communication to IN pin corrupted. | B |
| $V_{CC1}$ | 3 | GND1 | Device supply shorted to ground in side-1. Device damage is possible if high current from pin1 Vcc1 enters the device due to potential difference between pin1 and pin3. | A |
| GND1 | 4 | $V_{CC1}$ | Already considered in above row. | A |
| GND2 | 5 | OUT | OUT pin stuck low. Communication corrupted. If IN pin is driven high for extended duration, OUT pin stuck low creates a short between supply and ground with possible device damage. | A |
| OUT | 6 | NC | Device continues to function as expected. Normal operation. | D |
| NC | 7 | $V_{CC2}$ | Device continues to function as expected. Normal operation. | D |
| $V_{CC2}$ | 8 | NC | Already considered in above row. | D |

**Table 4-5. Pin FMA for Device Pins Short-Circuited to supply**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| $V_{CC1}$ | 1 | No effect. Normal operation. | D |
| IN | 2 | IN pin stuck high. Communication corrupted. | B |
| $V_{CC1}$ | 3 | No effect. Normal operation. | D |
| GND1 | 4 | Device side-1 unpowered. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible. | A |
| GND2 | 5 | Device side-2 unpowered. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible. | A |
| OUT | 6 | OUT stuck high. Communication disrupted. If IN is low for extended duration, OUT being stuck high creates a short and can damage the device. | A |
| NC | 7 | Device continues to function as expected. Normal operation. | D |
| $V_{CC2}$ | 8 | No effect. Normal operation. | D |

## 4.2 16-DW (wide-body SOIC) Package

Figure 4-2 shows the ISO7710/ISO7710-Q1 pin diagram for the 16-DW package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the ISO7710/ISO7710-Q1 data sheet.

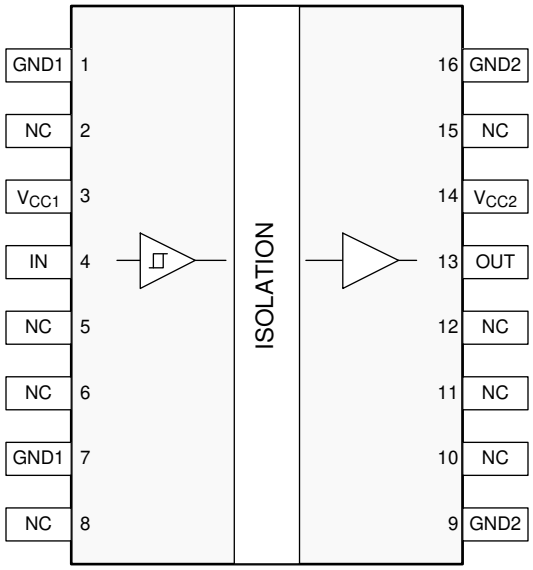


**Figure 4-2. Pin Diagram (16-DW Package)**

**Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| GND1 | 1 | Device continues to function as expected. Normal operation. | D |
| NC | 2 | Device continues to function as expected. Normal operation. | D |
| $V_{CC1}$ | 3 | No power to the device on side-1. Observe that the absolute maximum ratings for all pins of the device are met; otherwise device damage may be plausible. | A |
| IN | 4 | Input signal shorted to ground, so output (OUT) stuck to low. Communication from IN to OUT corrupted. | B |
| NC | 5 | Device continues to function as expected. Normal operation. | D |
| NC | 6 | Device continues to function as expected. Normal operation. | D |
| GND1 | 7 | Device continues to function as expected. Normal operation. | D |
| NC | 8 | Device continues to function as expected. Normal operation. | D |
| GND2 | 9 | Device continues to function as expected. Normal operation. | D |
| NC | 10 | Device continues to function as expected. Normal operation. | D |
| NC | 11 | Device continues to function as expected. Normal operation. | D |
| NC | 12 | Device continues to function as expected. Normal operation. | D |
| OUT | 13 | OUT stuck low. Data communication from IN to OUT lost. Device damage possible if IN is driven high for extended period of time. | A |
| $V_{CC2}$ | 14 | No power to the device on side-2. OUT pin state undetermined. | B |
| NC | 15 | Device continues to function as expected. Normal operation. | D |
| GND2 | 16 | Device continues to function as expected. Normal operation. | D |

**Table 4-7. Pin FMA for Device Pins Open-Circuited**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| GND1 | 1 | Device gets return ground through pin7. Normal operation. | D |
| NC | 2 | Device continues to function as expected. Normal operation. | D |
| $V_{CC1}$ | 3 | Operation undetermined. Either device is unpowered and OUT=default logic state or through internal ESD diode on IN pin, device can power up if IN is driven to logic high. If IN has current sourcing capability to provide regular operating current of device, ESD diode conducts that current and device damage plausible. | A |

**Table 4-7. Pin FMA for Device Pins Open-Circuited (continued)**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| IN | 4 | No communication to device possible. OUT stuck to default state (High for ISO7710-Q1 and Low for ISO7710F-Q1). | B |
| NC | 5 | Device continues to function as expected. Normal operation. | D |
| NC | 6 | Device continues to function as expected. Normal operation. | D |
| GND1 | 7 | Device gets return ground through pin1. Normal operation. | D |
| NC | 8 | Device continues to function as expected. Normal operation. | D |
| GND2 | 9 | Device gets return ground through pin16. Normal operation. | D |
| NC | 10 | Device continues to function as expected. Normal operation. | D |
| NC | 11 | Device continues to function as expected. Normal operation. | D |
| NC | 12 | Device continues to function as expected. Normal operation. | D |
| OUT | 13 | State of OUT undetermined. No data communication possible. | B |
| $V_{CC2}$ | 14 | Device unpowered and state of OUT undetermined. | B |
| NC | 15 | Device continues to function as expected. Normal operation. | D |
| GND2 | 16 | Device gets return ground through pin9. Normal operation. | D |

**Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

| Pin Name | Pin No. | Shorted to | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|---|
| GND1 | 1 | NC | Device continues to function as expected. Normal operation. | D |
| NC | 2 | $V_{CC1}$ | Device continues to function as expected. Normal operation. | D |
| $V_{CC1}$ | 3 | IN | IN stuck high. External bit-stream for communication to IN pin corrupted. OUT state high. | B |
| IN | 4 | NC | Device continues to function as expected. Normal operation. | D |
| NC | 5 | NC | Device continues to function as expected. Normal operation. | D |
| NC | 6 | GND1 | Device continues to function as expected. Normal operation. | D |
| GND1 | 7 | NC | Device continues to function as expected. Normal operation. | D |
| NC | 8 | GND1 | Already considered above. | D |
| GND2 | 9 | NC | Device continues to function as expected. Normal operation. | D |
| NC | 10 | NC | Device continues to function as expected. Normal operation. | D |
| NC | 11 | NC | Device continues to function as expected. Normal operation. | D |
| NC | 12 | OUT | Device continues to function as expected. Normal operation. | D |
| OUT | 13 | $V_{CC2}$ | OUT stuck high. Communication disrupted. If IN is low for extended duration, OUT being stuck high creates a short and can damage the device. | A |
| $V_{CC2}$ | 14 | NC | Device continues to function as expected. Normal operation. | D |
| NC | 15 | GND2 | Device continues to function as expected. Normal operation. | D |
| GND2 | 16 | NC | Already considered above. | D |

**Table 4-9. Pin FMA for Device Pins Short-Circuited to supply**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| GND1 | 1 | This can create potential difference between pin1 and pin7, causing high current to flow in device and potential device damage. | A |
| NC | 2 | Device continues to function as expected. Normal operation. | D |
| $V_{CC1}$ | 3 | Device continues to function as expected. Normal operation. | D |
| IN | 4 | IN pin stuck high. Communication corrupted. Out state high. | B |
| NC | 5 | Device continues to function as expected. Normal operation. | D |
| NC | 6 | Device continues to function as expected. Normal operation. | D |

**Table 4-9. Pin FMA for Device Pins Short-Circuited to supply (continued)**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| GND1 | 7 | This can create potential difference between pin1 and pin7, causing high current to flow in device and potential device damage. | A |
| NC | 8 | Device continues to function as expected. Normal operation. | D |
| GND2 | 9 | This can create potential difference between pin9 and pin16, causing high current to flow in device and potential device damage. | A |
| NC | 10 | Device continues to function as expected. Normal operation. | D |
| NC | 11 | Device continues to function as expected. Normal operation. | D |
| NC | 12 | Device continues to function as expected. Normal operation. | D |
| OUT | 13 | OUT stuck high. Communication disrupted. If IN is low for extended duration, OUT being stuck high creates a short and can damage the device. | A |
| $V_{CC2}$ | 14 | Device continues to function as expected. Normal operation. | D |
| NC | 15 | Device continues to function as expected. Normal operation. | D |
| GND2 | 16 | This can create potential difference between pin9 and pin16, causing high current to flow in device and potential device damage. | A |

# 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| Month Year | * | Initial Release |

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