User's Guide

Selection Guide for MCF831x Devices

ABSTRACT

The MCF831x family of devices provide a single-chip, code-free sensorless FOC solution for customers driving BLDC motors for applications such as residential fans, ceiling fans, water pumps, vacuum cleaners, and so forth. This application note provides the hardware, register map and firmware algorithm feature comparison differences between the MCF8316A and MCF8315A devices.

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Trademarks

1 Introduction

MCF8316A is the first of integrated sensorless BLDC motor controller in its family with the version 'A' firmware algorithm features. The MCF8315A is similar to MCF8316A device with lesser current ratings and additional features in algorithm and bug errata fixes from version MCF8316A. This app note contains the detailed comparison between the MCF8316A and MCF8315A in terms of hardware, algorithm features firmware and register map changes. This application note helps customers to shift from MCF8316A to MCF8315A and it also helps customer as selection guide for choosing between MCF8316A and MCF8315A devices.

2 Comparison Among the MCF8316A and MCF8315A

2.1 Hardware Comparison

Table 2-1. Hardware Comparison

Sl No.	Hardware	MCF8316A	MCF8315A
1	Operating voltage	4.5 to 35 V	4.5 to 35 V
2	Package	40-Pin VQFN	40-Pin VQFN
3	Pin number 39	NC	Alarm pin
4	Pin number 36	NC	DACOUT 1
5	Pin number 37	NC	DACOUT 2
6	Peak output winding current	8 A	5 A
7	$R_{DS(ON),}$ (HS+LS) at 25°C	95 mΩ	240 mΩ

2.2 Algorithm Features Comparison

The additional algorithm features of MCF8315A over MCF8316A and improvements are tabulated in Table 2-2.

Table 2-2. Algorithm Features Comparison

Sl No.	Algorithm Firmware Feature	MCF8316A	MCF8315A	Remarks
1	Alarm pin functionality	Not available	Available	Additional feature
2	DACOUT 1 and DACOUT 2	Not available	Available	Additional feature
3	Current based brake option in motor startup sequence	Not available	Available	Additional feature
4	In torque mode, the current reference can be given through duty command input Torque mode option in analog and PWM speed input mode	Not available	Available	Additional feature
5	Active braking exit limit feature	Not available	Available	Additional feature
6	FG configuration in fault state	Not available	Available	Additional feature
7	FG configuration in idle state/motor stop	Not available	Available	Additional feature
8	DC bus voltage filter	Always Enable	Configurable	Additional feature
9	FG angle interpolation	Configurable	Always enable	Minimizes tuning effort
10	MTR_STOP_BRK_TIME	The minimum brake time options for less than 1 mS are not functional	Minimum brake time can be configured from 1 mS	Removed the brake time options for 0.1 mS, 0.25 mS, 0.5 Ms
12	Vdc filter	Always enabled	Configurable. Can be enabled or disabled	Additional feature
13	ABNORMAL_BEMF_THR	Configurable from 10% to 80%	Configurable from 40% to 70%	Improved BEMF fault detection

Table 2-2. Algorithm Features Comparison (continued)

Sl No.	Algorithm Firmware Feature	MCF8316A	MCF8315A	Remarks
14	Hardware lock detection current limit deglitch time	Configurable from 1 µS to 15 µS	Configurable from 1 µS to 7 µS	Improvement in feature
15	Duty Hysteresis	Not available	Hysteresis around the Minimum duty cycle input	Additional feature
16	PWM speed input from 95 kHz to 100 kHz	Errata	Functional	Improvement in feature
17	Continuous refresh with GUI does not work when motor is running	Errata	Functional	Functionality fix

2.3 EEPROM Register Map Comparison

Table 2-3. EEPROM Register Map Comparison

Sl No.	Register Field Name	MCF8316A	MCF8315A	Comments	Impact to MCF8316A customers moving to MCF8315A
1	Register: ISD_CONFIG Bit Field: BRK_CONFIG (Bit 20)	Reserved	Brake configuration 0h = Brake time is used to come out of Brake state 1h = Brake current threshold and Brake time is used to come out of Brake state	New feature using current based brake during ISD for faster braking during start-up; reserved bits should be set to 0b in MCF8316A	1. No impact if brake during ISD is not used 2. No impact if time-based brake during ISD is used 3. Same register settings as in MCF8316A can be used in MCF8315A if current based brake is not needed"
2	Register: ISD_CONFIG Bit Field: BRK_CURR_THR Bit 19:17	Reserved	Brake current threshold Configurable from 0.0625 A to 5 A		
3	Register: INT_ALGO_1 Bit Field: BRAKE_CURRENT_PERSIST Bit 16:15	Reserved	Persistence time for current below threshold during low side brake Configurable from 50 mS to 500 mS		
4	REV_DRV_OPEN_LOOP_CURRENT	1.5 A to 5 A	0.9375 A to 3.125A	Current scaled by 0.625 for MCF8315A	Bit setting should be changed to maintain same/ similar current limit when changing to MCF8315A
5	ACTIVE_BRAKE_CURRENT_LIMIT	0.5 A to 7 A	0.3125A to 4.375 A		
6	ALIGN_OR_SLOW_CURRENT_ILIMIT	0.125 A to 8 A	0.0781 A to 5 A		
7	IPD_CURR_THR	0.25 A to 8 A	0.156 A to 5 A		
8	OL_ILIMIT	0.125 A to 8 A	0.0781 A to 5 A		
9	MPET_IPD_CURRENT_LIMIT	0.1 A to 2.0 A	0.0625 A to 1.25 A		
10	MPET_OPEN_LOOP_CURRENT_REF	1 A to 8 A	0.0625 A to 5 A		
11	CSA_GAIN	0 h = 0.15 V/A 1 h = 0.3 V/A 2 h = 0.6 V/A 3 h = 1.2 V/A	0 h = 0.24 V/A 1 h = 0.48 V/A 2 h = 0.96 V/A 3 h = 1.92 V/A		
12	ILIMIT: Reference for Torque PI Loop (A)	0.125 A to 8 A	0.0781 A to 5 A		
13	HW_LOCK_ILIMIT	0.125 A to 8 A	0.0781 A to 5 A		
14	LOCK_ILIMIT	0.125 A to 8 A	0.0781 A to 5 A		
15	BUS_CURRENT_LIMIT	0.125 A to 8 A	0.0781 A to 5 A		
16	NO_MTR_THR	0.05 A to 1 A	0.0312 A to 0.625 A		
17	Register: PIN_CONFIG Bit Field: VDC_FILT_DIS Bit: 27	Reserved Vdc filt is always enabled	Vdc filter disable 0 h = Enable 1 h = Disable	Additional feature	1. No impact 2. Use 0 h configuration to always enable Vdc filter

Table 2-3. EEPROM Register Map Comparison (continued)

SI No.	Register Field Name	MCF8316A	MCF8315A	Comments	Impact to MCF8316A customers moving to MCF8315A
18	Register: PIN_CONFIG Bit Field: FG_IDLE_CONFIG Bit 10:9	Not available	FG Configuration During Stop 0h = FG continues and end state not defined, provided FG_CONFIG (defining FG during coasting) 1 h = FG is pulled High 2 h = FG is pulled Low 3 h = FG is pulled High	Additional feature	1. No impact 2. Use 0 h configuration for backward compatibility
19	Register: PIN_CONFIG Bit Field: FG_FAULT_CONFIG Bit 8: 7	Not available	FG Configuration During Fault0h = Use last FG state when motor was driven 1 h = FG is pulled High 2 h = FG is pulled Low 3 h = FG active till BEMF drops below BEMF threshold defined by FG_BEMF_THR if FG_CONFIG set to 1b	Additional feature	1. No impact 2. Use 0 h configuration for backward compatibility
20	Register: PIN_CONFIG Bit Field: ALARM_PIN_EN Bit 6	Reserved Not available	Alarm Pin Enable 0 h = Disable 1 h = Enable	Additional feature	1. No impact 2. For 0 h configuration alarm pin will be disabled
21	Register: PERI_CONFIG1 Bit Field: ALARM_PIN_DIS Bit 8	Not functional	Reserved and replaced by ALARM_PIN_EN	Changed EPROM location of the bit	No impact
22	PIN_36_37_CONFIG	Reserved	Pin 36 and Pin 37 configuration 0 h = Pin 36 and Pin 37 are not defined as DAC pins 1 h = Pin 36 as DACOUT1 and PIN37 as DACOUT2	Additional feature	No impact
23	Register: INT_ALGO_1 Bit Field: ACTIVE_BRAKE_SPEED__DELTA_LIMIT_EXIT Bit 30:29	Not available (Bit no. 29 is used for FG_ANGLE_INTERPOLATE_E N Bit no. 30 is reserved)	Configurable from 2.5% to 10 %	Additional feature for configuring active braking exit limit	1. No impact if active braking is not used 2. Active braking exit limit configuration has to be chosen

Table 2-3. EEPROM Register Map Comparison (continued)

Sl No.	Register Field Name	MCF8316A	MCF8315A	Comments	Impact to MCF8316A customers moving to MCF8315A
24	ACTIVE_BRAKE_SPEED_DELTA_LIMIT	0 h = 2.5%	0 h = Reserved	Active braking entry limit shall be always grater than exit limit. Hence configuration for 2.5% is removed	1. Active braking speed entry limit configuration of 2.5% is removed 2. Minimum possible entry limit is 5%
25	OCP_LVL	0 h = OCP level is 16 A (Typical) 1 h = OCP level is 24 A (Typical)	0 h = OCP level is 9 A (Typical) 1 h = OCP level is 13 A (Typical)	OCP levels are different for MCF8316 and MCF8315	OCP levels are to be selected as per need
26	Register: INT_ALGO_1 Bit Field: FG_ANGLE_IN TERPOLATE_EN Bit 29	Configurable	Always Enabled This bit is used to specify the active braking exit speed limit	Minimizes tuning effort	1. No impact 2. This EPROM bit is used to select active braking exit limit
7	DAC_1 and DAC_2 registers	Not available	Available to configure DAC parameters	Additional feature	No impact
28	ABNORMAL_BEMF_THR	10% to 80%	40% to 70%	Changed bit enumeration values for better resolution	1. Use 011b in MCF8316A and tune if needed 2. No impact - use same value as in MCF8316A
29	HW_LOCK_ILIMIT_DEG	Configurable from 1 µS to 15 µS	Configurable from 1 µS to 7 µS	Additional bit in MCF8316A which was not applicable has been removed; set to 0100b in MCF8316A and 010b in MCF8315A for optimal performance	1. No impact - use bit setting 0100b for MCF8316A and leave unchanged for MCF8315A for optimal performance
30	Duty Hysteresis	Not available	Duty hysteresis for speed reference mode	New feature - added hysteresis for minimum duty cycle input	1. No impact 2. Hysteresis option at minimum duty cycle input threshold for MCF8315A
31	FIRST_CYCLE_FREQ_SEL	0 h = Defined by SLOW_FI RST_CYC_FREQ 1 h = 0 Hz	0 h = 0 Hz 1 h = Defined by SLOW_FIRST_CYC_FRE Q	Bit enumeration definitions switched in MCF8316A data sheet	No impact - use correct setting in MCF8316A tuning
32	MTR_STOP_BRK_TIME	0 h = 0.1 ms 1 h = 0.1 ms 2 h = 0.25 ms 3 h = 0.5 ms	0 h = 1 ms 1 h = 1 ms 2 h = 1 ms 3 h = 1 ms	Min possible brake time is 1ms; datasheet error in MCF8316A.	No impact since setting any value lower than 0100b in MCF8316A results in 1ms brake time only

Table 2-3. EEPROM Register Map Comparison (continued)

Sl No.	Register Field Name	MCF8316A	MCF8315A	Comments	Impact to MCF8316A customers moving to MCF8315A
33	WD timer fault	Not mentioned in data sheet	Available	Bit enumeration definitions not mentioned in MCF8316A datasheet	No impact

2.4 RAM Register Map Comparison

Table 2-4. RAM Register Map Comparison

Sl No.	Register Field Name	MCF8316A	MCF8315A
1	Register: CONTROLLER_FAULT_STATUS Bit Field: WATCHDOG_FAULT Bit 3	Reserved	Indicates Watchdog fault
2	Register: CONTROLLER_FAULT_STATUS Bit Field: STL_ENABLE_STATUS Bit 2	Reserved	STL Enable Status
3	Register: CONTROLLER_FAULT_STATUS Bit Field: STL_STATUS Bit 1	Reserved	STL Status
4	Register: CONTROLLER_FAULT_STATUS Bit Field: APP_RESET Bit 0	Reserved	App Reset
5	Register: ALGO_STATUS Register Bit Field: DUTY_CMD Bit 15:4	Reserved	12-bit value indicating decoded speed command in PWM/Analog mode DUTY_CMD (%) = DUTY_CMD/4096 * 100%
6	Register: ALGO_STATUS Register Bit Field: SYS_INIT_DONE Bit 3	Reserved	1 indicates device is ready for GUI control 0 indicates firmware is still copying EEPROM to shadow memory
7	Register: ALGO_STATUS Register Bit Field: SYS_ENABLE_FLAG Bit 2	Reserved	1 indicates GUI can control the register 0 indicates GUI is still copying default parameters from shadow memory
8	Register: ALGO_CTRL2 or ALGO_DEBUG2 Register Bit Field: FORCE_RECIRCULATE_STOP_SECTOR Bit 0	Reserved	Use to do the recirculation at specific sector during force motor stop condition
9	Register: DAC_1	Not available	DACOUT1 variable configuration register
10	Register: DAC_2	Not available	DACOUT1 variable configuration register

2.5 RAM Algorithm Variable Register Map Comparison

Table 2-5. RAM Algorithm Variable Register Map Comparison

Sl No.	Acronym	Register Name	MCF8316A Offset Address	MCF8315A Offset Address
1	ALGORITHM_STATE	Current Algorithm State Register	210h	190h
2	FG_SPEED_FDBK	FG Speed Feedback Register	246h	196h
3	BUS_CURRENT	Calculated DC Bus Current Register	410h	410h
4	PHASE_CURRENT_A	Measured Current on Phase A Register	43Eh	440h
5	PHASE_CURRENT_B	Measured Current on Phase B Register	440h	442h
6	PHASE_CURRENT_C	Measured Current on Phase C Register	442h	444h
7	CSA_GAIN_FEEDBACK	CSA Gain Register	466h	468h
8	VOLTAGE_GAIN_FEEDBACK	Voltage Gain Register	476h	472h
9	VM_VOLTAGE	VM Voltage Register	478h	474h
10	PHASE_VOLTAGE_VA	Phase A Voltage Register	47Eh	47Ah
11	PHASE_VOLTAGE_VA	Phase B Voltage Register	480h	47Ch
12	PHASE_VOLTAGE_VC	Phase C Voltage Register	482h	47Eh
13	SIN_COMMUTATION_ANGLE	Sine of Commutation Angle	4Bah	4B6h
14	COS_COMMUTATION_ANGLE	Cosine of Commutation Angle	4BCh	4B8h
15	IALPHA	IALPHA Current Register	4D4h	4D2h
16	IBETA	IALPHA Current Register	4D6h	4D4h
17	VALPHA	VALPHA Voltage Register	4D8h	4D6h
18	VBETA	VBETA Voltage Register	4DAh	4D8h
19	ID	Measured d-axis Current Register	4E4h	4E2h
20	IQ	Measured q-axis Current Register	4E6h	4E4h
21	VD	VD Voltage Register	4E8h	4E6h
22	VQ	VQ Voltage Register	4EAh	4E8h
23	IQ_REF_ROTOR_ALIGN	Align Current Reference	524h	524h
24	SPEED_REF_OPEN_LOOP	Open Loop Speed Register	53Ah	53Ch
25	IQ_REF_OPEN_LOOP	Open Loop Current Reference	548h	54Ch
26	SPEED_REF_CLOSED_LOOP	Speed Reference Register	5CCh	5D2h
27	ID_REF_CLOSED_LOOP	Reference for Current Loop Register	5FCh	604h

Table 2-5. RAM Algorithm Variable Register Map Comparison (continued)

Sl No.	Acronym	Register Name	MCF8316A Offset Address	MCF8315A Offset Address
28	IQ_REF_CLOSED_LOOP	Reference for Current Loop Register	5FEh	606h
29	ISD_STATE	ISD State Register	67Ah	680h
30	ISD_SPEED	ISD Speed Register	684h	68Ah
31	IPD_STATE	IPD State Register	6B8h	6BEh
32	IPD_ANGLE	Calculated IPD Angle Register	6FCh	702h
33	ED	Estimated BEMF EQ Register	742h	748h
34	EQ	Estimated BEMF ED Register	744h	74Ah
35	SPEED_FDBK	Speed Feedback Register	752h	758h
36	THETA_EST	Estimated rotor Position Register	756h	75Ch

3 References

- Texas Instruments: *MCF8316A Sensorless Field Oriented Control (FOC) Integrated FET BLDC Driver Data Sheet*
- Texas Instruments: *MCF8315A Sensorless Field Oriented Control (FOC) Integrated FET BLDC Driver Data Sheet*
- Texas Instruments: *MCF8316A Tuning User's Guide*
- Texas Instruments: *How to Design a Thermally-Efficient Integrated BLDC Motor Drive PCB*
- Texas Instruments: *BLDC Integrated MOSFET Thermal Calculator*

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