Application Note

TCAN284xx and TCAN285xx High Level Overview

Parker Dodson

ABSTRACT

The TCAN28xx families of devices (including TCAN285xx and TCAN284xx devices) are flexible mid-range system basis chips (SBCs) offered by TI. At the core, these devices include wired communication, power regulation, high side switches, protection features, and all tied together by a simple control system that can be facilitated by a controller through a 4-wire SPI bus. This document covers a high-level overview of these SBC families and their features that needs to act as a companion text to the devices' data sheets.

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1 Introduction

The TCAN28xx families of devices are a flexible line of mid-range system basis chips (SBCs) offered by TI. A mid-range SBC includes wired communication, power regulation, and high side switch(es) at a minimum – but this definition leaves a lot out of what the TCAN28xx devices are able to accomplish. The TCAN28xx families of devices include 2 main families – the TCAN284xx and the TCAN285xx lines of devices. These devices are all very similar with the differences easily decoded from the last three digits of the generic part number. If the device is TCAN284xx, the device supports standard CAN and CAN-FD while the TCAN285xx supports CAN-SIC. The second last to digit determines if the device supports LIN – devices with the pattern TCAN28x5x do not support LIN while devices with pattern TCAN28x7x do support LIN. Finally, the last digit determines the output voltage of the VCC1 LDO – devices with TCAN28xx3 have a 3.3V output on VCC1 while devices with TCAN28xx5 have a 5V output on VCC1.

This guide goes over a high-level view of what this device is capable of – and instead of fixating on small nuances this guide aims to give a high-level understanding of the devices features and why the features can be useful for a plethora of systems. This guide can start by going over the different device states that these SBCs employ and why. Next, a closer look at the power electronics integrated into the package. After power, the communication systems are examined. Following communications, the protection features can be explained. There is a brief overview of the programming, memory, and control of the SBC. Finally, miscellaneous features are discussed.

2 Device States

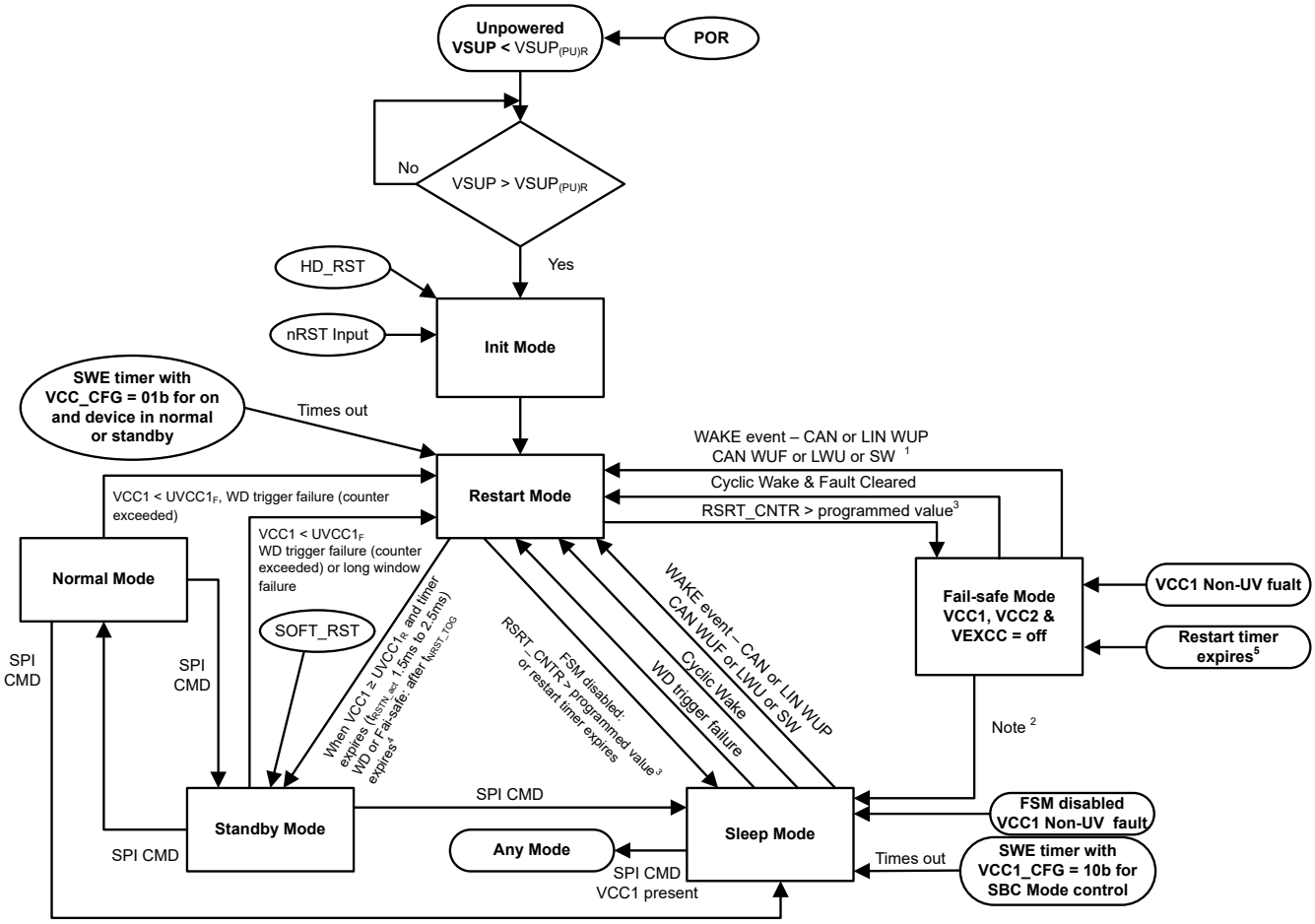

Figure 2-1. TCAN28xx State Diagram

The TCAN28xx devices all contain six different device states – two transitory states (init and restart), 3 standard operational states (standby, normal, and sleep) , and an optional fail-safe mode (fail-safe mode) for faults on SBC. The device states act as guardrails for features on the SBC as not all features are available in all modes. The SBC behavior is tied to which state the SBC is in and to properly design with this device all states and state transitions need to be understood. A brief overview of different subsystems and accessibility in each mode is shown in Table 2-1.

Table 2-1. SBC Block Overview by SBC Mode

Block	Restart	Sleep	Standby	Normal	Fail-Safe
nINT	High when VCC1 active	High if VCC1 on	Active	Active	Hi-Z
GFO	Programmed active state when VCC1 on	Programmed active state if VCC1 on	Active	Active	Hi-Z
SW	Off	Wake Capable/Off	Active	Active	Hi-Z
HSSx	Off	Off (default). HSS4 can be used for cyclic sensing wake, all other HSS pins can be configured for direct drive.	As Programmed	As Programmed	Off -HSS4 can be set up for cyclic sensing wake.
LIMP	Same as previous state, Low if leaving fail-safe mode or watchdog error	Previous state prior to sleep	Previous state prior to standby	Previous state prior to normal	Low
WAKEx	Off	As Programmed	As Programmed	Off	Active
CRXD	High	High if VCC1 on, Hi-Z otherwise	Configuration dependent	Configuration dependent	Hi-Z
LRXD	High	High if VCC1 on, Hi-Z otherwise	Configuration dependent	Configuration dependent	Hi-Z
nRST	Low	Low unless VCC1 on, then high	High	High	Off
SPI	Off	Active if VCC1 on	Active	Active	Off
Watchdog	Off	Off but can be programmed on if VCC1 on	Default on with long first pulse but programmable off	Active	Off
Low Power CAN RX	Default On for wake-capable	Default On for wake-capable	On if wake capable	On if wake capable	Default On for wake-capable
CAN transceiver	Off	Off	Programmable rx only	Programmable	Off
Low Power LIN RX	Default On for wake-capable	Default On for wake-capable	On if wake capable	On if wake capable	Default On for wake-capable
LIN Transceiver	Off	Off	Programmable rx only	Programmable	Off
LIN Bus Termination	Weak current pull-up	Weak current pull-up	35kΩ (typical)	35kΩ (typical)	Weak current pull-up
VCC1	Ramping	Off (default), programmable on	On	On	Off
VCC2	Ramping	Off (default), programmable on	On (default), programmable off	On (default), programmable off	Off
VEXCC	Ramping after initial configuration	Off (default); programmable on	Programmable	Programmable	Off

2.1 Init Mode

The first mode is a transitory mode, meaning that this operating state is transient and the SBC does not remain in this mode for long and can automatically transition out of this mode when operating conditions permit this to do so. The first state is the init mode – or initialization mode – which is used for the device to initialize. This mode is short lived and the operator, nor a controller, can do anything with SBC during this mode. Most subsystems are still off in the init mode with the exception of VCC1 and VCC2 which are turned on and ramping towards the regulated voltage targets (3.3V or 5V for VCC1 and 5V for VCC2)

There are four ways to enter this state and one way to exit. The most common way to enter init mode is to turn the power onto the device – as soon as the VSUP pin has reached appropriate power levels, VSUP_(PU)R, the device can enter init mode. A power on reset (POR) can also cause the device to become unpowered and reinitialize in init mode. A hard reset or an input signal placed on nRST can also cause the device to switch back to init mode, however in these two last cases the VSUP pin is already at an adequate voltage to begin initialization. The SBC can exit Init mode when VSUP crosses the UVSUP_R threshold and then enters into restart mode.

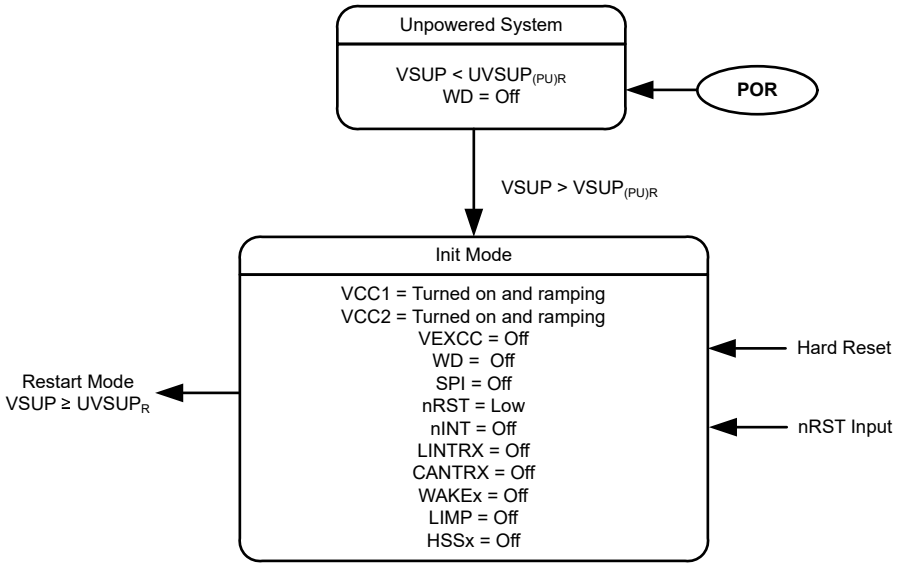

Figure 2-2. Init Mode

2.2 Restart Mode

The second mode is also transitory and is referred to as restart mode. This mode is used to finish initialization of SBC as well as acts as a landing state for selected faults. Most of the device is still in an off state during restart mode. All the voltage regulators are either on or ramping (depending on previous device state); LRXD and CRXD are held high, LIMP retains previous mode state, and the nRST pin is pulled low and depending on entry can either latch until mode change (during power up, wake, and undervoltage events) or pull low for a predefined time period then force a mode change to standby.

There are five different ways to enter into restart mode. The first is from Init mode – when VSUP has crossed the UVSUP_R threshold the device can transition to restart mode – for hard resets, POR, or power cycling this is the entry pathway. The next entrance is due to wake events while in either sleep or fail-safe mode, a wake event can transition the SBC into restart mode. The other three entryways into restart mode are from fault conditions. A UVCC1 event, which is an undervoltage event on VCC1, can cause the device to enter restart mode. If the watchdog timer failure counter exceeds the programmed threshold level, default is one failure, can cause the device to transition to restart mode. If VCC1 is enabled to be active in sleep mode a SWE timer expiration can cause the device to transition to restart mode.

There are three different ways to exit restart mode. If device is operating as expected without fault the device can transition to standby mode when VCC1 has crossed the UVCC1R threshold and sustains the voltage for t_RSTN_act signals to the SBC that VCC1 is at a ready an active state. The other two exit paths are due to fault conditions. Every time the device enters restart mode a restart counter is incremented and there is a programmable threshold for how many times device can restart before an error is flagged and the device can transition to fail-safe mode if enabled and sleep mode otherwise. By default, the reset counter can experience an overflow on the 5**th** device reset but this value can be changed to be larger or smaller. The other exit path is if the restart timer has elapsed and VCC1 never met the transition condition – in this case the device can transition to fail-safe mode if enabled and sleep mode otherwise.

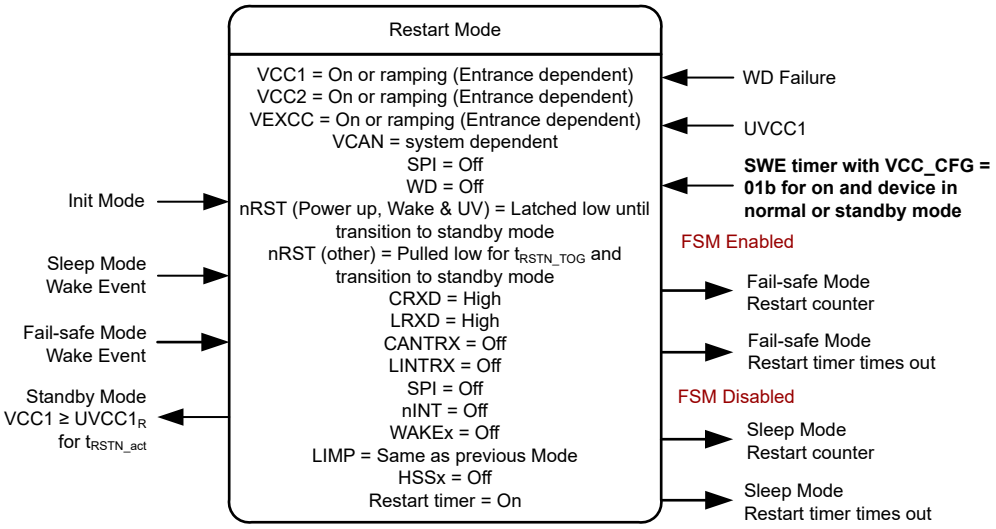

Figure 2-3. Restart Mode

2.3 Standby Mode

Standby mode is the first operational mode where the controller can interact with the SBC. Most features are accessible in this mode except transmission from wired transceivers. Standby mode is where most of the configuration of the device takes place as this is the first mode in which the SPI bus becomes active. Upon entry into standby mode a long window watchdog timer starts and must be triggered through the SPI bus or else the device can transition back to reset mode – this can be avoided during prototyping by holding the SW pin in the active state (by default the active state is high).

There are three different ways to enter into the standby mode. The first way is the transition from restart mode to standby when VCC1 has surpassed the UVCC1_R threshold and remained over the threshold for t_RSTN_act. If the SPI bus is active a SPI command can always be used to transition device back into standby mode – this is applicable for when device is in normal mode or sleep mode (if VCC1 is active in sleep, which by default is not). A soft reset can also cause the device to return to standby mode – but soft resets also require the SPI bus to be active.

There are multiple ways to leave standby mode – but the ways can be categorized in two groups: SPI command or fault condition. If everything is working as intended to leave standby mode a SPI command needs to be initiated and can lead the device into normal mode or sleep mode depending on specific command issued. The other exit path from standby is due to a fault condition – which depending on fault type and device configuration can result in the device entering restart mode, sleep mode, or fail-safe mode.

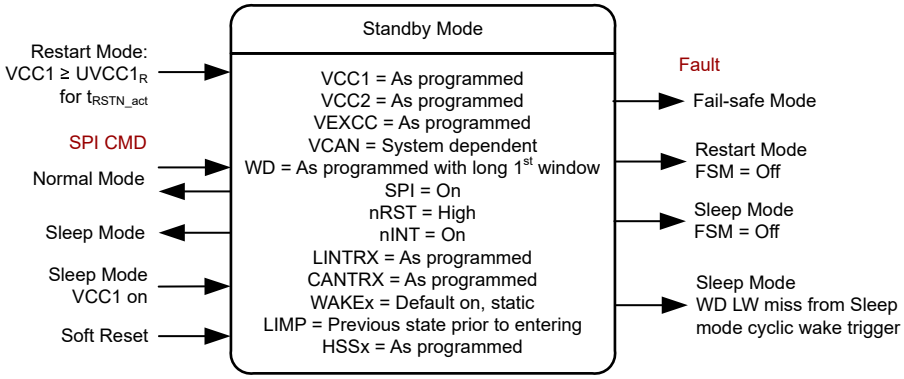

Figure 2-4. Standby Mode

2.4 Normal Mode

Normal mode is the main operational mode of the SBC as this in this mode all power electronics and transceivers are able to operate as intended. How the device operates in normal mode is dependent on direct configuration of device – but all standard features are accessible.

There is only one way to enter normal mode and two broad categories of exit conditions. To enter normal mode a SPI command needs to be sent while the SBC is in standby mode or sleep mode if VCC1 is on during sleep. To exit normal mode either a SPI command needs to be sent by the controller or a fault condition must occur. Depending on exact fault condition and device configuration a fault can cause the device to either enter restart mode, sleep mode, or fail-safe mode.

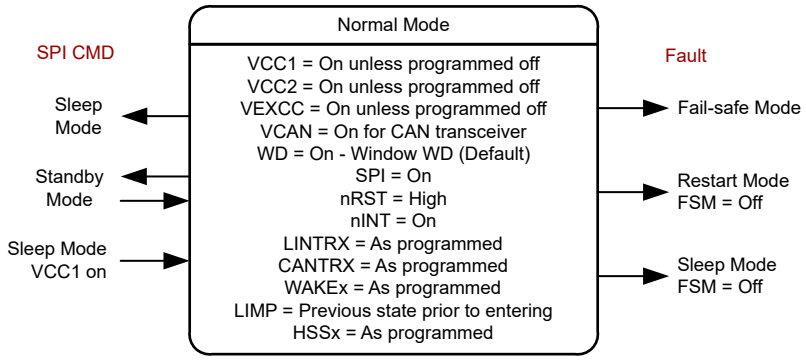

Figure 2-5. Normal Mode

2.5 Sleep Mode

Sleep mode is another common operational mode and is the power saving mode of the device. In sleep mode the transceivers can be set to wake-capable, watch dog timer can be set to timeout (default state is off), power regulation is off but can be set to be on, SPI is off unless VCC1 is set to on, and the HSS act as programmed. Before the device enters sleep, mode there must be one method of wake-up available or else the device does not transition to sleep mode and an interrupt can be set.

There are seven different ways to enter sleep mode across two general categories: SPI command and fault condition. The only standard, without fault, way to enter sleep mode is through a SPI command that can transition device from standby, normal, or fail-safe mode (if enabled). The other six ways to enter sleep mode are various fault conditions. If VCC1 is off during sleep mode (default) a SWE timer timeout can transition to the device to sleep mode. Another way for the device to enter sleep is if the restart timer timeouts during restart mode which can cause the SBC to enter sleep mode. The other four entrances can only happen if fail-safe mode is disabled – these are thermal shutdown on VCC1, overvoltage on VCC1 (OVCC1), short circuit on VCC1 (VCC1_SC), or a restart counter overflow – if fail-safe mode is enabled these faults can cause a transition to fail-safe instead.

There are four generalized ways to exit sleep mode depending on device configuration. The only universal way to exit sleep mode regardless of configuration is a device wake event which can cause the device to transition to restart mode. If VCC1 is on during sleep mode there are 3 other exits possible. The first of these is a SPI command to transition the device out of sleep mode to either standby or normal mode. A UVCC1 can cause the device to transition to restart mode. If watchdog is enabled during sleep mode a watchdog error counter overflow can cause a device transition to restart mode.

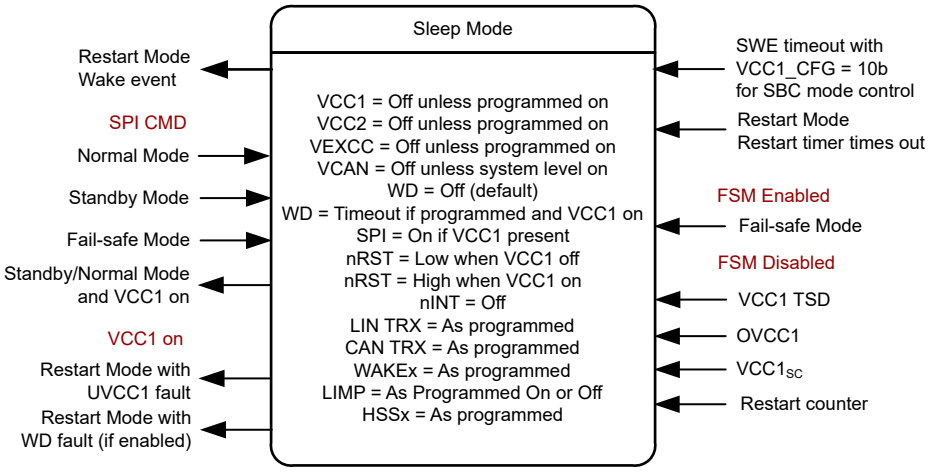

Figure 2-6. Sleep Mode

2.6 Fail-Safe Mode

The final mode for the SBC is fail-safe mode (FSM), an optional fault handling mode that can be used to increase design robustness. Upon entry to fail-safe mode most of the SBCs subsystems are turned off except LIMP which can be on, wake pins which can be as programmed, and the SWE timer. The following subsystems can react dependent on fault type: transceivers and HSS module.

There are five ways to enter fail-safe mode; all of which are fault conditions. Three of these are dependent on VCC1 – which include overvoltage (OVCC1), short circuit (VCC1_SC), thermal shut down (TSD). The other two entry pathways deal with restart mode failures, namely restart counter overflow or restart timer timing out.

There are three main ways to exit fail-safe mode and return to normal operation. The first way is a wake event occurs and all the faults have cleared which can cause the device to transition to restart mode. The second option is to enable the SWE timer during fail-safe mode and if the timer expires the device can transition to sleep mode and VCC1 can be off regardless of the programmed state of VCC1 during sleep mode. Lastly, if fail safe mode cyclic wake is enabled either timer1 or timer2 can have a programmed on time which can wake the device and check to see if faults have cleared – if enabled, the device can transition to restart mode otherwise the device remains in fail-safe mode until faults are cleared and that is detected during the on-time of the timer.

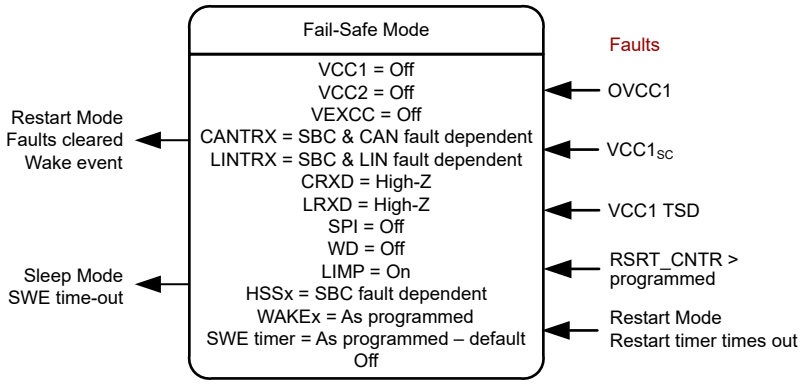

Figure 2-7. Fail-Safe Mode (FSM)

3 Power Electronics

With a basic understanding of how the device transitions between the different operational states, this is crucial to understand the power electronics within the device as well as some of the limitations. The TCAN28XX devices can be thought of as having three distinct power inputs and four distinct power management subsystems that act as power outputs and three distinct power inputs. The power inputs are VSUP, VHSS, and VCAN. For the power outputs, there are two integrated LDOs (VCC1 and VCC2), one integrated LDO controller (VEXCC), and four high side switch modules (HSS1 – HSS4).

3.1 VSUP

VSUP is the main power supply input into the device. This pin needs to be connected to the main power supply of the system – which is generally a battery that is nominally at a 12V output. This pin needs to have a reverse polarity protection diode between the pin and the power source as well as decoupling capacitances – especially a 100nF high frequency decoupling capacitor close to VSUP pin in addition to bulk capacitances. This is also highly suggested to include a PI filter after the diode that acts as an EMI filter. The SBC requires for operation that the VSUP voltage is between 5.5V to 28V which makes this a great option for 12V battery systems. The VSUP pin also acts as the input for the integrated LDOs as well as the external PNP attached to the integrated LDO controller. The voltage on VSUP governs when the device enters init and restart modes.

3.2 VHSS

VHSS is a separate power input that is used to feed the HSS module outputs (HSS1-HSS4). This has the same voltage input range as VSUP and in most applications can be directly shorted to VSUP – but this is not required. The VHSS pin only needs to be connected to a power supply if the HSS modules are used – if the pin remain unused, this pin does not need to be any input power. There needs to be a high frequency decoupling capacitor, 100nF, placed as close as physically possible to this pin if used in application.

3.3 VCAN

VCAN is the power input for the CAN transceiver and expects a 5V supply. This pin requires a power supply if the CAN bus is to be used at all in the application. There also needs to be a high frequency decoupling capacitor, 100nF, placed as physically close to the pin as possible. Many applications can use the VCC2 output to power the CAN bus and prevent the need for another discrete step-down power regulator. This pin does not need to request much more than 100mA of current during operation and in non-fault conditions generally less than 100mA.

3.4 VCC1

VCC1 is the primary LDO of the SBC that does not only provide an external power output but also is used to bias internal subsystems such as portions of the communication network and the SPI communication. VCC1's value is set based on the part number used – if the device has the pattern TCAN28xx5 the output is 5V and the logic pins of the device are referred to 5V and if the device part number has the pattern TCAN28xx3 the output is set to 3.3V with the logic pins referenced to 3.3V.

VCC1 can output up to 250mA of regulated output current that can be used to power external peripherals. A common use case of VCC1 is to power the controller of the SBC with the VCC1 voltage to eliminate the need for a discrete step-down regulator to power this controller. Other common options are providing biasing voltages for ADC inputs or other sensors (such as hall effect sensors).

VCC1, since this acts as the primary LDO for the TCAN28xx devices, also has a strong influence on the device state. Undervoltage events on VCC1 can result in the device transitioning to restart mode to try to bring VCC1 back to proper level or else this can transition to sleep or fail-safe (if enabled). Other fault conditions like OVCC1 and VCC1_SC can result in the device entering sleep or fail-safe (if enabled). The VCC1 LDO also has a temperature sensor that monitors the VCC1 LDO temperature and if a thermal fault is detected the device can transition to sleep or fail-safe mode. This LDO does act differently as faults on the other power electronics of the device do not result in mode changes, but on VCC1 there are mode changes. This is critical in any application that uses these devices that each VCC1 fault scenario is adequately mapped out at a system level to make sure the system can respond appropriately to VCC1 faults.

3.5 VCC2

VCC2 is the secondary LDO of the SBC that provides much of the same use cases as the VCC1 output with a few key differences. Every SBC in the TCAN28XX line of devices has the same output voltage for VCC2, 5V at a max output current of 200mA. In many applications this pin is directly connected to the VCAN pin – which regardless of TCAN28XX device chosen – requires a 5V supply and can generally have a supply current less than 100mA. The fault detection is also a bit different on the VCC2 LDO – this is because faults on VCC2 can result in action to be taken at the VCC2 output, VCC2 does not cause mode switches for the main SBC – so the SBC can run as normal even if the VCC2 output is currently in a fault state.

3.6 VEXMON, VEXCTRL, and VEXCC

The pins VEXMON, VEXCTRL, and VEXCC are all pins that lead to the integrated LDO controller of the TCAN28XX family. With the addition of a shunt resistor and PNP transistor with a β value between 50 and 500 an additional and adjustable LDO output is available. Connection for these pins is simple with a shunt resistance between VSUP and VEXMON and a PNP with the emitter pin connected to VEXMON, base pin on VEXCTRL, and collector pin on VEXCC can setup a 3**rd** LDO output for the device.

The controller supports output options of 1.8V, 2.5V, 3.3V, or 5V up to a current of 350mA while still supporting fault detection on this block. The fault detection is very similar to VCC2 in that faults on VEXCC does not cause the SBC to switch modes but only impact VEXCC block. This external LDO has the additional benefit of being able to load share with VCC1 allowing up to 700mA of output current for 3.3V or 5V (depending on TCAN28XX device chosen). These options are all configurable through the internal registers that are accessible through four-wire SPI communication.

The only value that can be a bit confusing to size is that of the shunt resistor between VSUP and VEXMON as this resistor has different purposes depending on usage of the VEXCC module.

If VEXCC is a stand-alone output then this resistance sets the current limit. The voltage drop between VSUP and VEXMON is controlled and specified to be between 150mV and 440mV regardless of VSUP or output configuration on VEXCC. The current produced with the voltage drop between VSUP and VEXMON – which following Ohm's law is 150mV to 440mV divided by the chosen shunt resistance – is the current limit of the VEXCC output. This can cause some confusion as the wide shunt voltage range leads to wide current limit ranges. To help simplify the 150mV value needs to be used as the point where under normal circumstances the load can never draw 150mV/R_shunt. The 440mV range needs to be used to tell you the max current limit – sometimes the max current limit is above the 350mA of maximum regulated output current– which means that current limiting does not initiate before and undervoltage or short circuit fault occurs. For example – if the application requires 150mA of current during operation this can be a good idea to set 160mA as the lowest possible current limit – which can just be 150mV/160mA which can be around 937.5mΩ as the shunt resistor. However, the lowest current that can trigger a current limit is 160mA – but the largest can be 440mV/937.5mΩ which is around 470mA. That means in this example the current limit can engage as soon as 160mA is reached, but this does not kick in until 470mA which means the device can experience an UV or short-circuit fault before the current is limited.

If VEXCC is being used in a load-sharing application the shunt resistor is used to set the ratio of current between the VEXCC and VCC1 outputs (for example, IEXCC/ICC1). This type of application expects higher total currents as low load currents, roughly less than 100mA, result in VEXCC not outputting current regardless of shunt resistance chosen. If the application load is less than 100mA is suggested not to use load sharing as the VEXCC generally cannot be outputting much – if any current at lower load currents. If the load current is larger the shunt resistance is picked through the following equations:

$$Ratio = \left(\frac{IVEXCC}{IVCC1}\right) \quad (1)$$

$$Rshunt = \left(\frac{8.824}{Ratio}\right) - \left(\left(\frac{1 + Ratio}{Ratio}\right) \times \left(\frac{0.8}{Iload}\right)\right) \quad (2)$$

In systems where the external LDO is not used the VEXMON pin needs to be shorted directly to VEXMON.

3.7 HSSx

The High Side Switch module (HSS) on the TCAN28xx devices contains four integrated high side switches labeled HSS1 through HSS4 that are fed from the VHSS pin. These switches can act as load switches, be used to generate a PWM signal, and used to generate a signal based on internal timer to the SBC. Individually, the switches each can carry up to 100mA of current and can be wired in parallel to allow up to 400mA of current through the switches.

Each HSS is individually controlled through the register configuration that is accessed through a four wire SPI bus. The switches have multiple modes that can be used in – on, off, associated to internal PWM (4 independent PWM's available at 200Hz or 400Hz with configurable duty cycles), associated to internal 10-bit timers (two options, timer1 and timer2), or directly driven through WAKE3/DIR (direct drive). These switches also detect fault conditions as well as open load conditions to the controller. HSS4 specifically can be used in cyclic sensing wake where the device uses HSS4 connected with a WAKE pin to periodically wake the device up based on either timer1 or timer2.

The addition of the high side switch module also upgrades this device from a general-purpose SBC to a mid-range device.

4 Communication Capabilities

The communication modules are some of the most important aspects of an SBC – the communication needed guides the type of SBC chosen for any specific application. The TCAN28XX line of devices do not disappoint as within the family there is support for classic CAN, CAN-FD, CAN-SIC, and LIN with devices varying depending on direct system needs.

4.1 CAN-FD and Classical CAN

CAN-FD and classical CAN are supported on all TCAN284XX devices. Each SBC contains a CAN-FD transceiver which is backwards compatible with classical CAN. The SBC can support up to 8Mbps for CAN-FD communications. There are only 4 communication pins to focus on for the CAN-FD transceiver – the pins are the differential pair (CANH and CANL) as well as the single ended logic I/O (CTXD and CRXD). The differential pair needs to be setup according to CAN standards – but an example of the CAN bus setup can be shown in the following figure.

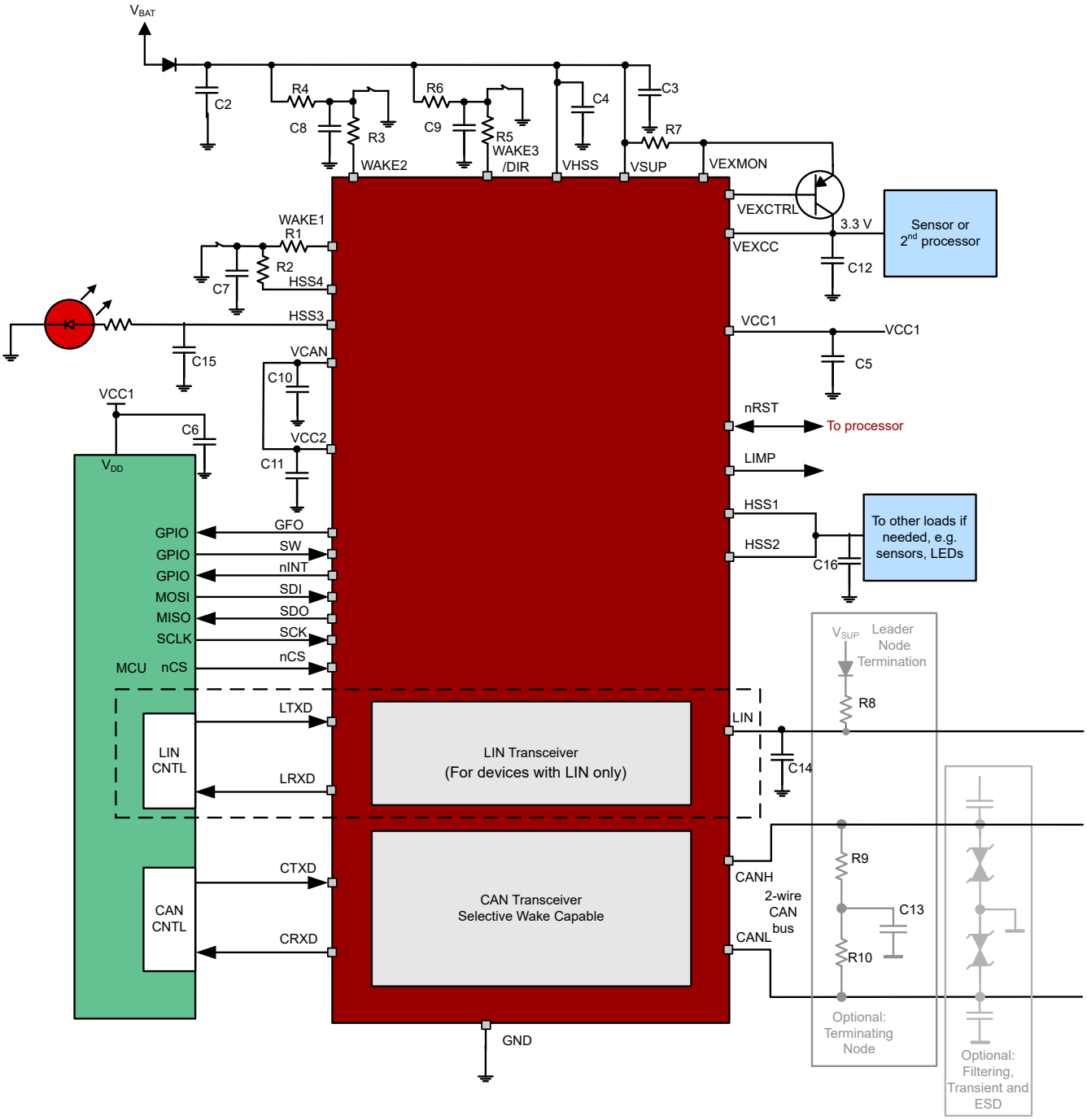

Figure 4-1. SBC Application Showing CAN Bus Connections

The transceiver can be configured as on, wake-capable, listen, off, controlled by SBC mode, or controlled by SBC mode without WUP support. The transceiver can be controlled independently of the SBC – however the SBC operating mode can determine what CAN modes can be used even if the transceiver is being controlled outside of an SBC mode control state.

Table 4-1. CAN State Availability by SBC Mode

SBC Mode	On	Listen	Wake Capable	Off	SBC Mode Control
Normal	Yes	Yes	Yes	Yes	On
Standby	No	Yes	Yes	Yes	Wake Capable
Sleep	No	No	Yes	Yes	Wake Capable
Restart	No	No	Yes	Yes	Wake Capable

Table 4-1. CAN State Availability by SBC Mode (continued)

SBC Mode	On	Listen	Wake Capable	Off	SBC Mode Control
Fail-Safe	No	No	Yes	Yes	Wake Capable

4.2 CAN-SIC

The TCAN285xx devices are very similar to the TCAN284xx devices except that the devices support CAN-SIC instead of classical CAN. There is not much difference in how to setup either device as the key difference between CAN and CAN-SIC is that in standard CAN communication there is a dominant (driven) state and a recessive (non-driven) state – however in CAN-SIC the recessive state is driven during the signal transition. The benefit of driving during the dominant to recessive transition is that this can reduce ringing caused by parasitic capacitances and inductances on the bus which can improve overall signal integrity. In general, the best CAN bus performance can be using CAN-SIC transceivers which are supported by the TCAN285xx line of devices.

4.3 LIN

LIN communication is supported on a subset of all the devices within the TCAN28XX family; namely devices with the pattern TCAN28X7X can contain a LIN transceiver. The devices with LIN capability with have 3 primary pins to focus on: the single ended logic I/O (LTXD and LRXD) and the LIN bus pin (LIN). The SBC can be configured as either a LIN commander or responder node depending on system need.

There are a few modes the LIN transceiver can operate in: on, fast, listen, wake capable, off, or SBC mode control. Similar to the CAN module – the transceiver can be configured independent of SBC mode, but SBC mode can determine available LIN modes.

Table 4-2. LIN State Availability by SBC Mode

SBC Mode	On	Fast	Listen	Wake Capable	Off	SBC Mode Control
Normal	Yes	Yes	Yes	Yes	Yes	On
Standby	No	No	Yes	Yes	Yes	Wake Capable
Sleep	No	No	No	Yes	Yes	Wake Capable
Restart	No	No	No	Yes	Yes	Wake Capable
Fail-Safe	No	No	No	Yes	Yes	Wake Capable

5 Protection Features

With strong feature support in terms of communication and power – the TCAN28XX family of devices also integrates extensive protection features to create a robust SBC. The protection features are multi-faceted that combine voltage monitoring, temperature monitoring, controller to SBC communication monitoring (through a watchdog timer), communication bus fault monitoring, LIMP home indicator, and a separate fail-safe mode available to SBC. The following subsections can take a dive into where the protection features are with a high-level guide to how they operate. Table 5-1 highlights important protection feature specifications.

Table 5-1. Key Supply Characteristics w.r.t. Fault Thresholds

Pin	Spec ID	Spec. Description	Min Value	Typ. Value	Max Value
ELECTRICAL SPECIFICATIONS					
VSUP	VSUP(PU)R	Supply On Detection	3.1V	3.4V	3.7V
VSUP	VSUP(PU)F	Supply Off Detection	2.7V	3V	3.3V
VSUP	UVSUP5R	5V Supply UV Recovery	4.9V	-	5.5V
VSUP	UVSUP5F	5V Supply UV Detection	4.5V	-	5.1V
VSUP	UVSUP33R	3.3V Supply UV Recovery	3.7V	-	4.4V
VSUP	UVSUP33F	3.3V Supply UV Detection	3.55V	-	4.25V
VHSS	UVHSSR	VHSS UV recovery	4.6V	-	4.9V
VHSS	UVHSSF	VHSS UV Detection	4.4V	-	4.7V
VHSS	OVHSSR	VHSS OV Detection	20V	-	22V
VHSS	OVHSSF	VHSS OV Recovery	18.8V	-	21.2V
VCAN	UVCANR	VCAN UV Recovery	-	4.2V	4.5V
VCAN	UVCANF	VCAN UV Detection	3.5V	4V	-
VEXCC	UVEXCCR	VEXCC UV Recovery	0.87 * VEXCC	0.9 * VEXCC	0.93 * VEXCC
VEXCC	UVEXCCF	VEXCC UV Detection	0.81 * VEXCC	0.85 * VEXCC	0.89 * VEXCC
VEXCC	OVEXCCR	VEXCC OV Detection	1.12 * VEXCC	1.15 * VEXCC	1.18 * VEXCC
VEXCC	OVEXCCF	VEXCC OV Recovery	1.07 * VEXCC	1.1 * VEXCC	1.13 * VEXCC
VEXCC	VEXCCSC18	VEXCC Short detection for 1.8V and 2.5V outputs	-	1.1V	1.26V
VEXCC	VEXCCSC	VEXCC Short Detection for 3.3V and 5V outputs	1.7V	-	2.3V
VCC1 (5V)	UVCC1R1	VCC1 UV Recovery 1	4.6V	-	4.85V
VCC1 (5V)	UVCC1F4	VCC1 UV Detection 1	4.5V	-	4.75V
VCC1 (5V)	UVCC1R2	VCC1 UV Recovery 2	3.85V	-	4.15V
VCC1 (5V)	UVCC1F4	VCC1 UV Detection 2	3.75V	-	4.05V
VCC1 (5V)	UVCC1R3	VCC1 UV Recovery 3	3.25V	-	3.55V
VCC1 (5V)	UVCC1F4	VCC1 UV Detection 3	3.15V	-	3.45V
VCC1 (5V)	UVCC1R4	VCC1 UV Recovery 4	2.5V	-	2.9V
VCC1 (5V)	UVCC1F4	VCC1 UV Detection 4	2.4V	-	2.8V
VCC1 (5V)	OVCC1R1	VCC1 OV Detection 1	5.25V	-	5.5V
VCC1 (5V)	OVCC1F1	VCC1 OV Recovery 1	5.15V	-	5.4V
VCC1 (5V)	OVCC1R2	VCC1 OV Detection 2	5.5V	-	5.7V
VCC1 (5V)	OVCC1F2	VCC1 OV Recovery 2	5.7V	-	5.6V

Table 5-1. Key Supply Characteristics w.r.t. Fault Thresholds (continued)

Pin	Spec ID	Spec. Description	Min Value	Typ. Value	Max Value
VCC1 (5V)	VCC15SC	VCC1 Short Circuit Detection Threshold	1.7V	-	2.3V
VCC1 (5V)	UVCC15RPR	VCC1 UV Prewarning Recovery (VCC1 = 5V)	4.65V	-	4.9V
VCC1 (5V)	UVCC15FPR	VCC1 UV Prewarning Detection (VCC1 = 5V)	4.55V	-	4.8V
VCC1 (3.3V)	UVCC1R1	VCC1 UV Recovery 1	3V	-	3.2V
VCC1 (3.3V)	UVCC1F4	VCC1 UV Detection 1	2.95V	-	3.15V
VCC1 (3.3V)	UVCC1R2	VCC1 UV Recovery 2	2.55V	-	2.75V
VCC1 (3.3V)	UVCC1F4	VCC1 UV Detection 2	2.5V	-	2.7V
VCC1 (3.3V)	UVCC1R3	VCC1 UV Recovery 3	2.25V	-	2.45V
VCC1 (3.3V)	UVCC1F4	VCC1 UV Detection 3	2.2V	-	2.4V
VCC1 (3.3V)	UVCC1R4	VCC1 UV Recovery 4	2.05V	-	2.25V
VCC1 (3.3V)	UVCC1F4	VCC1 UV Detection 4	2V	-	2.2V
VCC1 (3.3V)	OVCC1R1	VCC1 OV Detection 1	3.45V	-	3.6V
VCC1 (3.3V)	OVCC1F1	VCC1 OV Recovery 1	3.4V	-	3.55V
VCC1 (3.3V)	OVCC1R2	VCC1 OV Detection 2	3.6V	-	3.8V
VCC1 (3.3V)	OVCC1F2	VCC1 OV Recovery 2	3.5V	-	3.7V
VCC1 (3.3V)	VCC133SC	VCC1 Short Circuit Detection Threshold	-	1.22V	1.26V
VCC1 (3.3V)	UVCC133RPR	VCC1 UV Prewarning Recovery (VCC1 = 3.3V)	3.1V	-	3.28V
VCC1 (3.3V)	UVCC133FPR	VCC1 UV Prewarning Detection (VCC1 = 3.3V)	3V	-	3.2V
VCC2	UVCC2R	VCC2 UV Recovery	4.6V	-	4.9V
VCC2	UVCC2F	VCC2 UV Detection	4.5V	-	4.75V
VCC2	OVCC2R	VCC2 OV Detection	5.4V	-	5.6V
VCC2	OVCC2F	VCC2 OV Recovery	5.2V	-	5.5V
VCC2	VCC2SC	VCC2 Short Circuit Detection Threshold	1.7V	-	2.3V
TIMING SPECIFICATIONS					
LDO Outputs	tUVFLTR	UV detection delay	25us	-	50us
VCC1	tUVCC1PR	UV Prewarning Detection Delay	2us	-	12us
VCAN	tUVCANFLTR	UV Detection Delay on VCAN	2us	-	10us
LDO Outputs	tOVFLTR	OV Detection Delay	20us	-	45us
VHSS	tOVFLTRVHSS	OV Detection Delay VHSS	4us	-	12us

Table 5-1. Key Supply Characteristics w.r.t. Fault Thresholds (continued)

Pin	Spec ID	Spec. Description	Min Value	Typ. Value	Max Value
LDO Outputs	tVSC	SC Detection Delay	75us	100us	125us
VCC1+VEXCC	tVSCLS	SC Detection Delay when VEXCC and VCC1 are load sharing	75us	100us	125us
LDO Outputs	tLDOON	LDO On time during FSM to check if fault has cleared	-	-	3.8ms
VCC1	tLDOOFF	LDO Off time in fail-safe mode before wake events are accepted	250ms	300ms	350ms

5.1 Undervoltage (UV) Monitors

The TCAN28XX line of devices contains multiple voltage supervisors that monitor for undervoltage events on the following pins: VSUP, VHSS, VCAN, VEXCC, VCC1, and VCC2

5.1.1 VSUP

There are two or three low voltage levels monitored on the VSUP pin depending on the device chosen. For devices with VCC1 = 3.3V a supply detection threshold, VSUP_PU, a 3.3V level UVSUP_33, and a 5V level UVSUP_5 are monitored. If VCC1 = 5V only the supply detection and UVSUP_5 are monitored. The supply detection level is the boundary between the device in the unpowered or off state and the devices init mode – if the supply voltage rises above the supply detection threshold the device can start init mode and if this falls below the device can be in an off or unpowered state. For devices with VCC1 = 3.3V once the supply voltage has crossed the UVSUP_33 level VCC1 is able to be produce a regulated output and when VSUP has crossed the UVSUP_5 level VCC2 can produce a regulated output and be in regulation while other functions can be utilized. If devices with VCC1 = 3.3V have the supply voltage fall below the UVSUP_5 level the CAN transceiver can turn off, VCC2 can be in pass through, the LIN transceiver, on applicable devices, can still work but does not meet electrical and timing characteristics described in data sheet. For devices with VCC1 = 5V the SBC can react the same way as devices with VCC1 = 3.3V, but instead of the UVSUP_5 level only instead of a combination of UVSUP_33 and UVSUP_5.

5.1.2 VHSS

The VHSS pin has one UV monitor to detect a UVHSS event. A UVHSS event can be reported via the nINT pin (assuming device still has power) and can be indicated by the INT_4 interrupt register. The default behavior for a UVHSS event is to nothing beyond generate an interrupt; however, this can be configured to disable the switches in cases of undervoltage.

5.1.3 VCAN

The VCAN pin has one UV monitor to detect UVCAN events. When the voltage at the VCAN pin drops below UVCAN the transmitter switches off and disengages from the bus until VCAN has recovered. The receiver is still active. When the device is unpowered the device has an extremely low loading effect on the CAN bus as the leakage current is extremely low – with a max of 5uA.

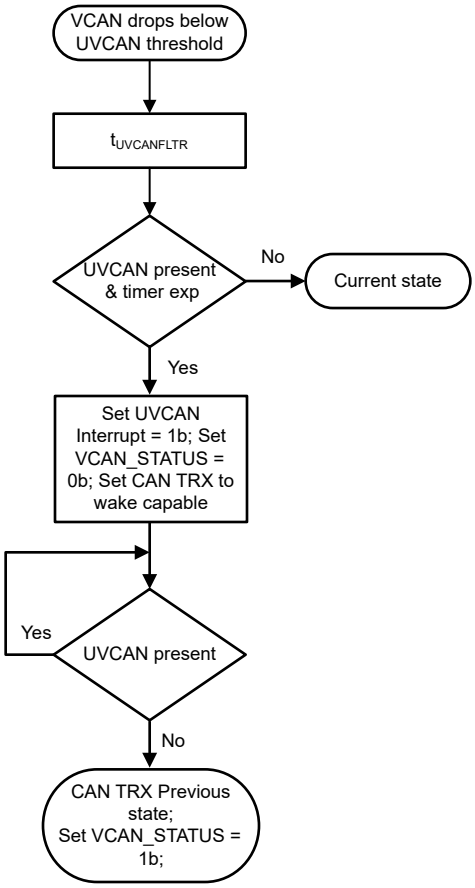

Figure 5-1. UVCAN State Diagram

5.1.4 VEXCC

The VEXCC output pin has monitors for UVEXCC events. UV events on the VEXCC pin can trigger an interrupt but does not cause an SBC mode change.

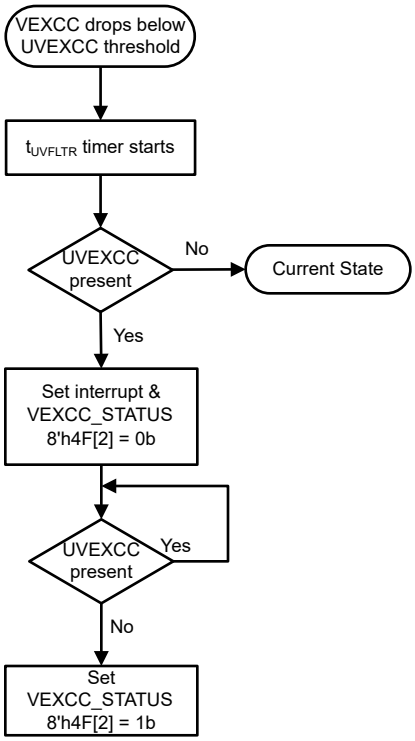

Figure 5-2. UVEXCC State Diagram

5.1.5 VCC1

The VCC1 output pin has both an UV monitor and a UV pre-warning that is used to watch the voltage on the output of VCC1. There are four different choices of UV thresholds for both devices where VCC1 = 3.3V and VCC1 = 5V; however, there only exists one pre-warning threshold within the device.

Since VCC1 is used for many internal functions of the SBC as well as the fact that most VCC1 outputs are used to power up the companion controller to SBC, UV events on the VCC1 rail have a much more complex reaction to UV events. The device first detects the VCC1 voltage dropping below the prewarning threshold and if this condition is held until for a long enough period to be detected by the UV filter timer this can set the prewarning interrupt and if UV event is gone this can remain in the same state. If the voltage continues to drop to where a UVCC1 event is triggered the device can then transition to Restart Mode with the SBC indicating the mode by pulling nRST low and the restart counter, if enabled can be incremented. If the restart counter hasn't been exceeded the device can start the restart timer and if the UVCC1 condition clears, VCC1 > UVCC1R for tRSTN_act, before the end of the restart timer the device can transition back into standby mode. If the restart timer times out before the UVCC1 condition clears the device can enter fail-safe mode, if enabled, or sleep otherwise. As previously mentioned, the UVCC1 threshold has four configurable options for each device in the TCAN28XX family of devices.

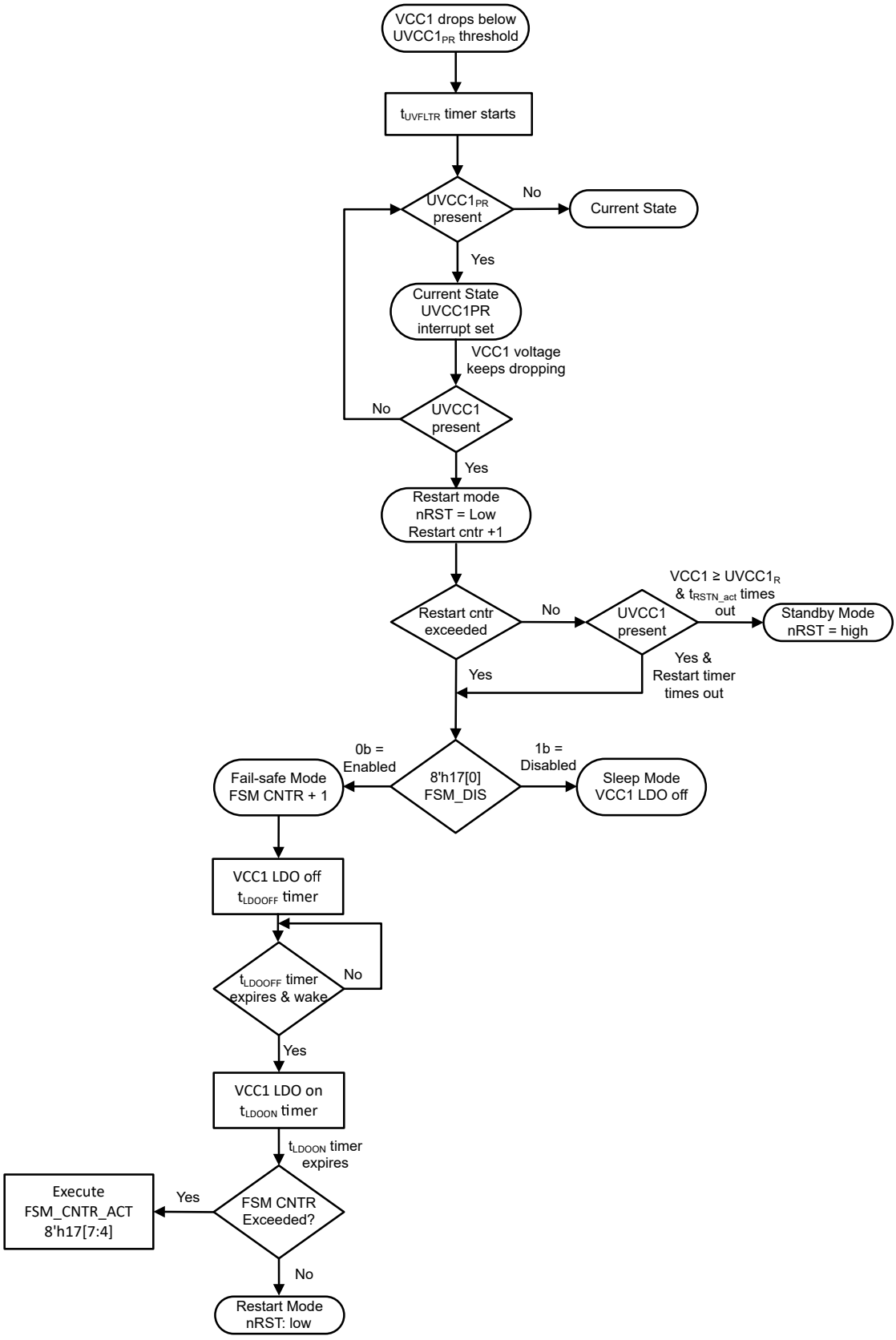

Figure 5-3. UVCC1 State Diagram

5.1.6 VCC2

The VCC2 pin, like VEXCC, monitors for UV events, but in case of UV event only an interrupt can be triggered with the SBC remaining in the current state.

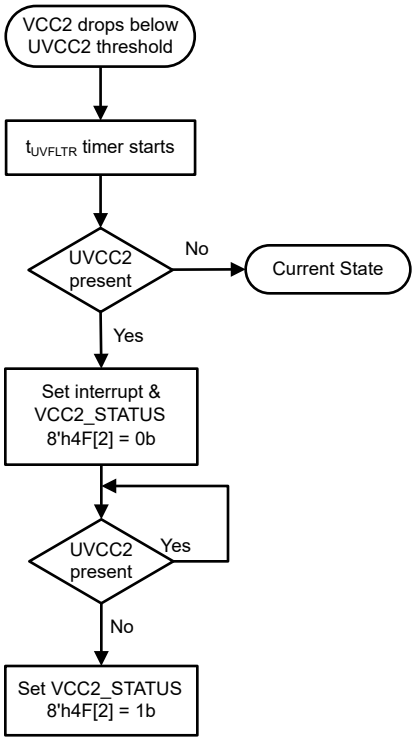

Figure 5-4. UVCC2 State Diagram

5.2 Overvoltage (OV) Monitors

5.2.1 HSSx

The HSS pins are monitored for OV conditions on the outputs. Similarly, to the UV conditions – by default all an OV condition can do is signal the condition on the nINT pin indicating an interrupt has been flagged. The pins can be configured that the switch is opened and disconnected from load in case of OV event – similar to UV event.

5.2.2 VCC1

VCC1 also is monitored for OV conditions; there is no pre-warning for OV events and there are two selectable OV thresholds to choose from on each variant device within the TCAN28XX family. If an OV event on VCC1 (OVCC1) is detected VCC1 can be shut-off and interrupt can be set before transitioning to fail safe mode, if enabled, or sleep mode otherwise. If device enters fail-safe mode the VCC1 output can be turned off for a period of tLDOOFF while the device monitors for wake events. If the timer has expired, there has been a wake-signal received, and the OVCC1 event has been cleared the device can check the fail-safe counter to determine next steps; however, if not all three of the checks are met the device can shut VCC1 off again and repeat. If the fail-safe counter hasn't been exceeded the device can restart but if the counter has been exceeded the device can respond based on the configuration in the FSM_CNTR_ACT bit field of register 17h. By default, the action is disabled but this can be changed to either perform a hard-reset (POR) or stop responding to wake events and go to sleep until the power is cycled.

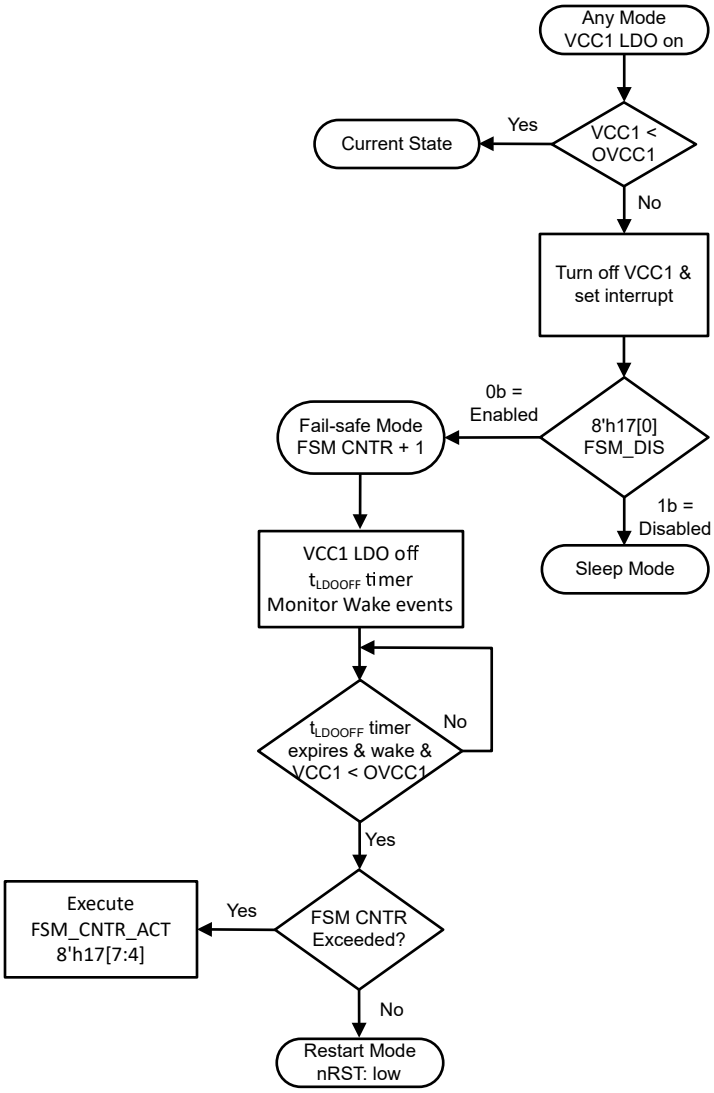

Figure 5-5. OVCC1 State Diagram

5.2.3 VCC2

VCC2 is also monitored for OV conditions. There is only one OVCC2 condition watched and there are no pre-warnings generated. If an OV condition is found VCC2 is shut off, an interrupt is generated, and VCC2's status bit is set to 0. This condition can be monitored until VCC2 < OVCC2 (recovery) which when reached can turn VCC2 back on and set the status bit to 1.

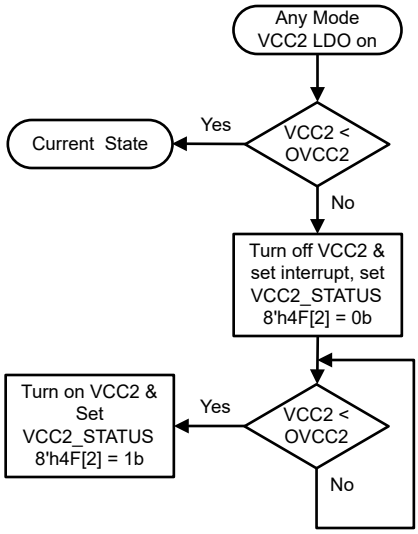

Figure 5-6. OVCC2 State Diagram

5.2.4 VEXCC

VEXCC is also monitored for OV conditions. The behavior to OV conditions is identical, except in terms of voltage thresholds as VEXCC has a variable output, but the overall process remains the same.

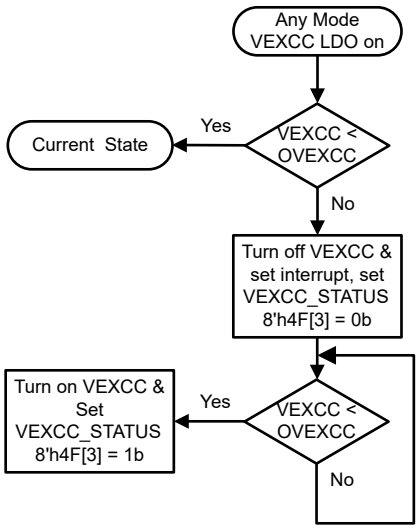

Figure 5-7. OVEXCC State Diagram

5.3 Short Circuit (SC) Monitors

The SBC also uses voltage monitors to watch for short circuit (SC) conditions on the voltage outputs VCC1, VCC2, and VEXCC. These monitors are not looking for an increase of current, but rather are UV monitors with much lower thresholds than what is described the UV section of protection features. SC events, similar to OV events, have more drastic impacts to the output where the short circuit is detected.

5.3.1 VCC1

VCC1 has the most complex reaction to SC events on the output due to this being intertwined with much of the SBC functionality and the expected use case (powering companion controller). On the onset of a SC event both the tUVFLTR and tVSC timers begin where tUVFLTR < tVSC. When the tUVFLTR timer expires the devices moves to restart mode and increments the restart counter. If the restart counter has not been exceeded the tVSC timer continues to run and if that expires VCC1 is shut off and the SC interrupt is generated and the device enters fail-safe, if enabled, and sleep otherwise. If the restart counter has been exceeded the device

automatically can transition to fail-safe mode, if enabled, and sleep otherwise. If fail-safe mode is enabled and the short has not been resolved the device transitions to fail-safe mode and starts the tLDOOFF with VCC1 = off. If the timer expires and there is a wake condition present the device can check to see if the fail-safe counter has been exceeded, and if the timer has this, can take the action as configured in bit field 7:4 at address 17h. If the counter has not been exceeded VCC1 can be turned on for tLDOON and the nRST pin can be pulled low. After the timer has expired if the short circuit condition has resolved the device goes to restart mode otherwise the device can go to sleep mode.

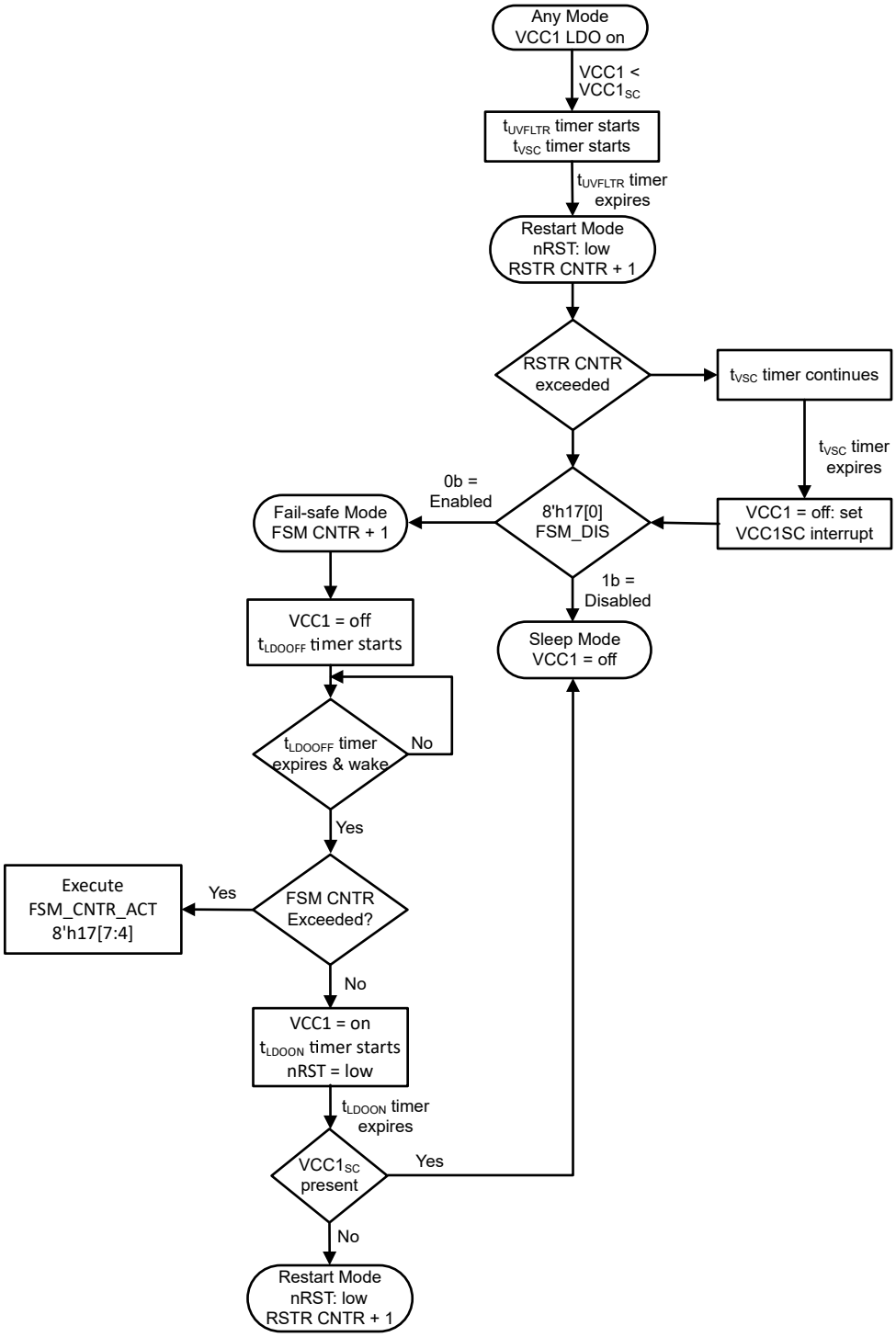

Figure 5-8. VCC1(SC) State Diagram

5.3.2 VCC2

VCC2 also monitors for short circuit events, but with much less impact on overall device during short circuits. Once a short circuit is detected the tVSC timer can start and if an event is detected after timer expires VCC1 is shut off, an interrupt is generated, and the VCC2 status bit is changed to 0. VCC2 can remain off until a SPI command is issued that turns VCC2 back on – at which point VCC2 output can be monitored for tLDOON time. If at the end of the tLDOON timer the short circuit still exists the process repeats otherwise VCC2 can remain on and the VCC2 status can be set to 1.

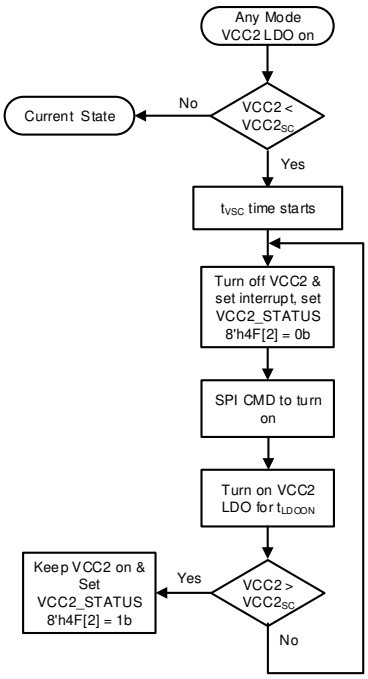

Figure 5-9. VCC2(SC) State Diagram

5.3.3 VEXCC

VEXCC is also monitored for SC conditions on the output. The VEXCC output operates in the same exact process as the VCC2 short circuit detection routine that exists on SBC.

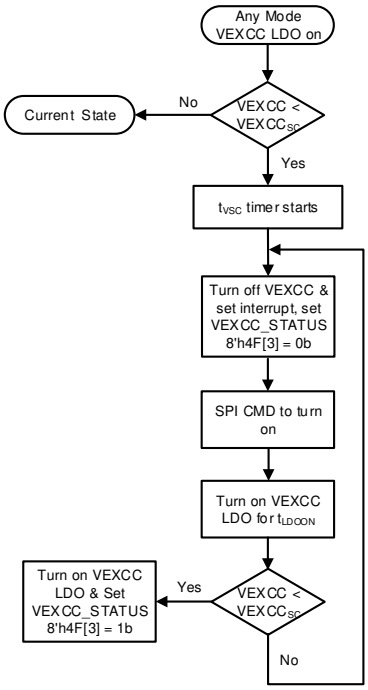

Figure 5-10. VEXCC(SC) State Diagram

5.4 Electrical Faults and Impact on SBC Mode

This has been discussed in previous sections how certain faults, primarily on VCC1, can impact the entire SBC mode and functionality – to summarize these points please see following tables that explain device state w.r.t. fault conditions.

Table 5-2. SBC Mode Vs. Fault Conditions

VSUP	VCC1	VCC2	VEXCC	SBC Mode
>UVSUP	>UVCC1	>UVCC2	N/A	Normal/Standby
>UVSUP	<UVCC1PR	>UVCC2	N/A	Previous Mode
>UVSUP	<UVCC1	>UVCC2	N/A	Restart
>UVSUP	>UVCC1	<UVCC2	N/A	Previous Mode
>UVSUP	>UVCC1	>UVCC2	<UVEXCC	Previous Mode
>UVSUP	>OVCC1	N/A	N/A	Fail-Safe or Sleep
>UVSUP	>UVCC1	>OVCC2	N/A	Previous Mode
>UVSUP	>UVCC1	N/A	<OVEXCC	Previous Mode
>UVSUP	<VCC1SC	N/A	N/A	Fail-Safe or Sleep
>UVSUP	>UVCC1	<VCC2SC	N/A	Previous Mode
>UVSUP	>UVCC1	N/A	<VEXCCSC	Previous Mode

5.5 Temperature Sensors

There are two separate temperature sensors monitoring the dies temperature on devices within the TCAN28XX family. The first sensor covers VCC1 LDO, external PNP control pins, and VEXCC; while the second covers VCC2 LDO, CAN transceiver, and LIN transceiver (if device is LIN capable). An overview of thermal specifications is shown in the following table.

Table 5-3. Thermal Shutdown (TSD) Key Specifications

Spec. ID	Spec. Description	Min	Typical	Max
TSDWR	Thermal Shutdown Warning	145°C	-	165°C
TSDWF	Thermal Shutdown Warning Release	130°C	-	155°C
TSDR	Thermal Shutdown	165°C	-	200°C
TSDF	Thermal Shutdown Release	155°C	-	190°C

The first temperature sensor that covers VCC1 as well as VEXCC and the associated control pins includes a thermal shutdown warning TSDW that can set an interrupt if crossed. The warning doesn't impact how the device is operating, but acts as an alert of a possible thermal shutdown occurring soon if action is not taken. If VCC1 or VEXCC see an increase in temperature to the thermal shutdown level, TSD, the TSD interrupt flag for VCC1/VEXCC can be set. VCC1 and VEXCC can be shut off during a thermal shutdown and the SBC can enter fail-safe mode if enabled and sleep otherwise and the nRST pin can be pulled low. If the device has fail-safe mode enabled if the die temperature falls below TSDF for 1s the device can transition to restart mode and turn VCC1 and VEXCC (if utilized) back on. During the thermal shutdown event VCC1 is off and the high side switches configuration can be reset – so if cyclic sensing is being utilized when a TSD event occurs the cyclic sensing functionality is no longer present.

The second temperature sensor covers VCC2 as well as the integrated transceivers. If a TSD event occurs on the second sensor VCC2 is shut off with the status being changed to 0 while the transceivers can be put into listen mode; this can also be marked with an interrupt being generated. Once the temperature has dropped below TSDF the transceivers can be re-enabled and after 1s VCC2 can be turned back on. If VCC2 is being used to power VCAN during a TSD event where VCC2 is shutoff a UVCAN event can occur putting the CAN transceiver into a wake capable state and cannot be re-enabled until VCC2 is fully powered again.

5.6 Watchdog

5.6.1 Watchdog Error Counter

Another popular protection feature that is common amongst varied applications is a watchdog timer. The watchdog timer is a bit more of an intelligent protection feature as instead of looking for thermal or electrical overstress this is used to make sure that proper communication is upheld between the controller and the SBC. The watchdog timer integrated into the TCAN28XX family of devices can be configured into multiple modes of operation depending on SBC mode. By default, watchdog has a long window period during the transition from restart to standby mode, this is active in standby after initial long window, and also active in normal mode. This can also be turned on in sleep mode if VCC1 is set to be active during sleep mode.

5.6.2 Timeout

The watchdog within the TCAN28XX line of devices also integrates a watchdog error counter. The counter increments whenever there is a missed watchdog event and decrements the error counter for correct events – but the counter can never go below 0. There is a threshold value that can be programmed to allow up to 15 missed triggers before SBC acts – but the default value is action can be taken after the first missed watchdog. When the error counter has surpassed the threshold, the SBC can move to restart mode with the watchdog error counter returning to 0 and then can return to standby mode. If the device restarts more than the restart counter allows a missed watchdog can result in entering fail-safe mode (if enabled) and sleep mode otherwise. The watchdog error counter is used in every type of watchdog implementation allowed by SBC.

5.6.3 Window

Window watchdog is a slightly more complex implementation of the timeout watchdog. In window watchdog there is a timeout period, like in the timeout watchdog; however, a watchdog trigger cannot be issued at any time during the window period unlike timeout. In window watchdog the window period is split evenly into a closed window period and an open window period, where the watchdog trigger must be sent during the open window period. This can be the second half of the window length – so for 128ms window the second 64ms is where the watchdog must trigger – however this is not that simple. The window, closed window, and open window periods all include tolerances so the tolerances are not exact. The safe trigger area can actually take up less than half of the total window period. The safe trigger area size can be calculated by taking the minimum total window time and subtracting the maximum closed window time where the start of the safe trigger area is the maximum closed window time and the end of the safe trigger area is the minimum window length. The TCAN28XX line of devices uses an internal oscillator with a +/-10% accuracy range to set up the window periods. If the window is set to 128ms, that means realistically, the closed and open windows are 64ms each – however with the ±10% tolerance this is unwise to use the nominal timing. First, finding the maximum closed window time, which is 1.1 × 64 = 70.4ms. Next, the minimum window period, which is 0.9 × 128ms = 115.2ms. Finally, with these two values the safe trigger area in this case is 70.4ms to 115.2ms instead of the 65ms to 128ms that can exist without tolerance.

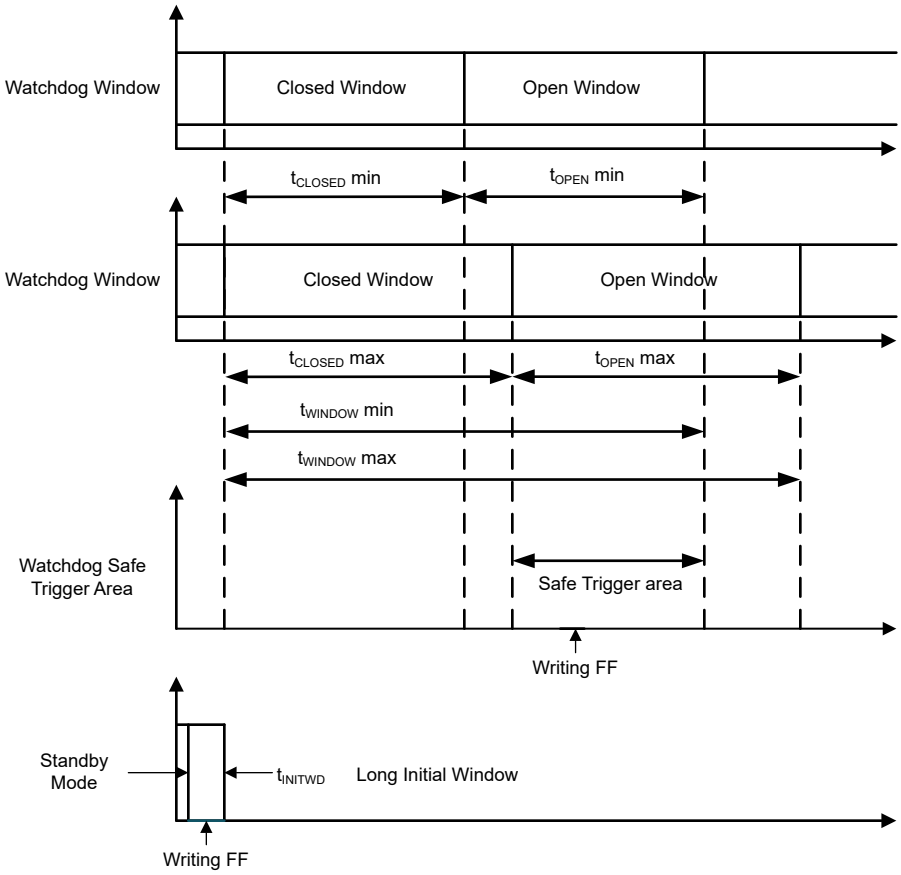

Figure 5-11. Window Watchdog Timing

5.6.4 Initial Long Window

There is a special window watchdog used when the SBC transitions from restart mode to standby mode. This is called the initial long window – and operates the same way as the standard window watchdog – but uses a different timing scheme to implement. The reason this is called a long window is because the shortest long window duration is a 150ms window and the default is 600ms where with typical window timing this is possible to have windows <150ms. The reason that this longer period exists is because all watchdog configuration must be done before the long window can be triggered as the watchdog registers lock after the long window has expired. This is also separate from other watchdog options available in standby mode and only occurs once on the transition from restart to standby.

5.6.5 Q&A

Q&A watchdog is the most complex watchdog scheme that can be implemented with the TCAN28XX line of devices. This integrates the window period of the window watchdog, but increases the complexity of the response trigger. In Q&A mode the watchdog has a window setup like in window watchdog, but the SBC expects responses in both sections of the total window. In this setting the SBC can pose a question that is read by the controller and the controller can respond with a 4-byte answer. The initial question read and the thee most significant bytes send to the SBC must occur in the first window section where the least significant byte is transmitted during the second period. Upon the reception of the last answer byte the question is reset, so in the first window the controller can actually skip the question request and just start with the answer (as long as the new question is known by controller). This not only makes sure that the communication link is in a decent condition like the previous watchdog types, but this also adds a layer of complexity by making the controller solve math problems and respond in reasonable state of time. This makes sure that valid data is being sent by the controller, not just if the controller is responding or not which gives an additional layer of robustness in the system as certain issues are not caught by standard watchdog implementations.

5.7 Communication Fault Monitoring

Fault monitoring on the communication bus is a system level key concern. Communication faults can result in the entire communication bus to become compromised causing potential harm to more than just the malfunctioning node. The TCAN28XX line of devices does include fault monitoring on itsthe communication busses to mitigate harm by alerting the controller of potential faults.

5.7.1 CAN

The CAN bus is monitored for 7 different fault conditions on the TCAN28XX line of devices; these are all captured in the CANBUS interrupt register (54h).

Table 5-4. CAN Bus Interrupts on TCAN28xx Devices

Bit Field	Flag	Description
7	UVCAN	UV Event on VCAN
6	RESERVED	N/A
5	CANHCANL	CANH and CANL shorted
4	CANHBAT	CANH shorted to battery
3	CANLGND	CANL shorted to GND
2	CANBUSOPEN	CAN Bus Opened
1	CANBUSGND	CANH shorted to GND or both CANH and CANL shorted to GND
0	CANBUSBAT	CANL shorted to VBAT or both CANH and CANL shorted to VBAT

From the interrupts that are monitored this needs to be clear that the fault types are not exhaustive and an interrupt alone generally does not give all the information an end designer wants or needs to know. To highlight this concept, ten different fault cases can be used to show what interrupts are registered and what information can be gathered from each fault at the SBC.

Table 5-5. CAN Bus Fault Scenarios

Fault #	CANH	CANL	Fault Detected	Comment
1	Open	Open	CANBUSOPEN	N/A
2	Open	Normal	CANBUSOPEN	SBC cannot tell difference between fault 1 and 2
3	Normal	Open	CANBUSOPEN	SBC cannot tell difference between faults 1,2, and 3
4	Shorted to CANL	Shorted to CANH	CANHCANL	N/A
5	Shorted to VBAT	Normal	CANHBAT	N/A
6	Shorted to GND	Normal	CANBUSGND	N/A
7	Normal	Shorted to VBAT	CANBUSBAT	N/A
8	Normal	Shorted to GND	CANLGND	N/A
9	Shorted to GND	Shorted to GND	CANBUSGND	SBC cannot tell difference between faults 6 and 9
10	Shorted to VBAT	Shorted to VBAT	CANBUSBAT	SBC can’t tell difference between faults 7 and 10

With interrupt map explored for CAN faults this needs to be clear that the SBC can tell the controller through an interrupt that there is an issue – and give some information on the fault – but this does not necessarily give all pertinent information about location and does not even give enough information to determine the pin that is at fault depending on exact fault scenario.

One fault that hasn’t been talked about is the dominant timeout fault. At the logic input pin, CTXD, if the level is set near GND and the device doesn’t detect a rising edge on this pin for 1ms (min) to 5ms(max) the CAN driver is disabled to prevent stuck bus conditions.

5.7.2 LIN

The LIN bus is not monitored in the same way that the CAN bus is – there is only one main protection feature on the LIN transceiver and that is dominant timeout. Similar to the CAN bus if the LIN transceiver is stuck on a dominant state for [20ms(min), 45ms(typ), 80ms(max)] the LIN transmitter is disabled to prevent stuck bus conditions.

5.8 LIMP

The last protection feature that has been briefly mentioned previously is the LIMP pin which supports LIMP home functionality. The LIMP signal is an active low output that can signal a system that there is a major issue that is occurring on the device. By default, the LIMP pin can activate when there are missed watchdog triggers and won't reset until the configured condition is met - which by default is three correct watchdog triggers after the missed watchdog trigger. This pin also can activate when the device enters into fail-safe mode alerting the system at large that there was a fault that caused the SBC to enter the fail-safe mode. This is possible to read the LIMP pin state, assuming VCC1 is active, by first enabling the read ability, which is done by setting 1A[6] = 1, then reading the LIMP state at address 1A[5].

6 Programming, Memory, and Control

The TCAN28xx line of devices includes a 4-wire SPI bus, an 8-bit register stack, and includes an EEPROM for device trimming and custom configurations. For a deep dive on all these subjects please look at *Firmware Guide for TCAN24xx and TCAN28xx Devices* or the specific data sheet of the TCAN28xx device being used.

6.1 SPI

The TCAN28XX line of devices includes a 4-wire SPI bus. The SBC is a peripheral device and expects the controller to control the communication flow between SBC and controller. The SDO, SDI, and SCLK pins represent the serial data out, serial data in, and serial clock data for the SBC; while the nCS pin is the active low chip select line. The device defaults to SPI mode 0 and expects one-byte transactions without a CRC. The device does support SPI modes 1, 2, and 3 as well as two-byte transaction mode and one-byte transaction mode with CRC enabled. The maximum SPI speed is 4MHz for one-byte mode without CRC and 2MHz otherwise. Configuration, watchdog triggers, and saving configurations are all done through the SPI bus.

6.2 EEPROM

The TCAN28xx line of devices also includes an EEPROM that serves 2 main purposes. The first purpose is that this contains trimming information for device operation – this portion of the EEPROM is not accessible to end user. The second use is to save a partial configuration using an EEPROM save – the following bits are saved within the TCAN28xx line of devices.

Table 6-1. Registers and Bits That can be Stored in EEPROM

Register ID	Register Address	Bits Saved
SPI_CONFIG	9h	0-3
SBC_CONFIG	Ch	0-1,4,6
VREG_CONFIG1	Dh	0-7
SBC_CONFIG1	Eh	0,3-5,7
WAKE_PIN_CONFIG1	11h	0-4
WAKE_PIN_CONFIG2	12h	0-1,5,6
WD_CONFIG_1	13h	0-7
WD_CONFIG_2	14h	0,5-7
WD_RST_PULSE	16h	4-7
DEVICE_CONFIG1	1Ah	0,4,7
DEVICE_CONFIG2	1Bh	0
SWE_TIMER	1Ch	3-7
nRST_CNTL	29h	5
WAKE_PIN_CONFIG4	2Bh	0-1,3,4-5,7
WD_QA_CONFIG	2Dh	0-7
HSS_CNTL3	4Fh	0,4

To save a partial configuration to the EEPROM one-byte transactions with CRC must be enabled. If the companion controller chosen does not support CRC bytes, please see table 8-26 in data sheet for process to save to EEPROM without CRC capable controller.

6.3 Interrupts

There are eight interrupt registers and one global interrupt register contained within the TCAN28XX line of devices. The global interrupt vector uses each bit as a logical OR'd output of a different interrupt register with the following structure.

Table 6-2. Global Interrupt Vector

Bit Position	Data	Comment
7	INT_7	Logical OR'd output of INT_7
6	INT_1	Logical OR'd output of INT_1

Table 6-2. Global Interrupt Vector (continued)

Bit Position	Data	Comment
5	INT_2	Logical OR'd output of INT_2
4	INT_3	Logical OR'd output of INT_3
3	INT_CANBUS	Logical OR'd output of INT_CANBUS
2	INT_4	Logical OR'd output of INT_4
1	INT_5	Logical OR'd output of INT_5
0	INT_6	Logical OR'd output of INT_6

Any issue that is flagged in one of interrupt registers can also show an interrupt in the global interrupt vector. Every SPI transaction that is performed on the device, regardless of SPI setup, can have the first byte out of the SDO pin as the global interrupt vector – so if an interrupt has been generated, this can show up here. If VCC1 is active, the interrupt generation can result in the nINT pin being pulled low. A full overview of interrupts can be seen in the following table.

Table 6-3. Device Interrupts

Register	Address	Bit Position	Data	Comment
INT_1	51h	7	WD	Watchdog Error
INT_1	51h	6	CANINT1	CAN Bus Wake Up
INT_1	51h	5	LWU	Local Wake Up
INT_1	51h	4	WKERR	SWE Timer has Expired, SBC in sleep
INT_1	51h	3	FRAME_OVF_1	Frame Error Counter Overflow
INT_1	51h	2	CANSLNT_1	CAN bus silent for tSILENCE
INT_1	51h	1	SWPIN	SW pin used to wake device
INT_1	51h	0	CANDOM_1	CAN Bus Stuck Dominant
INT_2	52h	7	SMS	Sleep Mode Status: flagged when error causes device to go to sleep
INT_2	52h	6	PWRON	Device Power is on
INT_2	52h	5	OVCC1	OV Event on VCC1
INT_2	52h	4	UVSUP5	VSUP UV event for 5V
INT_2	52h	3	UVSUP3	VSUP UV event for 3.3V
INT_2	52h	2	UVCC1	UV Event on VCC1
INT_2	52h	1	TSD_VCC1_VEXCC	Thermal Shutdown due to VCC1 or VEXCC
INT_2	52h	0	SME	Sleep Mode Exit – when SBC goes to restart mode or Fail-Safe from sleep with VCC1 on and fault occurs on VCC1
INT_3	53h	7	SPIERR	Sets when SPI status bit is set
INT_3	53h	6	SWERR	(SW_EN and (about SWCFG)) | FRAME_OVF
INT_3	53h	5	FSM	Entered Fail-Safe Mode
INT_3	53h	4	CRCERR	SPI CRC Error Detected
INT_3	53h	3	VCC1SC	Short Circuit Event on VCC1
INT_3	53h	2	RSTR_CNT	Restart Counter Exceeded Threshold

Table 6-3. Device Interrupts (continued)

Register	Address	Bit Position	Data	Comment
INT_3	53h	1	TSD_CAN_LIN	Thermal Shutdown due to VCC2, CAN, or LIN
INT_3	53h	0	CRC_EEPROM	EEPROM CRC Error
INT_CANBUS	54h	7	UVCAN	UV Event on VCAN
INT_CANBUS	54h	6	RESERVED	N/A
INT_CANBUS	54h	5	CANHCANL	CANH and CANL shorted
INT_CANBUS	54h	4	CANHBAT	CANH shorted to battery
INT_CANBUS	54h	3	CANLGND	CANL shorted to GND
INT_CANBUS	54h	2	CANBUSOPEN	CAN Bus Opened
INT_CANBUS	54h	1	CANBUSGND	CANH shorted to GND or both CANH and CANL shorted to GND
INT_CANBUS	54h	0	CANBUSBAT	CANL shorted to VBAT or both CANH and CANL shorted to VBAT
INT_7	55h	7	HSSOC1	HSS1 overcurrent
INT_7	55h	6	HSSOL1	HSS1 Open Load
INT_7	55h	5	HSSOC2	HSS2 overcurrent
INT_7	55h	4	HSSOL2	HSS2 Open Load
INT_7	55h	3	HSSOC3	HSS3 overcurrent
INT_7	55h	2	HSSOL3	HSS3 Open Load
INT_7	55h	1	HSSOC4	HSS4 overcurrent
INT_7	55h	0	HSSOL4	HSS4 Open Load
INT_4	5Ah	7	LIN1_WUP	LIN 1 Bus Wake
INT_4	5Ah	6	LIN1_DTO	LIN 1 Dominant Time Out
INT_4	5Ah	5	RSVD	N/A
INT_4	5Ah	4	CYC_WUP	Cyclic Wake-up via Timer
INT_4	5Ah	3	MODE_ERR	Illegal Transceiver state for mode change request
INT_4	5Ah	2	OVHSS	OV Event on VHSS
INT_4	5Ah	1	EEPROM_CRC_INT	EEPROM saved configuration CRC error
INT_4	5Ah	0	UVHSS	UV Event on VHSS
INT_6	5Ch	7	TSDW	Thermal Shutdown Warning
INT_6	5Ch	6	UVCC1PW	VCC1 UV Prewarning
INT_6	5Ch	5	UVEXCC	UV Event on VEXCC
INT_6	5Ch	4	OVEXCC	OV Event on VEXCC
INT_6	5Ch	3	VEXCCSC	SC Event on VEXCC
INT_6	5Ch	2	UVCC2	UV Event on VCC2
INT_6	5Ch	1	OVCC2	OV Event on VCC2
INT_6	5Ch	0	VCC2SC	SC Event on VCC2

Each interrupt vector has a companion mask register that allows an end user to disable interrupts that the user does not want to monitor for. Interrupt vectors can be cleared by writing 0xFF to an interrupt register that the end user wants to clear.

6.4 Control

The SBC does a lot of tasks without prompting within the system; however, this is not absolute and without a controller the device cannot fulfill all of the needed tasks. All control of the SBC is done through the SPI bus of the device and all configurable behaviors from the SBC are going to be guided by these configurations. At a system level the SBC can need additional control that the SBC cannot provide so this is critical that the control system of the system is well-defined with the specific SBC used in mind.

7 Miscellaneous Features

The TCAN28XX line of devices has many features that have already been discussed; however, there are still features that are utilized in many applications that does not neatly fit into the other sections of this document. This section gives some information about local wake ups (LWU), partial networking/selective wake, and then a little dive into the GFO, nRST, and SW pins.

7.1 Local Wake Ups

The TCAN28xx line of devices includes 3 WAKE pins that can be used as local wake-up signals to the device that are called WAKE1, WAKE2, and WAKE3/DIR. Local wake-up pins can be configured to send a wake-up signal on a falling edge, rising edge, or pulse input on these pins. Local wake ups can transition the SBC out of sleep mode when the signals are received. A potential use case of this feature is to initialize a device wake-up on the closing of a car door – assume that there is a hall-effect sensor on the door to the vehicle that is wired to push the WAKE pin high when the door closes – this can be used to wake-up the SBC upon vehicle door closing as this can indicate that the vehicle can have passengers inside and IC functionality can be needed at that point.

The LWU pins do have alternative functions beyond standard wake pins. WAKE1 and WAKE2 can be used in battery monitoring applications.

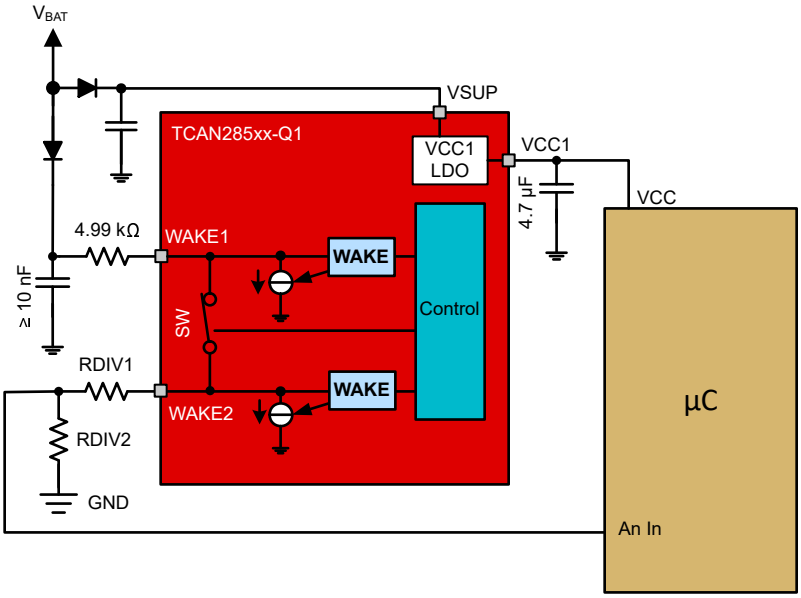

Figure 7-1. WAKE1/WAKE2 Alternative Function: Battery Monitoring with External ADC

In a battery monitoring application WAKE1 and WAKE2 are no longer LWU pins but instead act as the input and output of an analog switch. Before WAKE1 is a resistance that helps to limit current through the switch path as well as decoupling capacitor to GND. The battery signal is then transmitted through the switch and goes to a resistor divider to attenuate the voltage before this is moved to an external ADC (which can be integrated into the companion controller). The WAKE pins are capable of working up to 40V, so with a few additional resistors a battery monitoring circuit that attenuates the voltage before the ADC to prevent damage can easily be constructed if 3 local wake sources are unneeded in application.

WAKE3 also has an alternate function – as a direct drive input for the HSS module. Essentially WAKE3/DIR can be used to close/open any switch of combination of switches in the HSS module from an external source. If the HSS configuration options do not meet the systems needs WAKE3/DIR used as a direct drive pin can open up the control of the HSS module to a much larger pool of inputs.

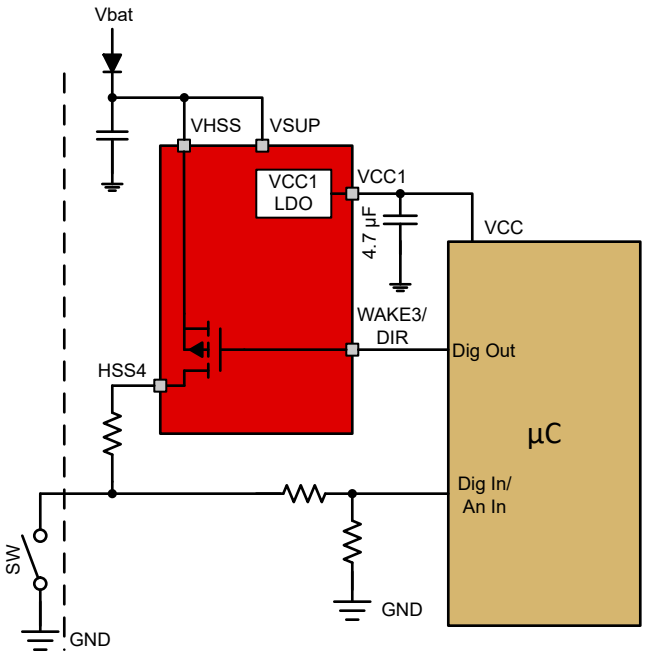

Figure 7-2. WAKE3 Alternative Function: Direct Drive for HSSx Module

While not directly an “alt function” of the wake pins – a common use case is to actually use HSS4 as a cyclic sensing wake source. During cyclic sensing wake the HSS4 module is tied to a timer (either timer1 or timer2) and the HSS4 output is directly connected to the WAKE pin – so during sleep mode HSS4 will put a signal onto the WAKE pin line to wake up the device periodically during sleep – and this can also be used in fail-safe mode as well.

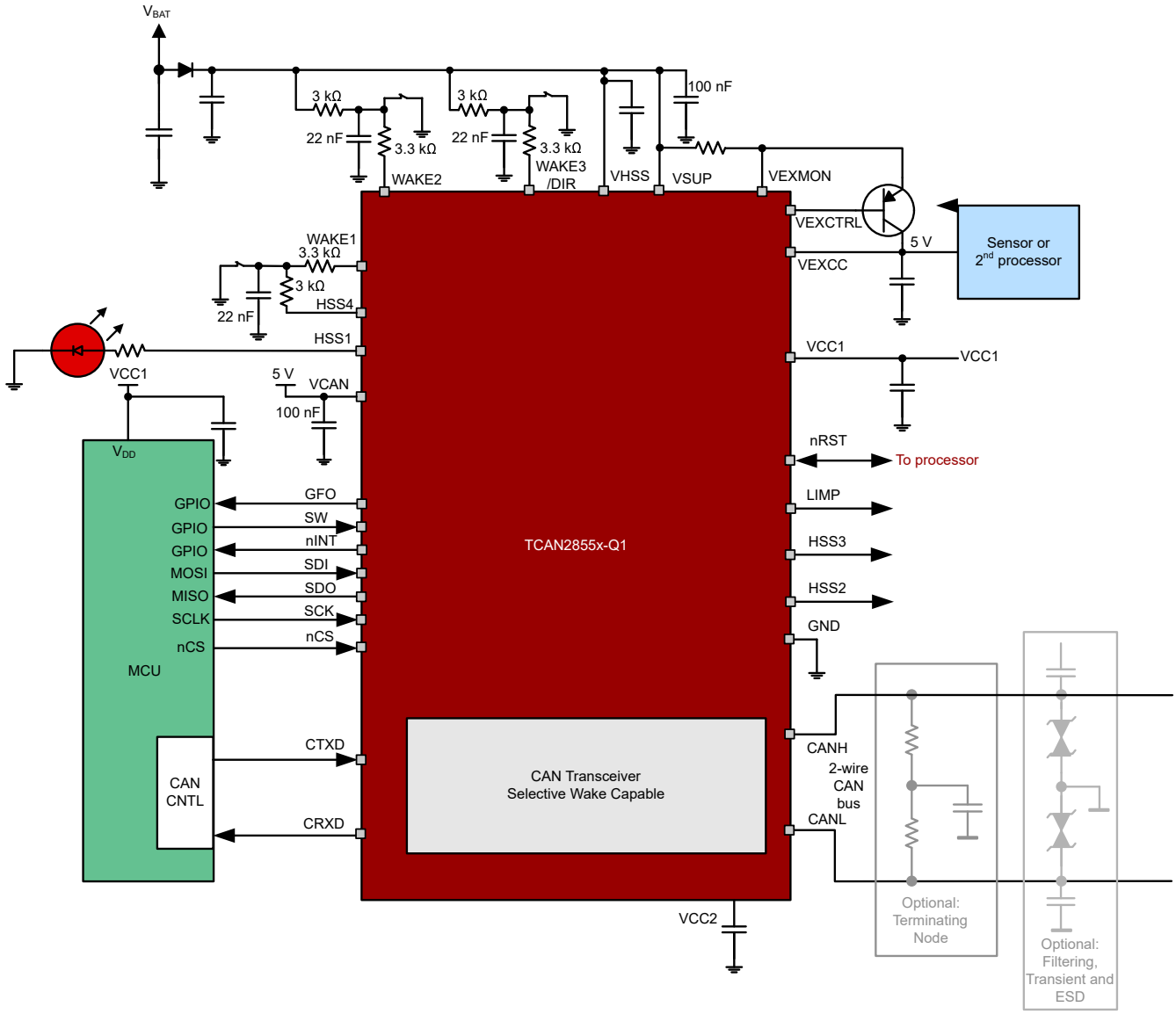

Figure 7-3. Application Showing HSS4 and WAKE1 Connected for Cyclic Sensing Wake

7.2 CAN Bus Wake Up (BWRR)

The device can also be woken up through a bus wake receive request (BWRR). When the can bus receives a wake up pattern (WUP) on the can bus while in sleep mode the device can transition to restart mode then to standby mode (assuming VCC1 is off during sleep). This can be indicated through the CRXD pin which can either latch or toggle depending on configuration chosen. This allows other devices on the bus to wake the SBC and CAN transceiver when the devices are sleeping.

A wake up pattern is defined from ISO 11898-2: 2024 and is comprised of three different parts.

1. A filtered dominant bus of least t_WK_FILTER followed by
2. A filtered recessive bus time of least t_WK_FILTER followed by
3. A second filtered dominant bus time of least t_WK_FILTER.

The sleeping device can ignore any other bus traffic that doesn't meet the conditions of a proper wake-up pattern.

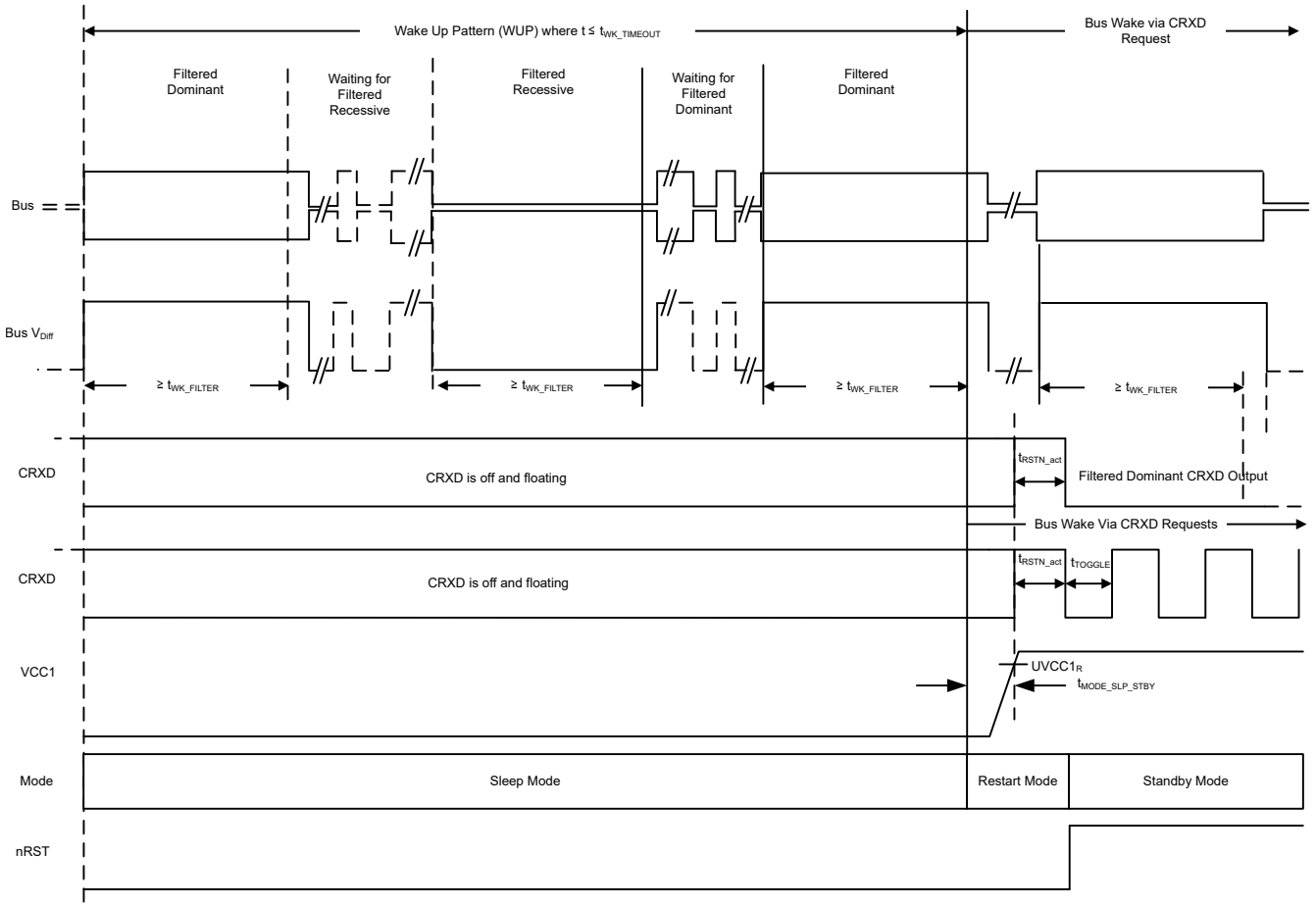

Figure 7-4. Wake-Up Pattern (WUP) on CAN Bus

7.3 Partial Networking

Partial networking allows a customizable network configuration where only select nodes in a system can respond to a CAN bus wake-up. Traditional CAN bus wake ups only require a wake-up pattern (WUP) to occur before this is recognized as a wake signal. This can be a great way to wake up all devices on the CAN bus through an active CAN device, but not every application needs or wants every CAN device to wake up for every situation. This is where partial networking comes into play – by adding a little more information after the WUP has occurred on the bus each individual CAN device can determine if this needs to wake up or not. There are three main checks that can be performed during partial networking to selectively decide what devices to wake up: ID verification, DLC verification, and data verification.

ID verification is the simplest, and most common, implementation of partial networking. In partial networking each CAN device has an 11-bit ID (classic) or can use an extended 29-bit ID depending on use. Each device within the TCAN28XX line of devices can have the ID altered based on system/application needs. If using partial networking with ID verification (lowest level of partial networking) the IDs that are accepted are a masked version of the devices ID where each bit of the mask represents a care “c” or a don’t care “d” value. If the device ID is 0b11001100110 and the mask string is 0bcccddddddddd that means any ID that meets the following pattern 0b110xxxxxxxx can wake the device up. So that means IDs such as 0b11011111111 and 0b11001010101 are valid IDs that can pass ID verification, but device IDs such as 0b01011111111 and 0b11100000000 can be rejected. This means that when using ID verification only devices that need to talk to each other are active while unneeded nodes are asleep (which saves on power consumption).

Partial networking can include even more layers of verification with DLC and data matching. The DLC field is a 4-bit number that represents how many data bytes to expect where values 0b0000 through 0b1000 represent 0 through 8 bytes respectively that can be used in classical CAN/ CAN FD and all values 0b1001 to 0b1111 represent 8 bytes only for classical CAN. If the DLC is formatted to be 0b0010 then two data bytes are expected

and if more or less than that is received the DLC matching has failed. This is only applicable when the data mask bit is set. If the data mask bit is set not only is the DLC matched to make sure proper transmission length, but the data is also matched. The TCAN28XX line of devices can configure 8 bytes of data for data verification. Data verification does work differently than ID verification as is not looking for exact matches as with ID – but just making sure that the incoming data has at least 1 matching 0b1 value. To help clarify this assume a DLC value of 1 (1 byte of data) with configured data within SBC to be 0b01010101 and now imagine two different inputs: 0b00100010 and 0b00000001. The first input 0b00100010 has no matching “1s” when compared to configured data so the first byte can fail data verification, but when looking to the second byte’s bit position 0 this is 1 for both the SBC configured data and the incoming data which means this can pass data verification.

For more details on implementation of partial networking or selective wake please see the specific device data sheet and or firmware guide.

7.4 GFO, nRST, and SW

First, the GFO pin is a general-purpose output pin and has a few potential configurations. The default is a simple general-purpose output that can be changed to either high or low via a SPI command to the SBC. This can be used to enable or inhibit an additional transceiver in case channel expansion is needed in the system, or just a general enable signal that can be utilized in multiple applications.

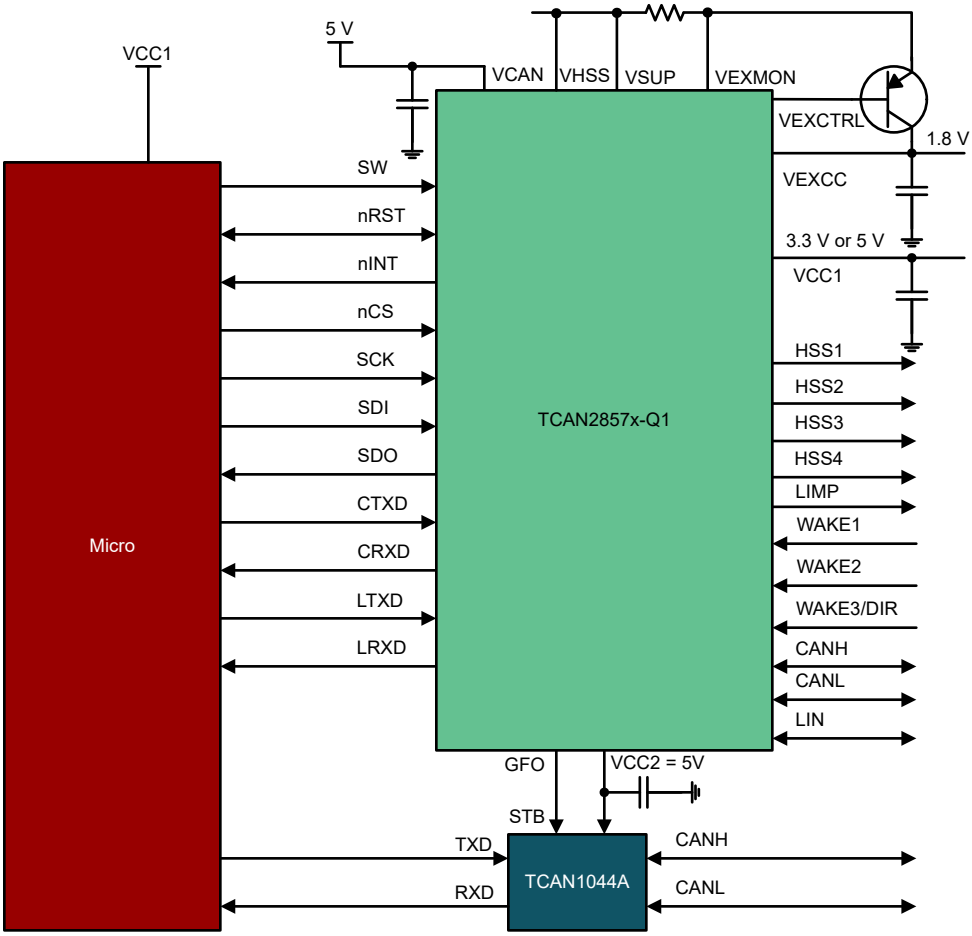

Figure 7-5. GFO Pin in Channel Expansion Application

However, the GFO pin is not just a standard output pin – this can also be used to communicate information back to the companion controller. Other functions this pin can perform are as follows: VCC1/VCC2/VEXCC electrical fault, watchdog interrupt, local wake up (LWU) request, bus wake up request (WUP), restart counter exceeded (indicated in standby mode), or a CAN bus fault. While all these functions can be accessed through SPI reads of interrupt registers and the nINT pin – the GFO pin can be configured for specific interrupts allowing the system to

respond to specific fault cases without needing to rely on a SPI read to get the pertinent information resulting in a potentially quicker system reaction time.

The next pin that can focused on in the nRST pin. This pin can indicate to companion processor when the device is in restart mode – but this pin is not just an output this also acts as an input. Applying a low signal on this pin can cause the device to perform a reset that can reload the EEPROM and set all other registers to factory setting. This is very common to use this pin and connect directly to companion controller so that controller resets when the SBC resets.

Finally, the SW pin. This pin has a few uses – but the most notable one is putting the device into software development mode. When the pin is held in active state (default high, can be changed to low) watchdog errors does not result in mode changes. The reason this is tied to *software development* is that when prototyping with this device the last thing that can be implemented is the watchdog timing as this can greatly slow down development of other features. If watchdog is active and the system is not setup for this the subsequent missed watchdogs can cause the device to switch modes – which by default the device can be active for about 3-4 seconds before entering fail-safe mode if watchdog is active and controller is unconfigured for watchdog. Holding this pin high does not stop the watchdog from operating, so watchdog testing can be done in software development mode, but this can stop negative impacts from watchdog timer. In actual systems this pin is not held in active state if this was only used for the primary purpose. That being said – this pin can also act as a digital wake-up pin in addition to the analog WAKE pins offered by the device.

8 Summary

The TCAN28xx line of devices are robust mid-range SBCs that have a dense feature set. While initially these devices can come off as overwhelming – the reality is that most of the features are relatively simple to understand as well as implement. This guide is meant to provide a high level understanding of the devices and potential features. After reading this guide a basic understanding of the differences between devices within this family, the devices state machine, main subsystems of the SBC, protection features, and miscellaneous features needs to be understood. This guide does not give exhaustive specification data, nor does this give a in-depth look into the firmware setup – for more information on those topics please see the devices data sheet and the firmware manual. For any remaining questions please reach out to us on E2E where one of our applications engineers can take a look at the inquiry.

9 References

- Texas Instruments, *Firmware Guide for TCAN24xx and TCAN28xx Devices*, application note.
- Texas Instruments, *TCAN241x-Q1 Automotive CAN FD System Basis Chip (SBC) with Integrated Buck Regulator and Watchdog*, data sheet .
- Texas Instruments, *TCAN245x-Q1 Automotive Signal Improvement Capable CAN FD System Basis Chip (SBC) with Integrated Buck Regulator and Watchdog,*, data sheet.
- Texas Instruments, *TCAN284xx-Q1 Automotive CAN FD and LIN System Basis Chip (SBC) with Integrated Watchdog, Selective Wake and Advanced CAN Bus Fault Diagnostics*, data sheet.
- Texas Instruments, *TCAN285x-Q1 Automotive CAN FD SIC and LIN System Basis Chip (SBC) with Wake Inputs and High-side Switches*, data sheet .

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