Product Overview
Isolating I2C Plus SPI Signals

TEXAS INSTRUMENTS
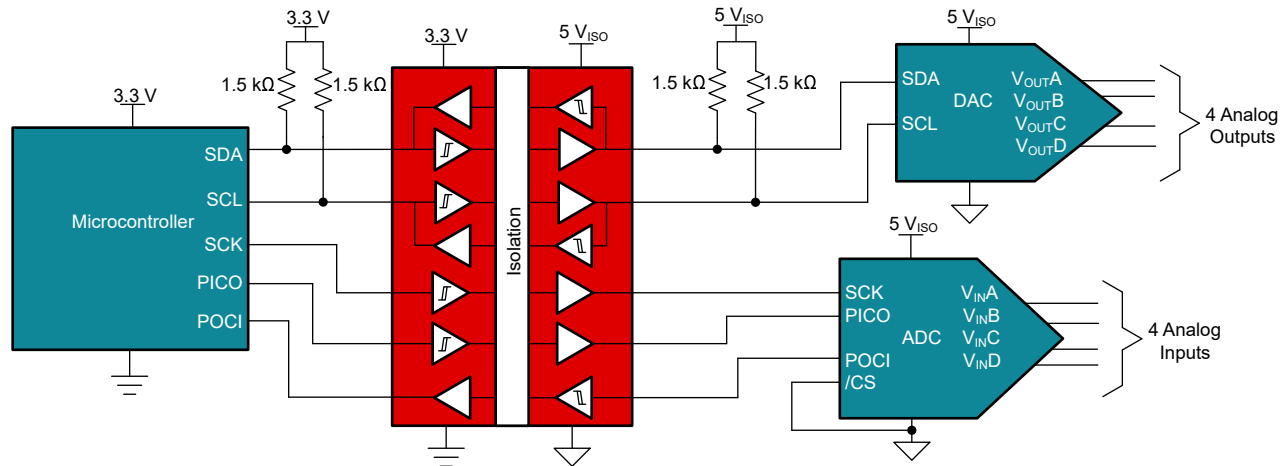
Example I2C Plus SPI Isolation Block Diagram

Design Considerations

- Prevents DC and unwanted AC currents between controller devices and peripheral ICs
- Allows signal transfer between controller devices and peripheral ICs
- Protects low voltage parts in a system from high voltage circuits
- Diminishes the effect of ground potential differences
- [FAQ] Why is the logic LOW level output voltage, VOL1, up to 0.8 V on Side 1 of the ISO1540/ISO1541 and ISO1640/ISO1641 bidirectional I2C isolators?
- [FAQ] How to calculate the maximum SPI speed supported by a digital isolator?
- I2C Bus Pullup Resistor Calculation
- How do Isolated I2C Buffers with Hot-Swap Capability and IEC ESD Improve Isolated I2C?

  Need additional assistance? Ask our engineers a question on the *TI E2E™ Isolation Support Forum*

Recommended Parts

Part Number	Voltage Range	Data Rate	Bidirectional SCL Communication	Features
ISO1644	3.0 - 5.5 V (Side 1) 2.25 - 5.5 V (Side 2)	**I2C** Standard Mode (0 to 100 kbps) Fast Mode (0 to 400 kbps) Fast-mode Plus (0 to 1 Mbps) High-Speed Mode (0 to 3.4 Mbps) **SPI** 0 to 50 Mbps	✓	High CMTI Reinforced Isolation Hot-Swappable I2C Connections Enhanced EMC Isolated SPI Support (POCI, PICO, CLK)

For more isolated I2C devices, browse through the *online parametric tool*; for device recommendations related to isolating SPI signals without I2C, please refer to the *Isolating SPI Signals* product overview.

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