User's Guide

THVD8000 EVM User's Guide

ABSTRACT

This user's guide describes the evaluation module (EVM) for a RS-485 over power transceiver THVD8000. This EVM helps designers evaluate the device performance for fast development and analysis of data transmission systems with power delivery on the same two wires.

Table of Contents

List of Figures

List of Tables

Trademarks

1 Overview

In the 1980s, the Electronics Industries Association (EIA) approved a balanced transmission standard called RS-485, which has become the industry's interface workhorse with widespread usage in various end equipment. Leveraging RS-485 physical layer signaling, THVD8000 enables power line communication on the same two wires. Built-in OOK modulation enables RS-485 data to be directly coupled onto existing power cables via series capacitors without any updates to the MCU or the controller. The THVD8000 receiver extracts the data from the power cables after AC-coupling by using a precise bandpass filter and a demodulator.

1.1 THVD8000 Operation

In the block diagram (Figure 1-1), a point to point communication is set up with two THVD8000EVM boards to demonstrate the THVD8000 functionality. In this test, the input TTL data from a microcontroller (MCU) is OOK modulated by THVD8000. The input low is converted to a high frequency clock signal, while the input high stays as a DC voltage. The signal is carried with DC power on the same bus for transmitting. the device in the receiver side demodulates the differential signal to digital domain, while the power is separated to drive the load.

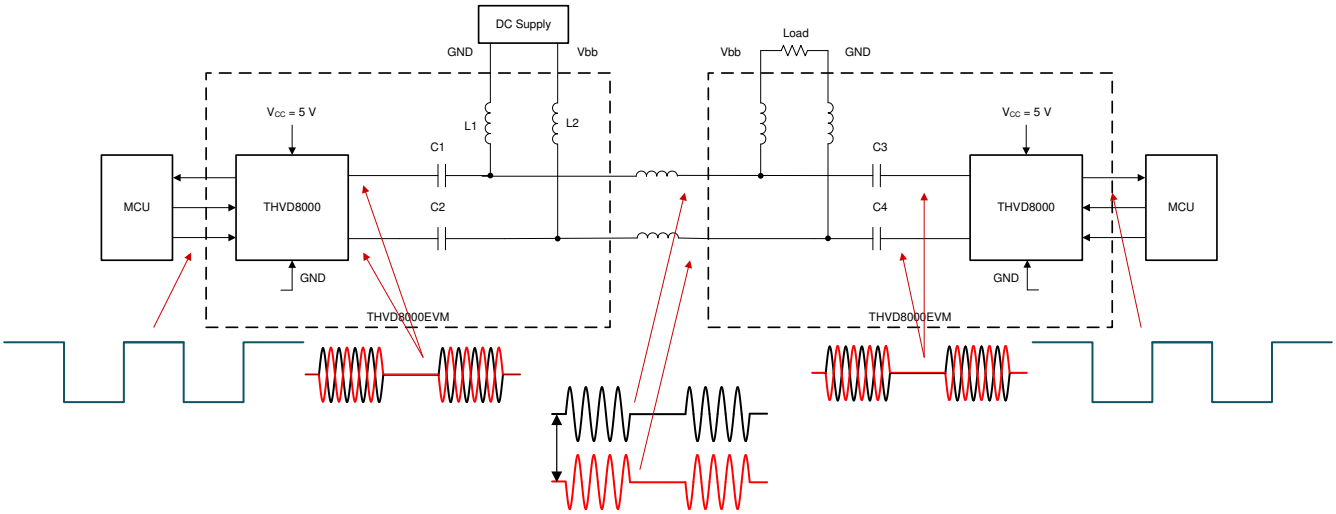

Figure 1-1. THVD8000 Operation

2 EVM Schematic and Layout

The THVD8000 EVM has simple connections to all necessary pins of the THVD8000 transceiver device, and jumpers where necessary to provide flexibility for device pin and data over power configuration. There are test points (loops) for all main points where probing is necessary for evaluation such as GND, VCC, D, R, A/B (bus pins), Pin 3 (MODE pin). The EVM supports many options for data over power configuration, such as various carrier frequencies via the pre-installed resistor bank. The EVM is pre-configured with two 120-Ω resistors that may be connected on the bus via jumpers. The inductor and capacitor for power delivery are also pre-installed for quick evaluation. TVS diodes for protection and other footprints are available for customer installation of the desired component(s).

2.1 THVD8000EVM Schematic

The schematic is shown in Figure 2-1. The function of each jumper and test point is listed in Table 2-1.

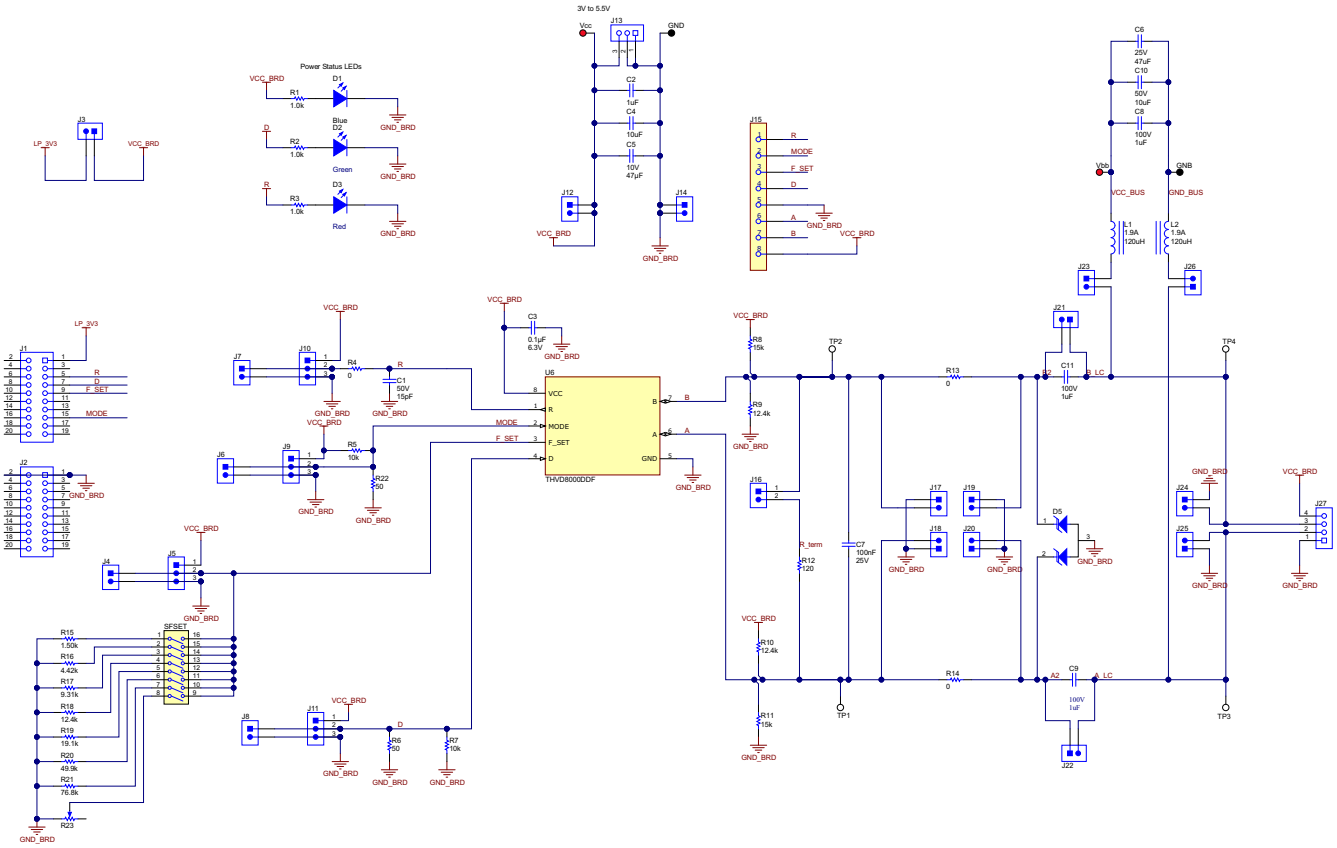

Figure 2-1. THVD8000EVM Schematic

Table 2-1. Jumpers and Test points

Connection	Type	Description
J1/J2	20 pin jumper	Used for optional external LaunchPad connection
J3	2 pin jumper	V_{CC} supply from LaunchPad (optional)
J4	2 pin jumper	F_SET, device pin 3 probing
J5	3 pin jumper	F_SET shunt to V_{CC} or GND
J6	2 pin jumper	MODE, device pin 2 probing
J7	2 pin jumper	R, device pin 1 probing
J8	2 pin jumper	D, device pin 4 probing
J9	3 pin jumper	Used for mode selection on pin 2. Shunt to Vcc for transmitting mode, shunt to GND for receiving mode.
J10	3 pin jumper	R pin shunt to V_{CC} or GND
J11	3 pin jumper	D pin shunt to V_{CC} for sending bit '1' or to GND for sending bit '0'
J12	2 pin jumper	V_{CC} input
J13	3 pin connector	V_{CC} and GND input (pin 1 and pin 2: GND; pin 3: V_{CC}c)
J14	2 pin jumper	GND input
J15	1 Socket	DDF socket (unpopulated)
J16	2 pin jumper	Connect 120 Ω termination to the bus.
J17	2 pin jumper	B probing
J18	2 pin jumper	A probing
J19	2 pin jumper	B probing

Table 2-1. Jumpers and Test points (continued)

Connection	Type	Description
J20	2 pin jumper	A probing
J21	2 pin jumper	Bypass B decoupling capacitor (unpopulated)
J22	2 pin jumper	Bypass A decoupling capacitor (unpopulated)
J23	2 pin jumper	Connecting inductor to bus B
J24	2 pin jumper	B probing (bus side after cap)
J25	2 pin jumper	A probing (bus side after cap)
J26	2 pin jumper	Connecting inductor to bus A
J27	4 pin connector	Bus wire connector (pin 1: GND, pin 2: B, pin 3: A, pin 4: V_{CC})
SFSET	8 position SPST switch	To set resistor value for carrier frequency selection
TP1	Test Point	A test point
TP2	Test Point	B test point

2.2 THVD8000EVM Layout

THVD8000EVM board layout is shown in Figure 2-2.

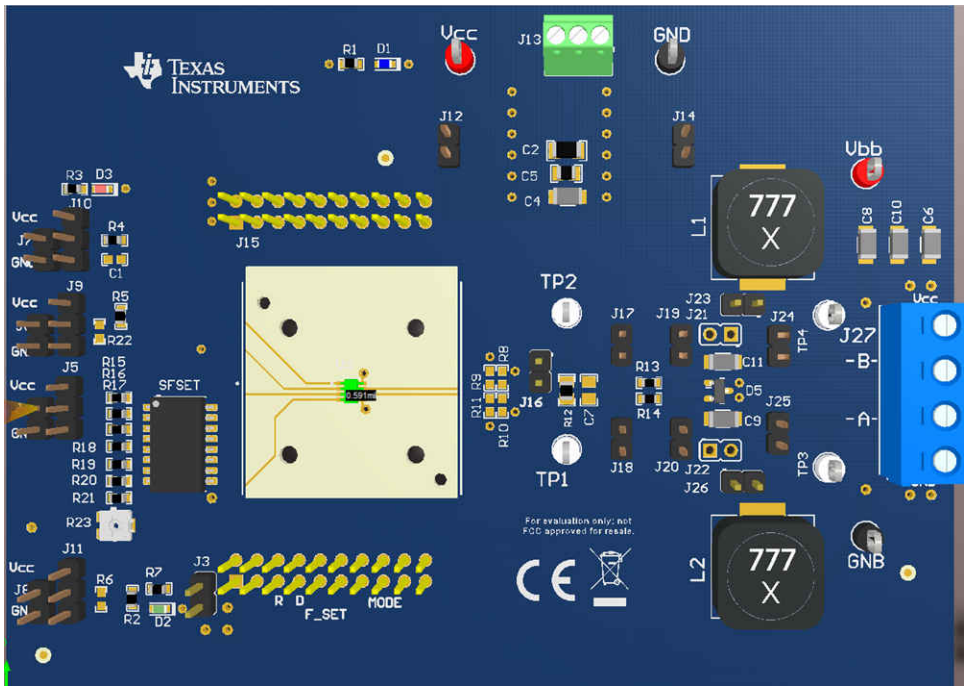

Figure 2-2. THVD8000EVM Layout

3 THVD8000EVM Setup and Operation

This section describes the setup and operation of the EVM for functional and parameter performance evaluation.

3.1 Overview and Basic Operation Settings

3.1.1 Transceiver V_{CC} power supply (J12 or J13 or V_{CC}) and GND (J14 or J13 or GND)

The basic setup of the THVD8000 EVM uses a single 3.3-V or 5-V power supply to evaluate the transceiver's performance. To power the transceiver, connect the 5-V or 3.3-V V_{CC} supply to the J12/J14 or J13 jumper headers or the V_{CC} and GND test-point loops. The power supplied should meet the required specification of V_{CC} for the transceiver being tested. LED D1 (blue) is used to indicate V_{CC} presence.

3.1.2 Power delivery supply V_{bb} (V_{bb}) and GNB (GNB)

To transfer the power on the same two wires as data, connect the supply to the V_{bb} and GNB test-point loops.

3.1.3 D input (J8 or J11)

The D (pin 4) of the transceiver, transmit data is routed to J8 or J11. The signal path to the J8 header is pre-installed with a 10-kΩ pull-down resistor R7 to GND. LED D2 (Green) is used to indicate a high state on D.

3.1.4 MODE input (J6 or J9)

The MODE (pin 2) of the transceiver sets the mode of the device. Pin 2 is routed to J6 or J9. The signal path to the J9 header is pre-installed with a 10-kΩ pull-up resistor R5 to V_{CC}.

3.1.5 F_SET input (J4 or J5)

The F_SET (pin 3) of the transceiver sets the carrier frequency of the OOK modulation of the device. The various resistors R15 (1.5 kΩ), R16 (4.4 kΩ), R17 (9.3 kΩ), R18 (12.4 kΩ), R19 (19 kΩ), R20 (50 kΩ), R21 (77 kΩ) are pre-installed with a dip switch SFSET for selection. A potentiometer with the range from 10 Ω to 10 kΩ, R23, is pre-installed for choosing the other resistance value, by which the larger resistance is obtained with rotating the head clockwise.

Table 3-1. F_SET Pin Resistor Selection

Resistor	Resistance (Ω)	Carrier frequency (kHz)
R15	1.5k	5000
R16	4.4k	2000
R17	9.3k	1000
R18	12.4k	750
R19	19k	500
R20	50k	187.5
R21	77k	125
R23	10-10k	variable

3.1.6 R output (J7 or J10)

The R (pin 1) of the transceiver, receive data is routed to J7 or J10. The signal path to the J10 header is pre-installed with a 0-Ω series resistor, R4. LED D3 (red) is used to indicate a high level on R.

3.1.7 Termination (J16)

Using header J16 makes the bus terminated with a pre-installed 120-Ω resistor, R12.

3.1.8 Capacitor and inductor bypass (J21, J22, J23, J26)

The headers J21 and J22 make the signal path bypass the decoupling capacitor C9 and C11. The headers J23 and J26 make the coupling inductor L1 and L2 connect to the signal path.

3.1.9 Wire connection (J27)

The header J27 makes the signal path to connect the media externally, such as a cable.

Table 3-2. J27 pin connection

Pin	Connection	Description
1	GND	Pin 4 of Transceiver. GND.
2	A	Bus wire
3	B	Bus wire
4	V_{CC}	Pin 1 of Transceiver. V_{CC}

3.2 Operation Example

This example shows step-by-step how to operate two boards for data over power communication.

1. Two EVM boards are required. Connect a 3.3-V to 5-V power supply capable of 100 mA to the test points V_{CC} and GND of each EVM boards. Due to the isolation of the signal path, the two boards can be powered by separate sources and with ground potential differences. The GND and Vcc connections are marked by the silk screen. This will be the main supply for the boards.
2. (Optional) Connect V_{bb} and GNB through V_{bb} and GNB connectors for power delivery. Short the shunt TL_A and TL_B to connect the inductor to bus. The maximum DC current rating of the populated inductor on the EVM is 1.9 A. The voltage rating of the populated capacitor is 100 V. On the transmitting board, V_{bb} and GNB connect to the power source, like a 12 V DC. On the receiving board, Vbb and GNB connect to the loading circuit (Figure 1). The received power may have a lower voltage level due to the cable loss.
3. Put a shunt connector on J9-2 (MODE pin) to V_{CC} on the transmitting board. Put a shunt connector on J9-2 (MODE pin) to GND on the receiving board. In this configuration, THVD8000 would work in transmitter or receiver mode only. Another option is to connect the MODE pin to an MCU control logic, for example, the signal that controls the DE/RE control inputs of a half-duplex transceiver.
4. Close one of the switches where the silk screen label shows SFSET for the carrier frequency selection. SFSET needs to be selected for both transmitting and receiving boards. Put the F_SET dip switch on the same setting on both boards.
5. Connect transmitting and receiving boards by a two-wire twisted cable by J27.
6. Connect the function generator to the J11-2 header on the transmitting board. Set the function generator to generate a square wave of a certain frequency, 50% duty cycle, the low voltage level to 0 V, and the high level to 5 V. This clock signal simulates the TTL data from MCU. Alternatively PRBS data from a signal generator can be transmitted. Please note the data rate is not recommended to be faster than 1/10 of the carrier frequency. The transmitted signal can be checked on an oscilloscope by test points TP1 and TP2 on the transmitting board, which should show a nearly rail-to-rail OOK modulated waveform at the carrier frequency. This indicates that the transmitter of THVD8000 operates correctly.
7. Connect an oscilloscope probe to the J10-2 pin on the receiving board. Setup the oscilloscope for proper time and voltage per division. Allow room to show three periods of bit-long waveform on the oscilloscope. The received TTL signal should match the transmitted data. This indicates that the receiver of THVD8000 operates correctly. Similarly the received signal can be checked on an oscilloscope by test points TP1 and TP2 on the receiving board. The received signal may have smaller amplitude due to the cable loss.
8. Both transmitting and receiving and functions can be tested for each board with swapped mode by repeating step 3 to 7.

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (May 2020) to Revision A (July 2021)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	2

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